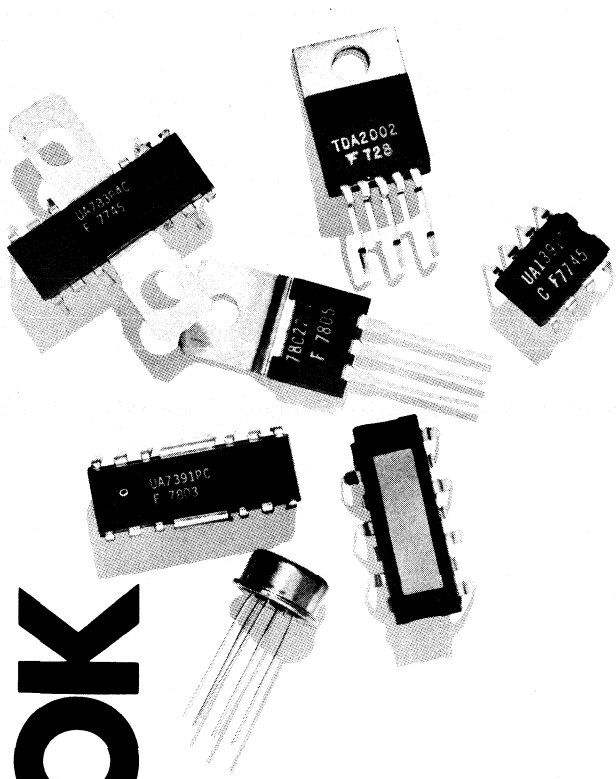
LINEAR CONSUMER DATA BOOK



FAIRCHILD

INTRODUCTION

The application of linear integrated circuit technology to consumer electronics pioneered by Fairchild with the μA703 RF-IF amplifier in 1967 has become one of the fastest growing segments of the linear market.

Today, systems ranging from home safety and appliances to television receivers to automotive control systems are economically performing complex functions with ever improving reliability. Fairchild Linear has been a major factor in the growth of this industry with:

- "State of the Art" technologies including ion implant, I^2L and compatible FET/linear processes.
- A continuing program of quality and reliability improvement to meet the ever increasing requirements of this industry and the end user of all of these systems — the consumer.
- High-volume, low-cost manufacturing.
- Cooperative product planning with our customers to achieve optimum system performance.

The combination of new technologies, new markets and new applications are continually bringing forth new circuits for the consumer market. Fairchild encourages discussion of your new ideas and is prepared to quote custom circuits for your high volume applications.

In summary, the Fairchild Consumer Linear team is working with customers to bring to the market linear circuits which will optimize cost and performance requirements of consumer electronic products — and they are being reliably produced in volume.

Contact us for your consumer needs. Put Fairchild to work for you.

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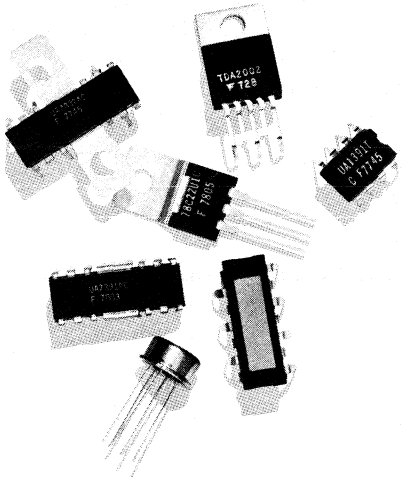

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1458CE	μA1458CHC	
1458CP	μA1458CTC	
1458E	μA1458HC	
1458P	μA1458TC	
1558E	μA1558HM	
3207A		9645DC
3245	9645/3245	
527		μA760HM
532		μA798TC
536		μA740AHM
556CJ	μA556PC	
709AE	μA709AHM	
709AH	μA709AFM	
709AL	μA709ADM	
709BE	μA709HM	
709BH	μA709FM	
709BL	μA709DM	
709CE	μA709HC	
709CJ	μA709PC	
709CL	μA709DC	
710BE	μA710HM	
710BH	μA710FM	
710BL	μA710DM	
710CE	μA710HC	
710CL	μA710DC	
711BE	μA711HM	
711BH	μA711FM	
711BL	μA711DM	
711CE	μA711HC	
711CJ	μA711PC	
711CL	μA711DC	
723BE	μA723HM	
723BL	μA723DM	
723CE	μA723HC	
723CJ	μA723PC	
723CL	μA723DC	
733DC	μA733DC	
733DM	μA733DM	
733FM	μA733FM	
733HC	μA733HC	
733HM	μA733HM	
741BE	μA741HM	
741BH	μA741FM	
741BL	μA741DM	
741CE	μA741HC	
741CJ	μA741PC	
741CP	μA741TC	
747BE	μA747HM	
747BL	μA747DM	
747CE	μA747HC	
747CJ	μA747PC	
747CL	μA747DC	
748BE	μA748HM	
748BH	μA748FM	
748BL	μA748DM	
748CE	μA748HC	
748CL	μA748DC	
748CP	μA748TC	
75S107		75107APC
75S108		75108APC
75S207		75207PC
75S208		75208PC
75322	9643DC	
75361	9644DC	
75361A		9643DC
75363	9643DC	
75450N	75450APC	
78M05BE	μA78M05HM	
78M05CE	μA78M05HC	
78M06BE	μA78M06HM	
78M06CE	μA78M06HC	
78M08BE	μA78M08HM	
78M08CE	μA78M08HC	
78M12BE	μA78M12HM	
78M12CE	μA78M12HC	
78M15BE	μA78M15HM	
78M15CE	μA78M15HC	
78M20BE	μA78M20HM	
78M20CE	μA78M20HC	
78M24BE	μA78M24HM	
78M24CE	μA78M24HC	
8216	μA8T26A	
8T26A	μA8T26APC	
8T26A	μA8T26ADC	
AN217		μA721PC
AM26LS29		9634
AM26LS30		9636A
AM26S10	9640	
AM26S11	9641	
AN559	μA0802	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
CA1190	TDA1190Z	
CA1310	μA1310	
CA3004T		μA703HC
CA3005T		μA703HC
CA3006T		μA703HC
CA3008		μA741FM
CA3008A		μA741FM
CA3010		μA741HM
CA3010A		μA741HM
CA3011T		μA753TC
CA3012T		μA753TC
CA3013T		μA753TC
CA3014T		μA753TC
CA3015		μA741HM
CA3015A		μA741HM
CA3016		μA741FM
CA3016		μA741FM
CA3018	μA3018HM	
CA3018A	μA3018HM	
CA3019	μA3019HM	
CA3021T		μA757DC
CA3022T		μA757DC
CA3023T		μA757DC
CA3026	μA3026HM	
CA3028AT		μA703HC
CA3028T		μA703HC
CA3029		μA741TC
CA3029A		μA741TC
CA3030		μA741TC
CA3030A		μA741TC
CA3036	μA3036HM	
CA3037		μA741DM
CA3037A		μA741DM
CA3038		μA741DM
CA3038A		μA741DM
CA3039	μA3039HM	
CA3041E		μA3065PC
CA3024E		μA3065PC
CA3043		μA3065PC
CA3044T		μA3064
CA3045	μA3045DM	
CA3046	μA3046DC	
CA3045	μA3054DC	
CA3058E		μA742DC
CA3059		μA742DC

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
CA3064E	μA3064PC	
CA3064T	μA3064HC	
CA3065E	μA3065PC	
CA3070E	μA780PC	
CA3071E	μA781PC	
CA3072E	μA746PC	
CA3075E	μA3075PC	
CA3078AS		μA776DM
CA3078AT		μA776HM
CA3078S		μA776TC
CA3078T		μA776HC
CA3079		μA742DC
CA3085		μA723HC
CA3085A		μA723HC
CA3085AF		μA723DC
CA3085AS		μA723DC
CA3085B		μA723HM
CA3085BF		μA723DM
CA3085BS		μA723DC
CA3085F		μA723DC
CA3085S		μA723DC
CA3086	μA3086DC	
CA3088E		μA720PC
CA3089E	μA3089PC	
CA3090E		μA758PC
CA3123E	μA720PC	
CA3126Q	μA787PC	
CA3134		TDA1190
CA3458S	1458TC	
CA3458T	1458HC	
CA3558S		1558HM
CA3558T	1558HM	
CA3741CS	μA741TC	
CA3741CT	μA741HC	
CA3741S		μA741HM
CA3741T	μA741HM	
CA3747CE	μA747PC	
CA3747CF		μA747DC
CA3747CT	μA747HC	
CA3747E	μA747DM	
CA3747F	μA747DM	
CA3747T	μA747HM	
CA3748CS	μA748TC	
CA3748CT	μA748HC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
CA3748S		μA748HM
CA3748T	μA748HC	
CA758E	μA758PC	
DAC-08	μA0801	
DAC-08A	μA0801A	
DAC-08C	μA0801C	
DAC-08E	μA0801E	
DS0026	9646/0026	
DS3486		9637A
DS3487		9634
DS3645	9645/3245	
DS3691		9636A
DS3692		9634
DS8834		μA8T26A
DS8835		μA8T26A
DS78LS120		9637A
DS8T26A	μA8T26A	
HA1156	μA1310	
HA11226		μA7300
LA1201		μA721PC
LAS1405	μA78H05KC	
LAS1412	μA78H12KC	
LAS1415	μA78H15KC	
LF111H	μAF111HM	
LF155AH	μAF155AHM	
LF155H	μAF155HM	
LF156AH	μAF156AHM	
LF156H	μAF156HM	
LF157AH	μAF157AHM	
LF157H	μAF157HM	
LF211H	μAF211HM	
LF311H	μAF311HC	
LF355AH	μAF355AHC	
LF355H	μAF355HC	
LF356A	μAF356AHC	
LF356H	μAF356HC	
LF357	μAF357HC	
LF357A	μAF357AHC	
LH0002	SH0002	
LH0021CK		μA791KC
LH0021K		μA791KM
LH0021K/883		μA791KMQB
LH0041		μA759HM
LH0061C		μA791KC
LH0061CK		μA791KM

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LH0061K		μA791KM
LH101H		μA741HM
LH201H		μA741HM
LH2101AD		μA747ADM
LH740AH		μA740AHM
LM101AD	μA101ADM	
LM101AF	μA101AFM	
LM101AH	μA101AHM	
LM101D	μA101DM	
LM101H	μA101HM	
LM1011		μA7300
LM102H	μA102HM	
LM104H	μA104HM	
LM105H	μA105HM	
LM106F		μA710FM
LM106H		μA710HM
LM107H	μA107HM	
LM108AD	μA108ADM	
LM108AF	μA108AFM	
LM108AH	μA108AHM	
LM108D	μA108DM	
LM108F	μA108FM	
LM108H	μA108HM	
LM109K	μA109KM	
LM111H	μA111HM	
LM117		μA78GKM
LM120H-05		μA79M05HM
LM120H-12		μA79M12HM
LM120H-15		μA79M15HM
LM120K-05		μA7905KM
LM120K-12		μA7912KM
LM124D	μA124DM	μA3503DM
LM1303N		μA749PC
LM1304N	μA732PC	
LM1307N	μA767PC	
LM1310	μA1310	
LM139	μA139DM	
LM139A	μA139ADM	
LM1414J		μA711DC
LM1458H	μA1458HC	
LM1458N	μA1458TC	
LM1488J	μA1488	9616DC
LM1489AJ	μA1489A	9617DC
LM1489J	μA1489	9617DC
LM1496H	μA796HC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM1496N	μA796PC	
LM1514J		μA711DM
LM1558H	μA1558HM	
LM160H	μA760HM	
LM1800N	μA758PC	
LM1820N	μA720PC	
LM1829N	μA787PC	
LM1841N	μA2136PC	
LM1850N		μA7390PC
LM198	μAF198	
LM210AF	μA201AFM	
LM201AH	μA201AHM	
LM201D	μA201DM	
LM201H	μA201HM	
LM202H	μA202HM	
LM204H	μA204HM	
LM205H	μA205HM	
LM206F		μA710FM
LM206H		μA710HC
LM207H	μA207HM	
LM208AD	μA208ADM	
LM208AF	μA208AFM	
LM208AH	μA208AHM	
LM208D	μA208DM	
LM208F	μA208FM	
LM208H	μA208HM	
LM209K	μA209KM	
LM220H-05		μA79M05HM
LM220H-12		μA79M12HM
LM220H-15		μA79M15HM
LM220K-05		μA7905KM
LM220K-12		μA7912KM
LM220K-15		μA7915KM
LM222N		μA555TC
LM224D	μA224DM	
LM2901N	μA2901PC	μA775PC
LM2902N	μA2902PC	
LM2904N		μA798TC
LM2905N		μA555TC
LM2907N		μA4151TC
LM2917N		μA7151PC
LM301AD	μA301ADC	
LM301AH	μA301AHC	
LM301AN	μA301ATC	
LM3018AH	μA3018HM	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM3018H	μA3018HM	
LM3019H	μA3019HM	
LM302H	μA302HC	
LM3026H	μA3026HM	
LM3039H	μA3039HM	
LM304H	μA304HC	
LM3045D	μA3045DM	
LM3046N	μA3046DC	
LM305AH	μA305AHC	
LM305H	μA305HC	
LM3053N	μA753TC	
LM3054N	μA3054DC	
LM306H		μA710HC
LM3064H	μA3064HC	
LM3065N	μA3065PC	
LM307H	μA307HC	
LM307N	μA307TC	
LM3070N	μA780PC	
LM3075N	μA3075PC	
LM308AD	μ308ADC	
LM308AH	μA308AHC	
LM308D	μA308DC	
LM308H	μA308HC	
LM308N	μA308TC	
LM3086N	μA3086DC	
LM309K	μA309KC	
LM311H	μA311HC	
LM311N	μA311TC	
LM320H-05		μA79M05HC
LM320H-12		μA79M12HC
LM320H-15		μA79M15HC
LM320K-05		μA7905KC
LM320K-12		μA7912KC
LM320K-15		μA7915KC
LM320MP-12		μA79M12AUC
LM320MP-15		μA79M15AUC
LM320MP-5.0		μA79M05AUC
LM320MP-6.0		μA79M06AUC
LM320MP-8.0		μA79M08AUC
LM320T-12		μA7912UC
LM320T-15		μA7915UC
LM320T-18		μA7918UC
LM320T-24		μA7924UC
LM320T-5		μA7905UC
LM320T-6		μA7906UC

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM320T-8		μA7908UC
LM323K	SH323KC	
LM323K	μA78H05KC	
LM324D	μA324DC	μA3403DC
LM324N	μA324PC	μA3403PC
LM339A	μA339ADC	
LM340K-05	μA7805KC	
LM340K-06	μA7806KC	
LM340K-08	μA7808KC	
LM340K-12	μA7812KC	
LM340K-15	μA7815KC	
LM340K-18	μA7818KC	
LM340K-24	μA7824KC	
LM340T-05	μA7805UC	
LM340T-06	μA7806UC	
LM340T-08	μA7808UC	
LM340T-12	μA7812UC	
LM340T-15	μA7815UC	
LM340T-18	μA7818UC	
LM340T-24	μA7824UC	
LM342P-12		μA78C12U1C
LM342P-15		μA78C15U1C
LM342P-18		μA78C18U1C
LM342P-24		μA78C24U1C
LM342P-5.0		
LM342P-6.0		
LM432P-8.0		μA78C08U1C
LM350N		75453BPC
LM351N	75453BPC	
LM358H	μA798HM	
LM360H	μA760HC	
LM376N	μA376TC	
LM380N		TBA820L
LM381AN		μA739DC
LM381N		μA739PC
LM382N		μA739PC
LM383	TDA2002	
LM386		μA7307
LM387N		μA739PC
LM388N		TBA820L
LM390	μAF398	
LM3905N		μA555TC
LM4250H		μA776HM
LM4250CH		μA776HC
LM4250CN		μA776DC
LM4250H		μA776HM
LM5108AJ	75108ADC	
LM55107AJ	55107ADM	
LM55108AJ	55108ADM	
LM55109J	55109DM	
LM55110J	55110A	
LM5524J	55S24	
LM5528J	5528DM	
LM5534J	55S234DM	
LM555CN	μA555TC	
LM556CN	μA556PC	
LM703LH	μA703HC	
LM709CH	μA709HC	
LM709CN	μA709PC	
LM709H	μA709HM	
LM710CH	μA710HC	
LM710CN	μA710PC	
LM710H	μA710HM	
LM711CH	μA711HC	
LM711CN	μA711PC	
LM711H	μA711HM	
LM723CD	μA723DC	
LM723CH	μA723HC	
LM723CN	μA723PC	
LM723D	μA723DM	
LM723H	μA723HM	
LM725AH	μA725AHM	
LM725CH	μA725HC	
LM725H	μA725HM	
LM733CD	μA733DC	
LM733CH	μA733CH	
LM733CN	μA733PC	
LM733D	μA733DM	
LM733H	μA733HM	
LM741CD	μA741DC	
LM741CH	μA741HC	
LM741CN-08	μA741TC	
LM741CN-14	μA741PC	
LM741F	μA741FM	
LM741H	μA741HM	
LM746N	μA746PC	
LM747CD	μA747DC	
LM747CH	μA747HC	
LM747CN	μA747PC	
LM747D	μA747DM	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM747H	μA747HM	
LM748CH	μA748HC	
LM748CN	μA748TC	
LM748H	μA748HM	
LM75107AJ	75107ADC	
LM75107AN	75107APC	
LM75108AN	75108APC	
LM75109J	75109DC	
LM75109N	75109PC	
LM75110J	75110A	
LM75110N	75110A	
LM75150J	75150DC	
LM75150N	75150PC	9616DC
LM75154J	75154DC	9617DC
LM75154N	75154PC	
LM75207J	75207DC	
LM75207N	75207PC	
LM75208J	75208DC	
LM75208N	75208PC	
LM7524J	75S24	
LM7524N	75S24	
LM7528J	7528DC	
LM7528N	7528PC	
LM75325J	75325DC	
LM75325N	75325PC	
LM7534J	75S234DC	
LM7534N	75S234PC	
LM7535J	7535DC	
LM7535N	7535PC	
LM75450J	75450BDC	
LM75450N	75450BPC	
LM75451N	75451BTC	
LM75452N	75452BTC	
LM75453N	75453BTC	
LM75454N	75454BTC	
M51728		μA7392
MC1303P		μA749PC
MC1304P	μA732PC	
MC1305P		μA732PC
MC1306		μA7307
MC1307P	μA767PC	
MC1310P	μA1310PC	
MC1311P	μA758PC	
MC1312P	μA1312PC	
MC1324P		μA746PC
MC1326P		μA746PC
MC1327		TDA2522
MC1328P		μA746PC
MC1339P		μA749PC
MC1350P		μA757DC
MC1351P		μA3065PC
MC1352P		μA757DC
MC1353P		μA757DC
MC1355P		μA3065PC
MC1357P	μA2136PC	
MC1358P		μA3065PC
MC1364P	μA3064PC	
MC1370P	μA780PC	
MC1371P	μA781PC	
MC1375P	μA3075PC	
MC1391	μA1391TC	
MC1394P	μA1394TC	
MC1398P		μA787PC
MC1408L6	μA0802C	
MC1408L7	μA0802B	
MC1408L8	μA0802A	
MC1410G		μA733HC
MC1411	9665	
MC1412	9666	
MC1413	9667	
MC1414L		μA711DC
MC1414P		μA711PC
MC1416	9668	
MC1420G		μA733HC
MC1435G		μA749DHC
MC1435L		μA749DC
MC1437L		μA749DC
MC1437P		μA749PC
MC1438R		μA791KC
MC14443		μA9708
MC14447		μA9708
MC1456CG		μA776HC
MC1456CL		μA776DC
MC1456G		μA776HC
MC1456L		μA776DC
MC1458CG	μA1458CHC	
MC1458CP1	μA1458CTC	
MC1458G	μA1458HC	
MC1458P1	μA1458TC	
MC1496G	μA796HC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MC1496P	μA796PC	
MC1508L8	μA0802	
MC1510F		μA733FM
MC1510G		μA733HM
MC1514F		μA711FM
MC1514L		μA711DM
MC1520G		μA733HM
MC1535G		μA749HM
MC1535L		μA749DM
MC1537L		μA749DM
MC1550G		μA757DC
MC1556G		μA776HM
MC1556L		μA776DM
MC1558G	μA1558HM	
MC1560G		μA78M00HM
MC1560R		μA7800KM
MC1561G		μA78MGHM
MC1561R		μA78MGHM
MC1563G		μA79MGHM
MC1563R		μA79MGHM
MC1569G		μA78MGHM
MC1569R		μA78GKM
MC1590		μA757DC
MC1596G	μA796HM	
MC1709CG	μA709HC	
MC1709CL	μA709DC	
MC1709CP1	μA709TC	
MC1709CP2	μA709PC	
MC1709F	μA709FM	
MC1709G	μA709HM	
MC1709L	μA709DM	
MC1710CG	μA710HC	
MC1710CL	μA710DC	
MC1710CP	μA710PC	
MC1710F	μA710FM	
MC1710G	μA710HM	
MC1710L	μA710DM	
MC1711CG	μA711HC	
MC1711CL	μA711DC	
MC1711CP	μA711PC	
MC1711F	μA711FM	
MC1711G	μA711HM	
MC1711L	μA711DM	
MC1712CG	μA702HC	
MC1712CL	μA702DC	
MC1712F	μA702FM	
MC1712L	μA702DM	
MC1723CG	μA723HC	
MC1723CL	μA723DC	
MC1723G	μA723HM	
MC1723L	μA723DM	
MC1741CG	μA741HC	
MC1741CG	μA747HC	
MC1741CL	μA741DC	
MC1741CP1	μA741TC	
MC1741CP2	μA741PC	
MC1741F	μA741FM	
MC1741G	μA741HM	
MC1741L	μA741DM	
MC1747CL	μA747DC	
MC1747G	μA747HM	
MC1747L	μA747DM	
MC1748CG	μA748HC	
MC1748CP1	μA748TC	
MC1748G	μA748HM	
MC1776CG	μA776HC	
MC1776G	μA776HM	
MC3245	9645/3345	
MC3301P	μA3301PC	
MC3302P	μA3302PC	
MC3360		μA7307
MC3401P	μA3401PC	
MC3403L	μA3403DC	
MC3403P	μA3403PC	
MC3425		μA7390TC
MC3430		75107APC
MC3433		75108APC
MC3440		9642DC
MC3441		9642DC
MC3443		9642DC
MC3448A	μA3448A	
MC3456	μA556PC	
MC3476	μA776PC	
MC3486		9637A
MC3487		9634
MC3503L	μA3503DM	
MC75107L	75107ADC	
MC75107P	75107APC	
MC75108L	75108ADC	
MC75108P	75108APC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MC75109L	75109DC	
MC75109P	75109PC	
MC75110L	75110ADC	
MC75110PC	75110APC	
MC75207L	75207DC	
MC75207P	75207PC	
MC75208L	75208DC	
MC75208P	75208PC	
MC7524L	75S24	
MC7524P	75S24	
MC7528L	7528DC	
MC7528P	7528PC	
MC75325L	75325DC	
MC75325P	75325PC	
MC7534L	755234DC	
MC7534P	755234DC	
MC75365		9645PC
MC75450L	75450BDC	
MC75450P	75450BPC	
MC75451P	75451BTC	
MC75452P	75452BTC	
MC75453P	75453BTC	
MC75454P	75454BTC	
MC75491P	75491PC	
MC75492P	75492PC	
MC7705CP		μA78M05UC
MC7706CP		μA78M06UC
MC7708CP		μA78M08UC
MC7712CP		μA78M12UC
MC7715CP		μA78M15UC
MC7718CP		μA7818UC
MC7720CP		μA78M20UC
MC7724CP		μA78M24UC
MC7805CK	μA7805KC	
MC7805CP	μA7805UC	
MC7806CK	μA7806KC	
MC7806CP	μA7806UC	
MC7808CK	μA7808KC	
MC7808CP	μA7808UC	
MC7812CK	μA7812KC	
MC7812CP	μA7812UC	
MC7815CK	μA7815KC	
MC7815CP	μA7812UC	
MC7818CK	μA7812KC	
MC7818CP	μA7812UC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MC7824CK	μA7824KC	
MC7824CP	μA7824UC	
MC7905CK	μA7905KC	
MC7905CP	μA7905UC	
MC7906CK	μA7906KC	
MC7906CP	μA7906UC	
MC7908CK	μA7908KC	
MC7908CP	μA7908UC	
MC7912CK	μA7912KC	
MC7912CP	μA7912UC	
MC7915CK	μA7915KC	
MC7915CP	μA7915UC	
MC7918CK	μA7918KC	
MC7918CP	μA7918UC	
MC7924CK	μA7924KC	
MC7924CP	μA7924UC	
MC8T13L	μA8T13DM	
MC8T13P	μA8T13PC	
MC8T14L	μA8T14DM	
MC8T23P	μA8T23PC	
MC8T24P	μA8T24PC	
MC8T26A	μA8T26A	
MFC4060A		μA78MGT2C
MFC4062A		μA78MGT2C
MFC4063A		μA78MGT2C
MFC4064A		μA78MGT2C
MFC6030A		μA78MGT2C
MFC6032A		μA78MGT2C
MFC6033A		μA78MGT2C
MFC6034A		μA78MGT2C
MFC8000		μA739PC
MFC8001		μA739PC
MFC8002		μA739PC
MFC8030		μA703HC
MFC8070		μA742DC
MLM101AG	μA101AHM	
MLM104G	μA104HM	
MLM105G	μA105HM	
MLM107G	μA107HM	
MLM109G		μA78M05HM
MLM109K		μA109KM
MLM110G	μA110HM	
MLM201AG	μA201AHM	
MLM204G	μA204HM	
MLM205G	μA205HM	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MLM207G	μA207HM	
MLM209G		μA78M05HM
MLM209K	μA209KM	μA7805KM
MLM210G	μA210HM	
MLM301AG	μA301AHC	
MLM301AP1	μA301ATC	
MLM304G	μA304HC	
MLM305G	μA305HC	
MLM307G	μA307HC	
MLM309G		μA78M05HC
MLM309K	μA309KC	
MLM310G	μA310HC	
MLM311G	μA311HC***	
MLM311P1	μA311TC***	
ML1408-6L	μA0802CDC	
ML1408-7L	μA0802BDC	
ML1408-8L	μA0802ADC	
ML1508-8L	μA0802DM	
MMH0026	9646/0026	
NE515A	μA733PC	
NE515K		μA733HC
NE521A		75107APC
NE521F		75107ADC
NE522A		75108APC
NE522F		75108ADC
NE526A		μA760DC
NE526K		μA760HC
NE527K		μA760HC
NE529K		μA760HC
NE536T	μA740HC	μA740HC
NE545		μA7300
NE550A		μA723PC
NE550L		μA723HC
NE555V	μA555TC	
NE556A	μA556PC	
NE556F	μA556DC	
NE592A		μA733PC
NE645		μA7300
N10145	10145A	
N10149	10146	
N5071A	μA781PC	
N5072A	μA746PC	
N5558T	μA1458HC	
N5558V	μA1458TC	
N5570B	μA780PC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
N8T13B	8T13PC	
N8T13F	8T13DC	
N8T14B	8T14PC	
N8T14F	8T14DC	
N8T15F		9616DC
N8T16F		9627DC
N8T23B	8T23PC	
N8T23F	8T23DC	
N8T24B	8T24PC	
N8T24F	8T24DC	
N8T26A	μA8T26A	
OP-02		μA741AHM
OP-04		μA741AHM
OP-05		μA714HC
OP-07	μA714HC	
PA239A		μA739PC
RC1488D	μA1488	9616DC
RC1489AD	μA1489A	9617DC
RC1489D	μA1489	9617DC
RC4136D	μA4136DC/DM	
RC4136DB	μA4136PC	
RC4136DP	μA4136PC	
RC4151	μA4151	μA7151
RC4152		μA7151
RC4558DN	μA4558TC	
RC4558T	μA4558HC	
RC55109D	55109DM	
RC555DN	μA555TC	
RC556D	μA556DC	
RC556DP	μA556PC	
RC733TF	μA733HC	
RC75107AD	75107ADC	
RC75107AP	75107APC	
RC75108AD	75108ADC	
RC75108ADP	75108APC	
RC75109D	75109DC	
RC75109DP	75109PC	
RC75110D	75110ADC	
RC75150D	75150DC	
RC75154M	75154DC	
RC7524M	75S24DC	
RC7524MP	75S24PC	
RC7528M	7528DC	
RC7528MP	7528PC	
RC75325M	75325DC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
RC75325MP	75325PC	
RC8T13M	μA8T13DC	
RC8T13MP	μA8T13PC	
RC8T14M	μA8T14DC	
RC8T14MP	μA8T14PC	
RC8T23M	μA8T23DC	
RC8T23MP	μA8T23PC	
RC8T24M	μA8T24DC	
RC8T24MP	μA8T24PC	
RC9621D	9621DC	
RC9622D	9622DC	
RM4136D	μA4136DM	
RM55107AD	55107ADM	
RM55108AD	55108ADM	
RM55110D	55110DM	
RM5524M	5524DM	
RM5525M	5525DM	
RM55325M	55325DM	
RM555T	μA555HM	
RM556D	μA556DM	
RM733TF	μA733HM	
RM8T13M	μA8T13DM	
RM8T14M	μA8T14DM	
SE515K		μA733HM
SE526A		μA760DM
SE526K		μA760HM
SE527K		μA760HM
SE529A		μA733DM
SE529K		μA760HM
SE536T		μA740HM
SE550L		μA723HM
SE592K		μA733HM
SH76008		TDAA2002
SH76018		TDA2002
SN2660JA		μA776DM
SN52L022L		μA798HM
SN52L044JA		μA3503DM
SN52309LA		μA78M05HM
SN52506J		μA711DM
SN52510L		μA710HM
SN52514J		μA711DM
SN52520J		μA710DM
SN52558L	μA1558HM	
SN52660L		μA776HM
SN52702J	μA702DM	
SN52702L	μA702HM	
SN52709J	μA709DM	
SN52709L	μA709HM	
SN52710J	μA710DM	
SN52710L	μA710HM	
SN52711J	μA711DM	
SN52711L	μA711HM	
SN52723J	μA723DM	
SN52723L	μA723HM	
SN52741J	μA741DM	
SN52741L	μA741HM	
SN52747J	μA747DM	
SN52747L	μA747HM	
SN52748J	μA748DM	
SN52748L	μA748HM	
SN52771J		μA776DM
SN52771L		μA776HM
SN52777J	μA777DM	
SN52777L	μA777HM	
SN52810J		μA710DM
SN52810L		μA710HM
SN52811J		μA711DM
SN52811L		μA711HM
SN52820J		μA711DM
SN529K		μA733HC
SN5510FA		μA833FM
SN5510L		μA733HM
SN55107AL	55107ADM	
SN55107BJ	55107BDM	
SN55108AJ	55108ADM	
SN551088J	55108BDM	
SN55109J	55109DM	
SN5511FA		μA733FM
SN5511L		μA733HM
SN55110J	55110ADM	
SN55112J	55112DM	
SN55114J	9614DM	
SN55114SB	9614FM	
SN55115J	9615DM	
SN55115SB	9615FM	
SN5512L		μA733HM
SN55121J	55121DM	
SN55122J	55122DM	
SN55123J	55123DM	
SN55124J	55124DM	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN5514L		μA733HM
SN55207J	55207DM	
SN55208J	55208DM	
SN55234J	55S234DM	
SN5524J	55S24DM	
SN55325J	55325DM	
SN55325SB	55325FM	
SN55326SB	55326FM	
SN55327SB	55327FM*	
SN55450BJ	55450BDM	
SN55450J	55450DM	
SN55451BL	55451BHM	
SN55451L	55451HM	
SN55452BL	55452BHM	
SN55452L	55452HM	
SN55453BL	55453BHM	
SN55453L	55453HM	
SN55454BL	55454BHM	
SN55454L	55454HM	
SN55460J	55460DM	
SN55461L	55461HM	
SN55462L	55462HM	
SN55463L	55463HM	
SN55464L	55464HM	
SN71710J	μA710DC	
SN72L022L		μA798HC
SN72L022P		μA798TC
SN72L044JA		μA3403DC
SN72L044N		μA3403PC
SN72301AN	μA301ADC	
SN72301L	μA301AHC	
SN72301P	μA301ATC	
SN72304L	μA104HM	
SN72305AL	μA305AHC	
SN72305L	μA305HC	
SN72307L	μA307HC	
SN72307P	μA307TC	
SN72308AL	μA308AHC	
SN72308AN	μA308ADC	
SN72308L	μA308HC	
SN72308N	μA308DC	
SN72309LA		μA78M05HC
SN72310L	μA310HC	
SN72311L	μA311HC	
SN72311P	μA311TC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN72376P	μA376TC	
SN72440J		μA742DC
SN72440N		μA742DC
SN72506J		μA711DC
SN72506N		μA711PC
SN72510J		μA710DC
SN72510L		μA710HC
SN72510N		μA710PC
SN72514J		μA711DC
SN72514N		μA711PC
SN72555P	μA555TC	
SN72556N	μA556PC	
SN72558L	μA1458HC	
SN72558P	μA1458TC	
SN72660JA		μA776DC
SN72660L		μA776HC
SN72660N		μA776DC
SN72660P		μA776TC
SN72702J	μA702DC	
SN72702L	μ702HC	
SN72709J	μA709DC	
SN72709L	μA709HC	
SN72709P	μA709TC	
SN72710L	μA710HC	
SN72710N	μA710PC	
SN72711J	μA711DC	
SN72711L	μA711HC	
SN72711N	μA711PC	
SN72720J		μA710DC
SN72720N		μA710PC
SN72723J	μA723DC	
SN72723L	μA723HC	
SN72723N	μA723PC	
SN72733J	μA733DC	
SN72733L	μA733HC	
SN72733N	μA733PC	
SN72741J	μA741DC	
SN72741L	μA741HC	
SN72741N	μA741PC	
SN72741P	μA741TC	
SN72747J	μA747DC	
SN72747L	μA747HC	
SN72748J	μA748DC	
SN72748L	μA748HC	
SN72748N	μA748DC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN72748P	μA748TC	
SN72771J		μA776DC
SN72771L		μA776HC
SN72771N		μA776DC
SN72771P		μA776TC
SN72777J	μA777DC	
SN72777L	μA777HC	
SH72777N	μA777DC	
SN72777P	μA777TC	
SN72810J		μA710DC
SN72810L		μA710HC
SN72810N		μA710PC
SN72811J		μA711DC
SN72811L		μA711HC
SN72811N		μA711PC
SN72820J		μA711DC
SN72820N		μA711PC
SN7496	7496	
SN7497	7497	
SN7510L		μA733HC
SN75107AJ	75107ADC	
SN75107AN	75107APC	
SN75107BJ	75107BDC	
SN75107BN	75107BPC	
SN75108AJ	75108ADC	
SN75108AN	75108APC	
SN75108BJ	75108BDC	
SN75108BN	75108BPC	
SN75109J	75109DC	
SN75109N	75109PC	
SN7511L		μA733HC
SN7511N		μA733PC
SN75110AJ	75110ADC	
SN75110AJ	75110APC	
SN75110J	75110ADC	
SN75110N	75110APC	
SN75112J	75112DC	
SN75112N	75112PC	
SN75114J	9614DC	
SN75114N	9614PC	
SN75115J	9615DC	
SN75115N	9615PC	
SN7512L		μA733HC
SN7512N		μA733PC
SN75121J	75121DC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN75121N	75121PC	
SN75122J	75122DC	
SN75122N	75122PC	
SN75123J	75123DC	
SN75123N	75123PC	
SN75124J	75124DC	
SN75124N	75124PC	
SN75124L		μA733HC
SN7514P		μA733PC
SN75150J	75150DC	9616DC
SN75150P	75150PC	9616DC
SN75152J	9627DC	
SN75154J	75154DC	9617DC
SN75182N		9615DC
SN75183N		9614DC
SN75188J	1488DC	
SN75189AJ	1489ADC	
SN75189J	1489DC	
SN7520	75S20	
SN75207J	75207DC	
SN75207N	75207PC	
SN75208J	75208DC	
SN75208N	75208PC	
SN75224J	75S24DC	
SN75224N	75S24PC	
SN75225J	75225DC	
SN75225N	75225PC	
SN75232J	75232DC	
SN75232N	75232PC	
SN75234J	75S234DC	
SN75234N	75S234PC	
SN75235J	75235DC	
SN75235N	75235PC	
SN75238J	75238DC	
SN75238N	75238PC	
SN7524J	75S24DC	
SN7524N	75S24PC	
SN7528J	7528DC	
SN7528N	7528PC	
SN75325J	75325DC	
SN75325N	75325PC	
SN75326J	75326DC*	
SN75236N	75326PC*	
SN75327J	75327DC	
SN75327N	75327PC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN7534J	75S234DC	
SN7534N	75S234PC	
SN75450BJ	75450BDC	
SN75450BN	75450BPC	
SN75450N	75450BPC	
SN75451BL	75451BHC	
SN75451BP	75451BTC	
SN75451P	75451BTC	
SN75452BL	75452BHC	
SN75452BP	75452BTC	
SN75452P	75452BTC	
SN75453BL	75453BHC	
SN75453BP	75453BTC	
SN75453P	75453BTC	
SN75454BL	75454BHC	
SN75454P	75454BTC	
SN75460J	75460DC	
SN75460N	75460PC	
SN75461L	75461HM	
SN75461L	75462HM	
SN75461P	75461TC	
SN75463P	75463TC	
SN75464L	75464HM	
SN75464P	75464TC	
SN75471L	75471HC	
SN75471P	75471TC	
SN75472L	75472HC	
SN75472P	75472TC	
SN75473L	75473HC	
SN75473P	75473TC	
SN75474L	75474HC	
SN75474P	75474TC	
SN75491N	75491PC	
SN75492N	75492PC	
SN76001N	TBA641A12	
SN76005ND		μA706BPC
SN76024ND		μA706BPC
SN76104N	μA732PC	
SN76105N		μA732PC
SN76111N	μA767PC	
SN76115	μA1310	
SN76116N	μA758PC	
SN76131N	μA739PC	
SN76149N	μA749PC	
SN76227		TDA2522
SN76242N	μA780PC	
SN76243N	μA781PC	
SN76246N	μA746PC	
SN76298N		μA787PC
SN76545		TBA920
SN76565N	μA3064PC	
SN76591P	μA1391TC	
SN76594P	μA1394TC	
SN76600P		μA757PC
SN76635N	μA720PC	
SN76642N		μA2136PC
SN76650N		μA757PC
SN76666N	μA3065PC	
SN76669N	μA2136PC	
SN76675N	μA3075PC	
SN76678P	μA753TC	
SN76689N	μA3089PC	
SSS725AJ		μA725AHM
SSS725BJ		μA725EHM
SSS725EJ		μA725EHC
SSS741CJ		μA741EHC
SSS741J		μA741AHM
SSS747CK		μA747EHC
SSS747CP		μA747EDC
SSS747K		μA747AHM
SSS747P		μA747ADM
SSS1408A-6	μA0802C	
SSS1408A-7	μA0802B	
SSS1408A-8	μA0802A	
SSS1508A-8	μA0802	
S5558T	μA1558HM	
S5596K	μA796H	
S8T13F	μA8T13DM	
S8T14F	μA8T14DM	
S8T15F		9616DM
S8T16F		9627DM
TA7157	μA1310	
TAA630S	TAA630S	TDA2522
TBA396		TDA2560
TBA510	TBA510	
TBA520	TBA520	TDA2522
TBA530	TBA530	TDA2530
TBA540	TBA540	
TBA560C	TBA560C	TDA2560
TBA570		μA721PC

LINEAR INDUSTRY CROSS REFERENCE GUIDE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
TBA641A12	TBA641A12	
TBA641B11	TBA641B11	
TBA800	TBA800	
TBA810AS	TBA810AS	
TBA810DS	TBA810DS	
TBA810DAS	TBA810DAS	
TBA810S	TBA810S	
TBA920	TBA920	
TBA920S	TBA920S	
TBA970	TBA970	
TBA990	TBA990	TDA2522
TCA600		μA7392
TCA610		μA7392
TCA900		μA7392
TCA910		μA7392
TCA940		μA783P4C
TDA1170	TDA1170	
TDA1270	TDA1270	
TDA1037		TDA2002
TDA1190	TDA1190	
TDA1190Z	TDA1190Z	
TDA1327		TDA2522
TDA2002	TDA2002	
TDA2002A	TDA2002A	
TDA2150		TDA2560
TDA2160		TDA2522
TDA2521	TDA2521	
TDA2522	TDA2522	
TDA2530	TDA2530	
TDA2560	TDA2560	
TDA2590	TDA2590	
TDA2610		TDA1190
TL081		μAF771C
TL081A		μAF771
TL810		μA710HM
TL811		μA711HM
U2001A	9665	
ULN2002A	9666	
ULN2003A	9667	
ULN2004A	9668	
ULN2111A		μA2136PC
ULN2113A		μA3065PC
ULN2114A	μA746PC	
ULN2114K	μA746HC	
ULN2120A	μA732PC	

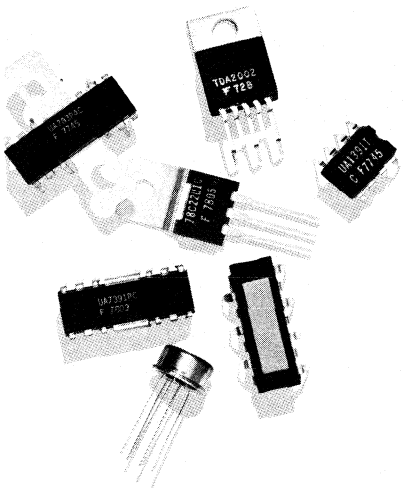
Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
ULN2121A		μA767PC
ULN2122A		μA732PC
ULN2124A	μA780PC	
ULN2126A	μA739PC	
ULN2127A	μA781PC	
ULN2128A	μA767PC	
ULN2129A		μA3075PC
ULN2136A	μA2136PC	
ULN2137A	μA720PC	
ULN2165A	μA3065PC	
ULN2209M	μA753TC	
ULN2210A		μA758PC
ULN2224A		μA788PC
ULN2228A		μA788PC
ULN2244A	μA758PC	
ULN2298A		μA787PC
ULX2262A	μA787PC	
ULX2264A	μA3064PC	
ULX2267A	μA3067PC	
ULX2289A	μA3089PC	
YKB2219	μA1310	
μA709CA	μA709PC	
μA709CT	μA709HC	
μA709Q	μA709FM	
μA709T	μA709HM	
μA710CA	μA710HC	
μA710CT	μA710HC	
μA710Q	μA710FM	
μA710T	μA710HM	
μA711CA	μA711PC	
μA711CK	μA711HC	
μA711K	μA711HM	
μA723CA	μA723PC	
μA723CL	μA723HC	
μA723L	μA723HM	
μA733A	μA733DM	
μA733CK	μA733HC	
μA733C1	μA733DC	
μA733K	μA733HM	
μA7330A	μA733PC	
μA7331	μA733DM	
μA740CT	μA740HC	
μA741CA	μA741PC	
μA741CT	μA741HC	
μA741CV	μA741TC	

LINEAR INDUSTRY CROSS REFERENCE GUIDE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
μA741T	μA741HM	
μA747CA	μA747PC	
μA747CK	μA747HC	
μA747K	μA747HM	
μA748CA	μA748DC	
μA748CT	μA748HC	
μA748CV	μA748TC	
μA748T	μA748HC	
μA78L02ACLP	μA78L26AWC	
μA78L05ACLP	μA78L05AWC	
μA78L06ACLP	μA78L62AWC	
μA78L08ACLP	μA78L08AWC	
μA78L12ACLP	μA78L12AWC	
μA78L15ACLP	μA78L15AWC	
μA78M05CKC	μA78M05UC	
μA78M05CLA	μA78M05CHC	
μA78M05MLA	μA78M05HM	
μA78M06CKC	μA78M06UC	
μA78M06CLA	μA78M06CHC	
μA78M06MLA	μA78M06HM	
μA78M08CKC	μA78M08UC	
μA78M08CLA	μA78M08CHC	
μA78M08MLA	μA78M08HM	
μA78M12CKC	μA78M12UC	
μA78M12CLA	μA78M12CHC	
μA78M12MLA	μA78M12HM	
μA78M15CKC	μA78M15UC	
μA78M15CLA	μA78M15CHC	
μA78M15MLA	μA78M15HM	
μA78M20CKC	μA78M20CUC	
μA78M20CLA	μA78M20CHC	
μA78M20MLA	μA78M20HM	
μA78M24CKC	μA78M24CUC	
μA78M24CLA	μA78M24CHC	
μA78M24MLA	μA78M24HM	
μA7805CKA	μA7805KC	
μA7805CKC	μA7805UC	
μA7805MKA	μA7805KM	
μA7806CKA	μA7806KC	
μA7806CKC	μA7806UC	
μA7806MKA	μA7806KM	
μA7808CKA	μA7808KC	
μA7808CKC	μA7808UC	
μA7808MKA	μA7808KM	
μA7812CKA	μA7812KC	
μA7812CKC	μA7812UC	
μA7812MKA	μA7812KM	
μA7815CKA	μA7815KC	
μA7815CKC	μA7815UC	
μA7815MKA	μA7815KM	
μA7818CKC	μA7818UC	
μA7818MKA	μA7818KM	
μA7824CKC	μA7824UC	
μA7824MKA	μA7824KM	
μA7885CKA	μA7885KC	
μA7885CKC	μA7885UC	
μA7885MKA	μA7885KM	
μA79M05CKC	μA79M05AUC	
μA79M05CLA	μA79M05AHC	
μA79M05MLA	μA79M05HM	
μA79M06CKC	μA79M06AUC	
μA79M06CLA	μA79M06AHC	
μA79M06MLA	μA79M06HM	
μA79M08CKC	μA79M08AUC	
μA79M08CLA	μA79M08AHC	
μA79M08MLA	μA79M08HM	
μA79M12CKC	μA79M12AUC	
μA79M12CLA	μA79M12AHC	
μA79M12MLA	μA79M12HM	
μA79M15CLA	μA79M15AHC	
μA79M15MLA	μA79M15HM	
μA79M20CKC	μA79M20AUC	
μA79M20CLA	μA79M20AHC	
μA79M20MLA	μA79M20HM	
μA79M24CKC	μA79M24AUC	
μA79M24CLA	μA79M24AHC	
μA79M24MLA	μA79M24HM	
μA7905CKA	μA7905KC	
μA7905CKC	μA7905UC	
μA7905MKA	μA7905KM	
μA7906CKA	μA7906KC	
μA7906CKC	μA7906UC	
μA7906MKA	μA7906KM	
μA7908CKA	μA7908KC	
μA7908CKC	μA7908UC	
μA7908MKA	μA7908KM	
μA7912CKA	μA7912KC	
μA7912CKC	μA7912UC	
μA7912MKA	μA7912KM	
μA7915CKA	μA7915KC	

LINEAR INDUSTRY CROSS REFERENCE GUIDE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
μA7915CKC	μA7915UC	
μA7915MKA	μA7915KM	
μA7918CKA	μA7918KC	
μA7918CKC	μA7918UC	
μA7918MKA	μA7918KM	
μA7924CKA	μA7924KC	
μA7924CKC	μA7924UC	
μA7924MKA	μA7924KM	



QUALITY, RELIABILITY AND HI REL PROCESSING

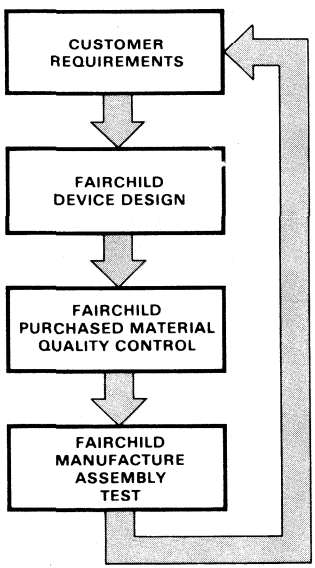
Introduction

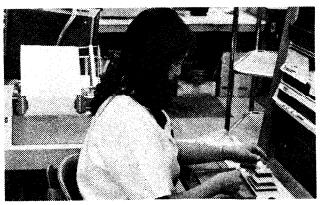
There are three basic ingredients in the manufacture of reliable Linear Circuits. First, the device must be designed with the user's applications and reliability requirements in mind. Secondly, the device must be manufactured with the optimum technology for the application. Thirdly, controls must be established to assure maintenance of the quality/reliability levels established in the design of the device. Consideration is given to the reliability influence of each part of the manufacturing and testing cycle with constant feedback from internal reliability monitoring; customer feedback on the results is a vital factor. The Fairchild reliability concept can be presented as constant feedback system which begins and ends with the customer *(Figure 2-1)*.

Areas of Consideration

Device Applications and Reliability

The reliability cycle begins with the customer. His device application, environment for its usage and end-product reliability requirements are major factors in establishing the quality/reliability levels. The customer is the final judge.





Customer Design Breadboard

Fig. 2-1 Customer Feedback System

Device Design

Inherent component reliability is a function of the product/process design. New Fairchild designs as well as modifications or extensions of existing designs with known performance and reliability characteristics are rigorously evaluated. Three different factors in the manufacture of an IC significantly affect its reliability.

The Silicon Chip — Fairchild's design-technology capability utilizes epitaxial layer to achieve the desired electrical parameter characteristics. The surface influences long-term gain and voltage/leakage stability. The metallization determines mechanical integrity and current distribution.

Chip Assembly — The process and materials used to assemble the chip and package must preserve the inherent reliability of the chip and be inherently reliable to withstand thermal, mechanical and electrical stresses.

The Package — The package must effectively transfer heat from the chip to the outside world and protect the chip during handling and use.

Incoming Quality Control (IQC)

All purchased materials for Fairchild Linear circuits are controlled through central specification control, product engineering, and reliability and quality assurance (R&QA) located in Mountain View. Materials are purchased and inspected per control documents using three IQC methods.

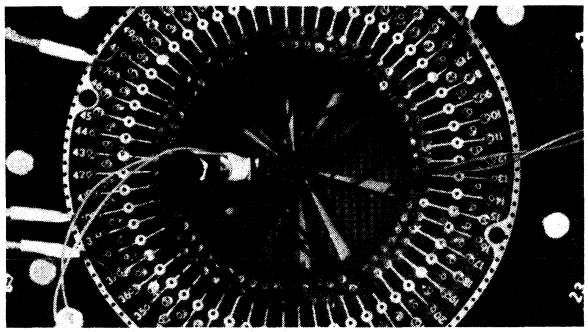
Direct visual and mechanical inspection
Functional testing
Composition analysis utilizing chemical and x-ray techniques from both internal and external sources.

In addition to centralized IQC, each manufacturing facility has a local, fully equipped IQC department. These facilities concentrate on cleanliness, plating quality and functionality. A computer file is made on each vendor's performance and quarterly reports are generated and analyzed.

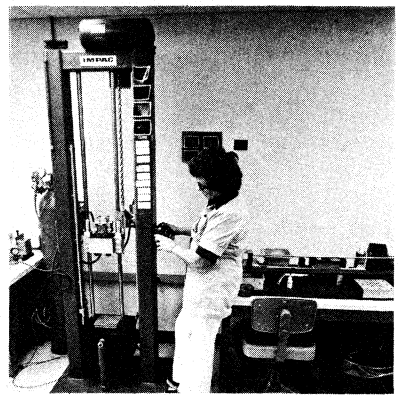
Wafer Manufacture

Wafers used to fabricate Fairchild Linear Circuits are made at Fairchild. This includes crystal pulling, slicing, polishing and epitaxial layer growth. Fairchild designs rely on accurate control of thickness and resistivity. All critical operations have laminar-flow clean-air hoods directly over the work areas. Wafer fabrication is essentially a series of masking and furnace cycles in which geometries are defined and impurities (dopants) introduced to form emitter, base and resistor regions. Daily controls are maintained on furnace temperatures to within $\pm 1°$ C. Resistivities (ρ_S) of diffused layers are recorded on every run. Each masking step defines a new portion of the device geometry. A post develop inspection is performed to assure that each wafer has been properly exposed and chemically developed before final etching. When the masking and etching procedures are completed, a final inspection assures that the geometry is properly aligned, etched and cleaned. Following each production masking step, a sample inspection is performed by quality control inspectors to verify correct process implementation.

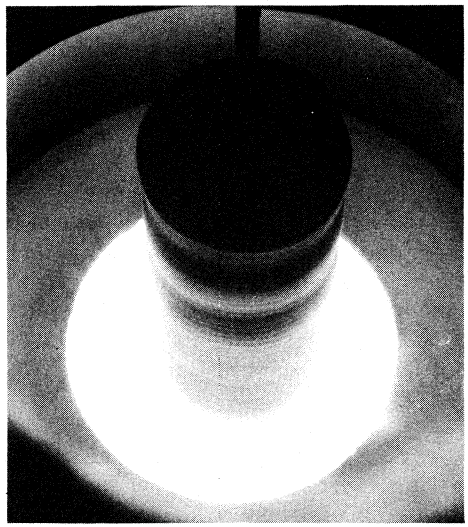
After masking and diffusion, the metallization process completes wafer manufacture. Fairchild uses electron-beam evaporation techniques to deposit gold and aluminum. Deposits are controlled through utilization of automated process sequencing,which includes an automatic thickness controller. Every run is gated through a first optical (1st opt.) inspection before it leaves the wafer fabrication area. Cleanliness, mask alignment, metal adherence (front and back) and general workmanship are inspected.



Wafer Probing



IQC Area



Crystal Puller

Wafer Testing
Before the wafers are scribed and broken into dice for assembly onto headers or shipment to a customer as probed dice, they are electrically sorted. Each wafer is automatically probed with multiple tests to duplicate or correlate the dice to the final product test requirements. Rejected dice are ink marked and later scrapped. A final quality control gate is performed before the probed wafers can be forwarded to assembly.

Device Assembly
After the wafers are scribed and broken, a second optical (2nd opt.) QC inspection is performed. The dice are inspected for wafer fabrication (handling) damage, as well as for defects which may cause assembly problems or result in latent reliability problems.

Monitors are performed on both assembly equipment and operators. Machines are shut down if defect control limits are exceeded and suspect material is rejected and 100% screened. Key items inspected are die orientation, voids under die, proper bond formation, wirepull strength and cleanliness.

A third optical (3rd opt.) gate is performed prior to final device sealing. If rejected, the lot is 100% screened by production and resubmitted to QC. Accepted lots are sent to the final seal operation, where the packages are monitored for weld strength and hermeticity (except plastic packages).

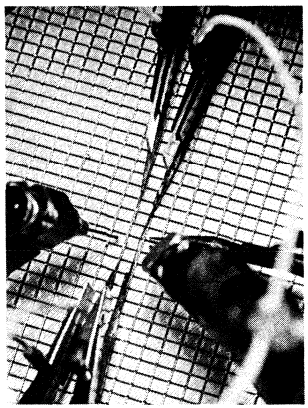
Device Testing
Before shipment, all devices are 100% production tested to the following minimum inspection levels.

Functional dc	0.25% AQL	
25° C dc	0.65% AQL	
25° C ac	1.5% AQL	
Temperature dc	1.5% AQL	
Mechanical/Visual	0.65% AQL	
Marking Performance	15/0 LTPD	
Fine Leak	1.0% AQL	Hermetic Devices Only.
Gross Leak	0.4% AQL	

Customers with special testing requirements are accommodated through an internal specification system. All internal test specifications formatted from customer documents are signed off by QA before they can be issued to the test area.

Device Application
The total reliability effort is completed full-cycle with the customer. Operation in the customer application is the final consideration in device reliability. How each device is handled during system assembly by the customer, heat-sunk (mounted) and cooled during operation, and the amount of overload stresses (due to the system malfunction or misuse) greatly impacts the device reliability. Thus, the customer's specification requirements, the manufacturer's device design, manufacture, test, the actual circuit into which the device is inserted and the equipment containing that circuit in the field all affect the device and reliability.

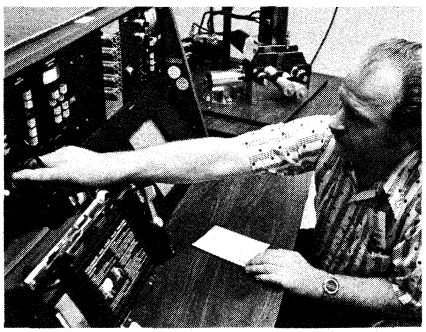
Failure Analysis
Failure analysis results performed by customers and by Fairchild on returned devices provide one of the most important inputs for consideration in Fairchild's total linear reliability concept. Failures generated by line monitors, life tests and field applications are analyzed to provide corrective action in terms of product design, assembly and testing methods. A scanning electron microscope (SEM) and an Auger electron microscope for chemical analysis are available for inspection of materials.

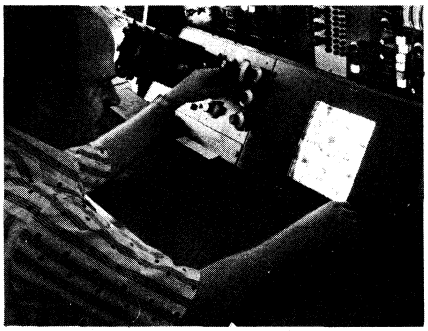


Die Probing

Device Testing

IQC Sign-off





Failure Analysis

Reliability Monitor and Control

Line Monitors

Line monitors are used to monitor the production line on a weekly basis. These monitors are designed to provide a constant feedback on product reliability. The following assembly/test monitors are conducted on a routine basis.

Assembly	Test
Package integrity	High-temperature reverse bias
Lead integrity	Intermittent operating life (power cycling)
Die integrity	High-temperature storage
Die-attach integrity	Temperature cycling
Bond integrity	Thermal shock
	Autoclave*
	85% R.H./85° C biased*

*Applied to plastic devices only.

Extended Reliability Tests

In conjunction with the weekly line-monitor program, Fairchild employs an extended reliability test program which is designed to reflect the long-term stability of Fairchild's Linear products. A summary of these reliability tests is shown in *Table 2-1.*

Quality and Reliability Data

Supplemental brochures are published on an annual basis which provide detailed failure rate data. Please contact Fairchild Sales Offices for additional reliability and quality information.

EXTENDED RELIABILITY TESTS	METAL CAN	PLASTIC
High Temperature Operating Life T_A = 150° C Readouts at 0, 168, 500, 1000 Hours	X	X
Temperature Cycling -65° C to +150° C (MIL-STD-883, Method 1010.1, Cond. C) Readouts at 0, 10, 100 Cycles Hermeticity (1×10^{-7} - TO-5, 1×10^{-6} - TO-3)	X	
Constant Acceleration F = 20K g 1 Min. Ea. 6 Axis (MIL-STD-883, Method 2001)	X	
Impact Shock 1500 g x 5 Blows (MIL-STD-883, Method 2002)	X	
Vibration, Variable Frequency 10 g (MIL-STD-883, Method 2007)	X	
Biased Humidity T_A = 85° C, RH = 85% Readouts at 0, 168, 500, 1000 Hours		X
Thermal Shock -55° C to +125° C Readouts at 0, 10, 100 Cycles MIL-STD-883, Method 1011, Condition C	X	X
Autoclave T_A = 125° C ± 2° C 15 Psi, 24 Hours		X

Table 2-1 Reliability Test Summary

HI REL PROCESSING — MIL-M-38510/MIL STD-883

A unique "company", within Fairchild Linear, is totally dedicated to the processing of high reliability products and to serving the special needs of the HI REL community. It consists of marketing, engineering, production control, manufacturing and quality assurance. Fairchild's HI REL processing facilities are among the most modern and sophisticated in the semiconductor industry. Screening procedures are set up to conform to the most recent version of MIL-STD-883, in conjunction with MIL-M-38510, which establishes standardized requirements for design, material, performance, control and documentation needed to achieve prescribed levels of device quality and reliability.

HI REL Unique II Program

Fairchild's Unique II program fills a longstanding need for a definite and comprehensive program covering HI REL semiconductor products...a program offering users a selection among multi-level screening flows and reliability requirements...a program providing clear and precise definitions on all areas of contractual performance...a program designed to reduce the high costs and delivery delays normally associated with HI REL. The objectives and benefits of the Unique II program for integrated circuits are these:

- Offers a full spectrum of processing options, including full compliance JAN and 883 Classes S, B, and C.
- Offers full compliance with JAN MIL-M-38510 and emphasizes the importance of this program.
- Accommodates the special needs of users' source control and specification control drawings.
- Offers models to aid users in development of source control drawings.
- Takes the mystery out of in-house processing to MIL-STD-883 and to MIL-M-38510 detail specifications. The Unique II program is definitive as to the similarities and differences in these requirements.
- Provides users with alternatives that may be used when JAN slash sheets or QPLs are unavailable, or for programs that demand the highest level of quality and reliability.

Fairchild offers a complete processing capability to fulfill requirements ranging from the least demanding to the most complex, including the following:

- Scanning Electron Microscope (SEM) Inspection
- Level A Visual
- Bond Pull and Die Shear Testing
- Read and Record and Δ Drift Parameters
- Particle Impact Noise Detection (Pin-D) Testing
- Group A, B, C and D Qualification Testing.

Standard Unique II processing flows are given on the following pages; special flows will be quoted on an individual basis.

MATRIX VI — COMMERCIAL AND INDUSTRIAL RELIABILITY PROGRAM

Commercial and industrial users increasingly demand optimized quality and reliability for the semiconductor integrated circuits purchased for their systems. Specific factors — increased integrated circuit usage per board, high costs for receiving inspection, pc board and systems repair, and the frequently immeasurable cost associated with field failures — require the user to attain high quality and reliability coupled with total cost. Matrix VI is designed to meet these user requirements.

Fairchild's Matrix VI Program offers a broad spectrum of screens and high technology/high volume integrated circuit products to meet the user's quality and reliability requirements typically associated with the commercial and industrial marketplace. There are two screening options for each package type, each with a separate degree of reliability and cost level. To simplify a cost-effective analysis, reliability factors have been assigned to each screening level. (See following pages.)

It is the goal of Matrix VI to achieve the highest possible reliability consistent with the user's needs and to avoid "over-buying". Cost-effective reliability is the essence of Matrix VI, the most comprehensive program of its kind now offered to the industrial/commercial marketplace.

JAN PART NUMBERING SYSTEM

J M 38510/ 101 01 B G C

JAN DESIGNATOR

Cannot be marked with "J" unless qualified on Part I or Part II of QLP-38510

General Procurement Spec.

REFERS TO DETAIL SPEC

101 Op Amps
102 Voltage Regulators
103 Comparators
104 Interface
105 733
106 Voltage Followers
107 3-Terminal Voltage Regulators
108 Transistor Arrays
109 Timers
110 Quad Op Amps

Defines Device Type

PROCESSING LEVEL

S
B
C

PACKAGE TYPE

A 14-pin $^1/_4$ x $^1/_4$ **Flatpak**
B 14-pin $^1/_4$ x $^1/_8$ **Flatpak**
C 14-pin $^1/_4$ x $^3/_4$ **DIP**
D 14-pin $^1/_4$ x $^3/_8$ **Flatpak**
E 16-pin $^1/_4$ x $^3/_4$ DIP
F 16-pin $^1/_4$ x $^3/_8$ Flatpak
G 8-pin Can
H 10-pin $^1/_4$ x $^1/_4$ Flatpak
I 10-pin Can
J 24-pin $^1/_2$ x $1^1/_4$ DIP
K 24-pin $^3/_8$ x $^1/_2$ Flatpak
L 24-pin $^3/_8$ x $^1/_2$ Flatpak
X 3-pin TO-5 Can
Y 2-pin TO-3 Can
Z 24-pin $^1/_4$ x $^3/_8$ Flatpak

LEAD FINISH

A Hot Solder DIP
B Tin Plate
C Gold Plate
X Any of the above

LINEAR JAN GENERIC PART NUMBERS – EXAMPLES

JM38510/	01	02	03	04	05	06	07	08	09	10
101	741	747	101A	108A	2101	2108	118			
102	723									
103	710	711	106	111	2111					
104	55107	55108	9614	9615	55113	7831	7832	7820	7830	
105	733									
106	102	110	2110							
107	109	78M05	78M12	78M15	78M24	7805	7812	7815	7824	
108	3018	3045								
109	555	556								
110	148	149	4741	4136	124					

Note: Dated material. Please contact Fairchild for latest revisions.

HI REL PROCESS SCREENING REQUIREMENTS

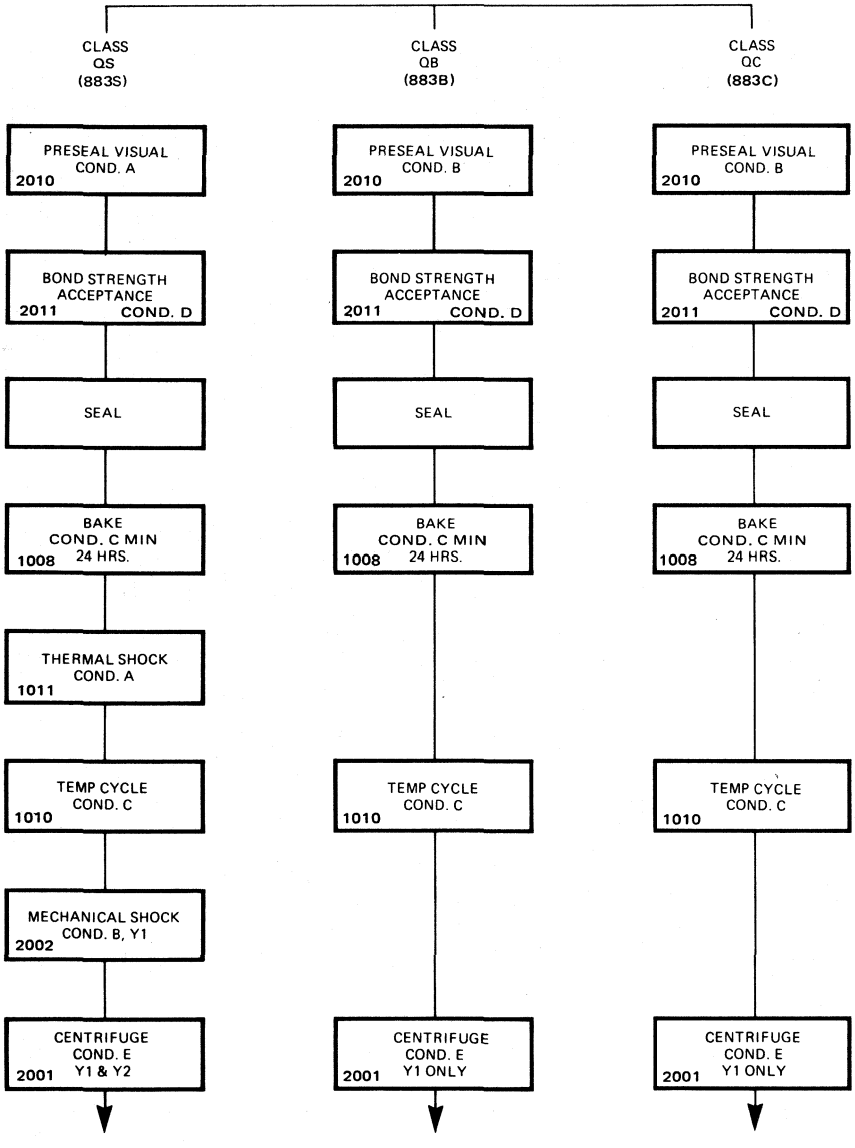
MIL-STD-883B TEST METHODS	DESCRIPTION	JAN M38510 CLASS B	JAN M38510 CLASS C
Preseal Visual MTD. 2010	Cond. A Maximum Visual Criteria Cond. B. Optimum Visual Criteria	PRESEAL VISUAL COND. B	PRESEAL VISUAL COND. B
Bond Strength MTD 2011	Bond strength is monitored on a sample basis three times per shift per machine	BOND STRENGTH COND. D	BOND STRENGTH COND. D
Seal	Devices are hermetically sealed for compliance to MIL-STD-883 requirements	SEAL	SEAL
High Temp Storage MTD 1008	Cond. C Tstg = 150°C	BAKE COND. C MIN 24 HRS.	BAKE COND. C MIN 24 HRS.
Temperature Cycle MTD 1010	Cond. C −65°/150°C 10 cycles	TEMP CYCLE COND. C	TEMP CYCLE COND. C
Constant Acceleration MTD 2001 (Note1)	Cond. E 30000 G's X_1, X_2, Y_1, Y_2	CENTRIFUGE COND. E Y_1 ONLY	CENTRIFUGE COND. E Y_1 ONLY
Hermetic Seal MTD 1014 (Note 1)	Cond. A Fine-Helium $5x10^{-8}$ cc/sec Cond. B Fine-Radiflo $5x10^{-8}$ cc/sec Cond. C Gross-FC43/Hot 10^{-3} cc/sec or Gross-FC78/Vacuum 10^{-5} cc/sec	HERMETICITY COND. A/B COND. C	HERMETICITY COND. A/B COND. C
Pre Burn-in Electrical MTD 5004	25°C dc electrical testing to remove rejects prior to submission to burn-in screen	PRE B/I ELECT 25°C dc	
Burn-in Screen MTD 1015	Cond. A, Cond. B, Cond. C Cond. D, Cond. E, Cond. F	BURN IN* 160 HRS 125°C	
Post Burn-in Electrical MTD 5004	Post Burn-in electrical screening to cull out devices which failed as a result of burn-in. Test Parameters may include: 25°C dc, 125°C dc, −55°C dc, 25°C dc, 25°C ac and 25°C Functional tests.	PST B/I ELECT 25°C dc +125°C dc −55°C dc 25°C ac 10% PDA	ELECTRICAL 25°C dc 25°C FUNCTIONAL
Quality Conformance Inspection MTD 5005	Group A: Electrical Characteristics Group B: Package oriented Tests Group C: Life Tests Group D: Environmental Tests	QUALITY CONFORMANCE Gp A, B, C and D	QUALITY CONFORMANCE Gp A, B, C and D
External Visual MTD 2009	3X, 10X magnification: Verify dimensions, configuration, lead structure, marking and workmanship	EXTERNAL VISUAL 100%	EXTERNAL VISUAL 100%
RELIABILITY	Figure of Merit	15	2
ORDERING	Part Number	JM38510/ 10101BCB	JM38510/ 10101CCB
	Part Marking	JM38510/ 10101BCB	JM38510/ 10101CCB

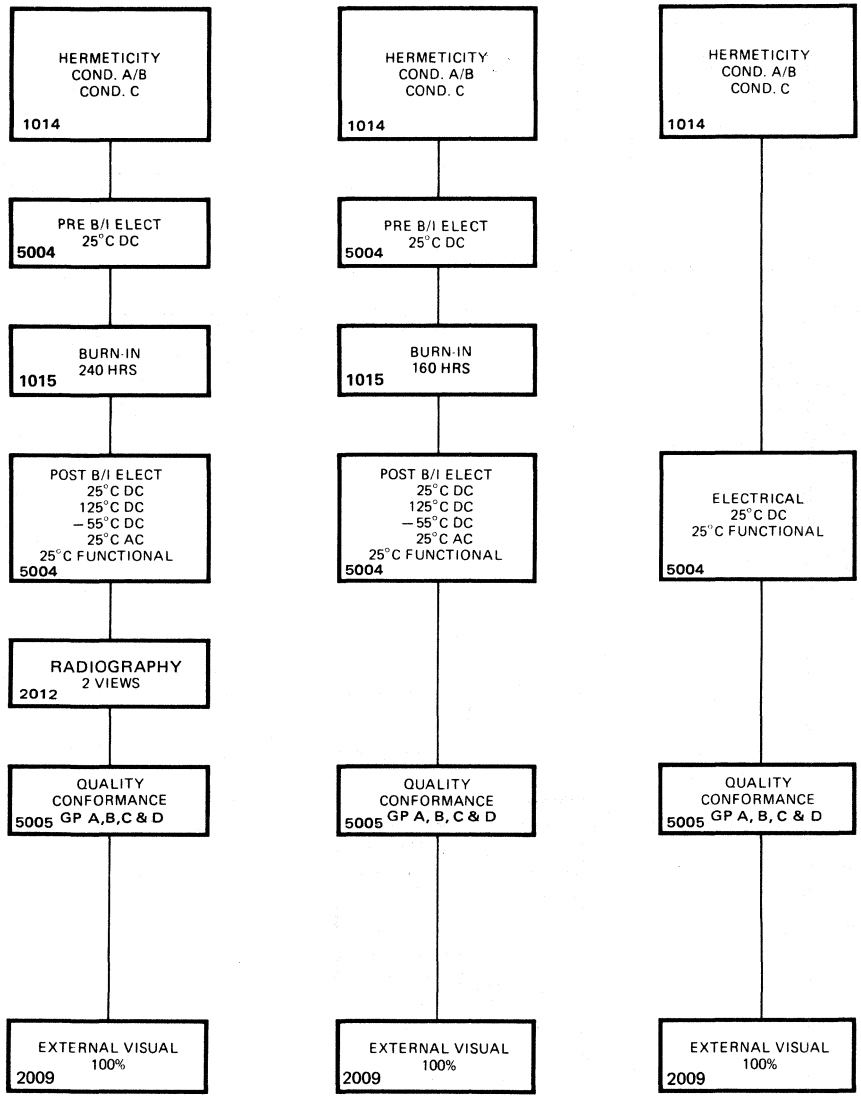
NOTE: RELIABILITY Figure of Merit is the Reliability Improvement Factor from RADC Reliability Notebook, Vol. II, RADC-TR-67-108, Table XII-6, page 419.

1. Not Applicable for T0-3 Cans

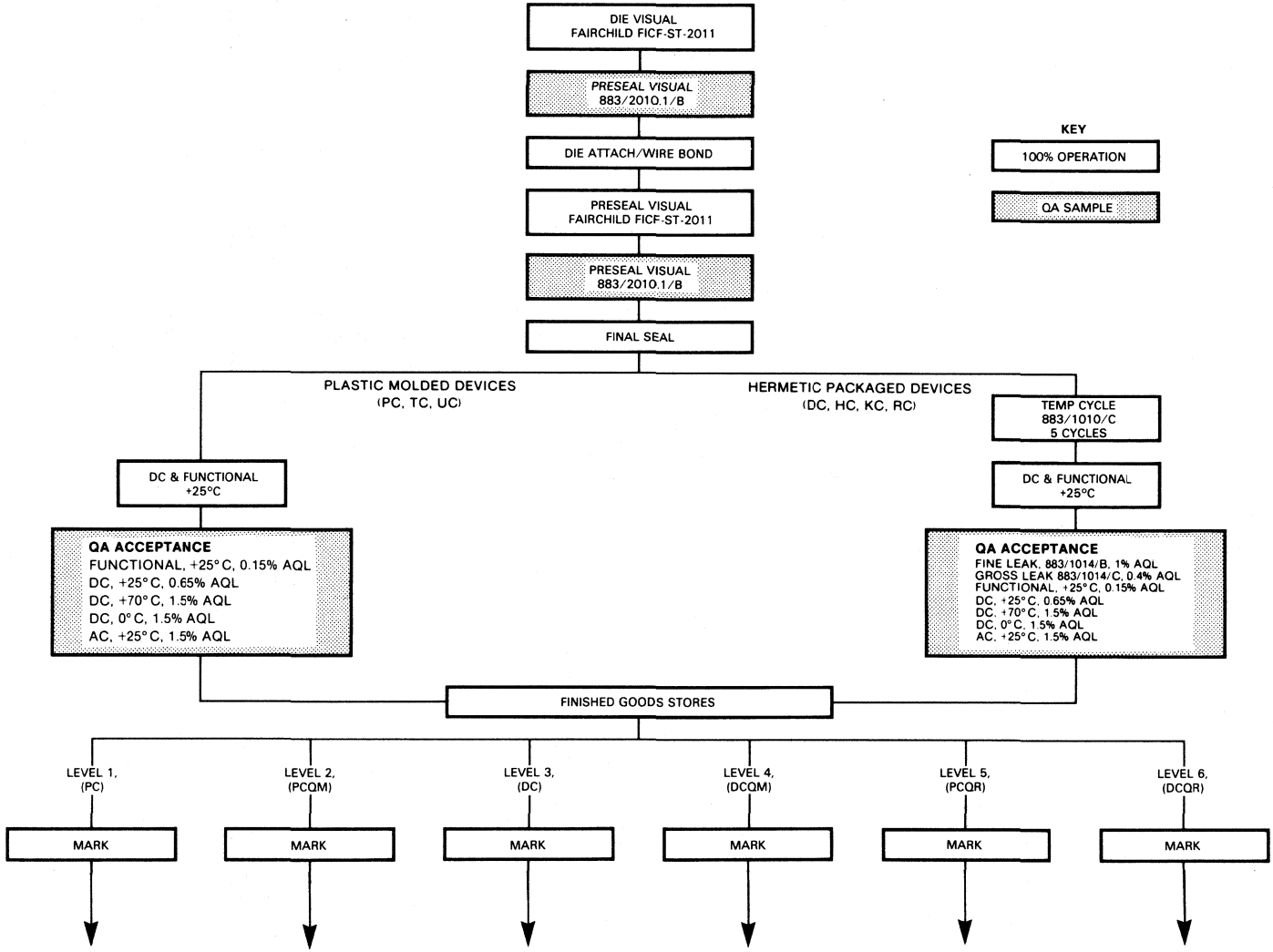
*Time Temperature Curve (method 1015) may be used.

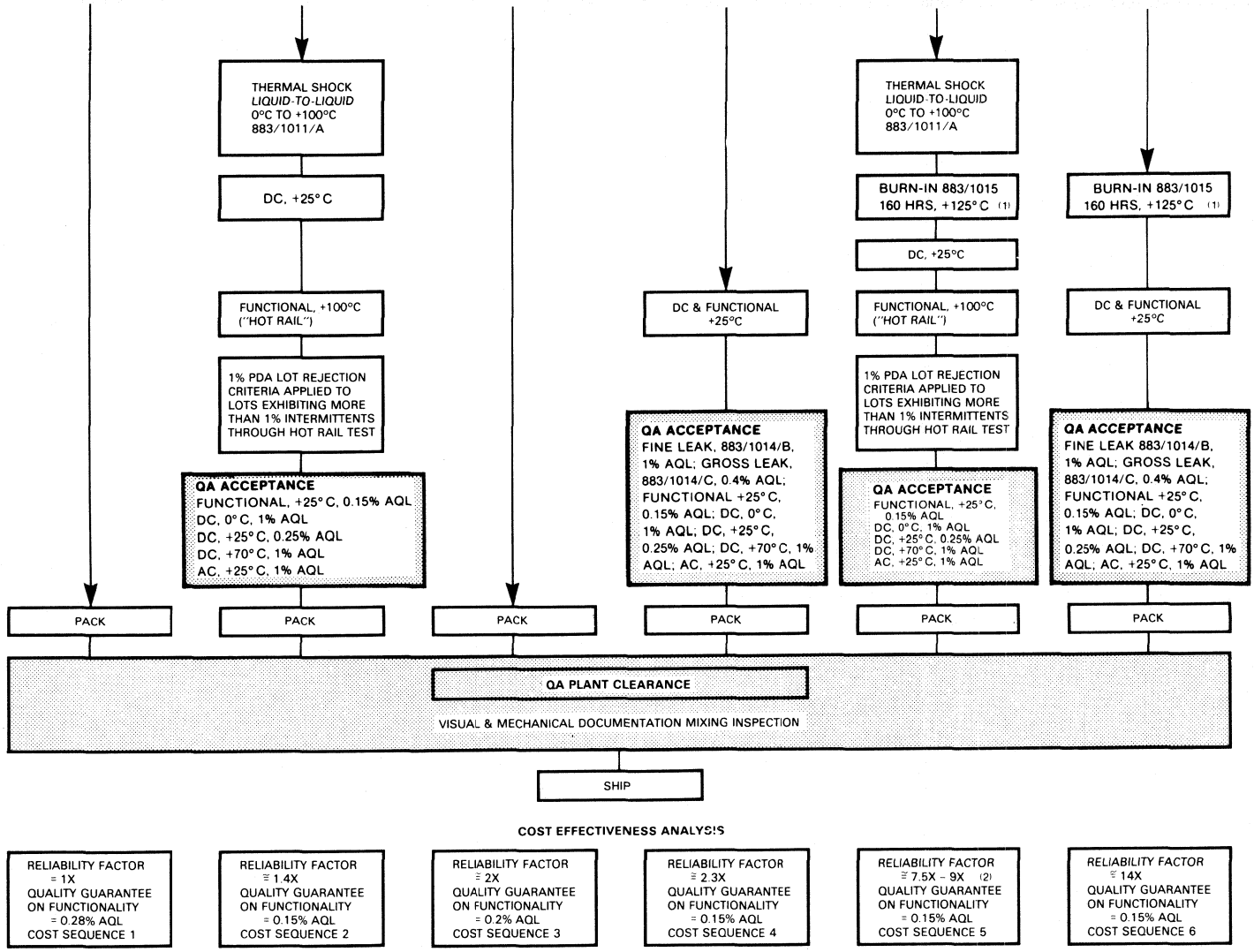
UNIQUE II


CLASS QS (883S)
CLASS QB (883B)
CLASS QC (883C)
PRESEAL VISUAL COND. A 2010
PRESEAL VISUAL COND. B 2010
PRESEAL VISUAL COND. B 2010
BOND STRENGTH ACCEPTANCE 2011 COND. D
BOND STRENGTH ACCEPTANCE 2011 COND. D
BOND STRENGTH ACCEPTANCE 2011 COND. D
SEAL
SEAL
SEAL
BAKE COND. C MIN 1008 24 HRS.
BAKE COND. C MIN 1008 24 HRS.
BAKE COND. C MIN 1008 24 HRS.
THERMAL SHOCK COND. A 1011
TEMP CYCLE COND. C 1010
TEMP CYCLE COND. C 1010
TEMP CYCLE COND. C 1010
MECHANICAL SHOCK COND. B, Y1 2002
CENTRIFUGE COND. E Y1 & Y2 2001
CENTRIFUGE COND. E Y1 ONLY 2001
CENTRIFUGE COND. E Y1 ONLY 2001

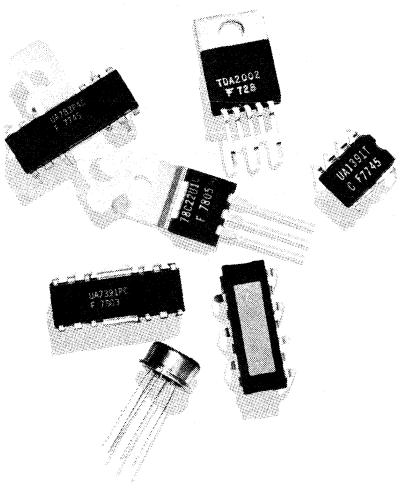

HERMETICITY
COND. A/B
COND. C
1014
PRE B/I ELECT
25°C DC
5004
BURN-IN
240 HRS
1015
POST B/I ELECT
25°C DC
125°C DC
−55°C DC
25°C AC
25°C FUNCTIONAL
5004
RADIOGRAPHY
2 VIEWS
2012
QUALITY
CONFORMANCE
5005 GP A,B,C & D
EXTERNAL VISUAL
100%
2009
μA741 DMQS
HERMETICITY
COND. A/B
COND. C
1014
PRE B/I ELECT
25°C DC
5004
BURN-IN
160 HRS
1015
POST B/I ELECT
25°C DC
125°C DC
−55°C DC
25°C AC
25°C FUNCTIONAL
5004
QUALITY
CONFORMANCE
5005 GP A, B, C & D
EXTERNAL VISUAL
100%
2009
μA741 DMQB
HERMETICITY
COND. A/B
COND. C
1014
ELECTRICAL
25°C DC
25°C FUNCTIONAL
5004
QUALITY
CONFORMANCE
5005 GP A, B, C & D
EXTERNAL VISUAL
100%
2009
μA741 DMQC

MATRIX VI PROCESS FLOW OPTIONS & COST EFFECTIVENESS





NOTE:
(1) Temperature Accelerated Testing may be used for MIL-STD-883 method 1015 Test Condition F.
(2) Burn-In has the same relative effectiveness for plastic molded devices as for ceramic/hermetic packaged devices. Assuming a controlled (air conditioned and constant power) field application/environment, the reliability factor would be approximately 9x. But should the field application be in a less controlled and power on/off application, the reliability would be approximately 7.5X.



DICE POLICY

GENERAL INFORMATION

Fairchild linear integrated circuits, constructed using the Fairchild Planar* epitaxial process, are available in dice form incorporating these features:

- Commercial or Military Selection (Military Limits Probed at 25°C)
- MIL-STD-883, Method 2010.2, Condition B Visual
- Gold Backing
- Glass Passivation
- Protective Packaging

ELECTRICAL CHARACTERISTICS

Each die is electrically tested at 25°C to guaranteed commercial dc parameters.

Military grade dice are guardband tested at 25°C dc to guarantee military temperature range operation.

QUALITY ASSURANCE

All Fairchild linear dice are 100% visually inspected and conform to MIL-STD-883, Method 2010.2, Condition B. In addition, quality control visually inspects the dice to a given sampling plan.

Each die is gold backed to aid die attach. Most dice are available with glass passivation coating with only the bonding pads exposed.

SHIPPING PACKAGES

Linear dice are packaged in containers with an anti-static sheet inserted between the lid and the dice. This sheet guards against electrostatic damage during shipment and storage.

The clear plastic carrier allows visual inspection of all the packaged dice. Each carrier is heat sealed within a transparent bag. A small piece of dehydrator paper with humidity indicating color is inserted in each bag prior to sealing.

ORDER INFORMATION

The minimum order quantity is 100 pieces and 100 piece increments of value greater than $1000.00 per line item.

Each linear integrated circuit die has a unique order code which describes the device type, the dice designation and type of electrical tests performed. The dice designation is denoted by an "X" and is substituted for the package code. Examples follow:

Generic Type	Order Code
μA741C**	μA741XC
μA3045	μA3045XC
μA75450	μA75450XC
μA101A	μA101AXC
μA796C	μA796XC

**Some device types imply a military or commercial range by the generic type. Where this does not occur the suffix should be:

XM Military Grade Die

or XC Commercial Grade Die

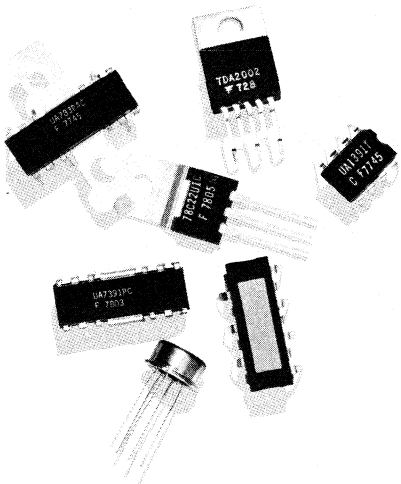
SPECIAL CHIP PROCESSING

If there is a need for additional testing or processing, Fairchild will negotiate with the customer to meet his requirements.

PRODUCT AVAILABLE IN DICE FORM

Please refer to FSC OEM Price List for product available in die form.

*Planar is a patented Fairchild process.



μA703

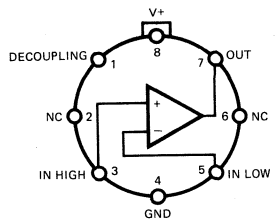
RF-IF AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA703 is a monolithic RF-IF Amplifier constructed using the Fairchild Planar* epitaxial process and is intended for use as a limiting or non-limiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability and versatility of the device.

- **29 mmho MINIMUM FORWARD TRANSADMITTANCE**
- **1.0 mmho/0.05 mmho MAXIMUM INPUT/OUTPUT CONDUCTANCE**
- **18 pF/4.0 pF MAXIMUM INPUT/OUTPUT CAPACITANCE**

CONNECTION DIAGRAM
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5C
PACKAGE CODE H



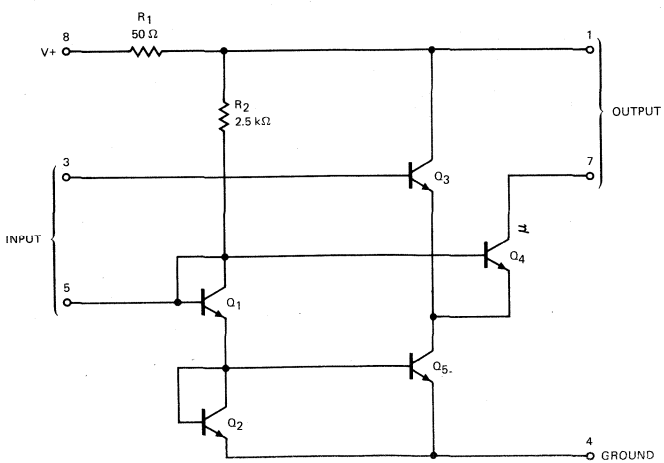
ORDER INFORMATION

TYPE	PART NO.
μA703	μA703HM
μA703C	μA703HC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	±5.0 V
Internal Power Dissipation	200 mW
Operating Temperature Range (μA703)	–55°C to +125°C
Operating Temperature Range (μA703C)	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Pin Temperature (Soldering, 10 s)	300°C

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

μA703

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_+ = 12$ V unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Power Consumption	$e_{IN} = 0$		110	170	mW
Quiescent Output Current	$e_{IN} = 0$	2.1	2.5	3.1	mA
Peak-to-Peak Output Current	$e_{IN} = 400$ mV rms, f = 1 kHz	4.0			mA
Output Saturation Voltage				1.7	V
Forward Transadmittance	$e_{IN} = 10$ mV rms f $\leq$ 1 kHz	29	35		mmbo
Input Conductance	$e_{IN} < 10$ mV rms, f $\leq$ 5 MHz		0.30	0.43	mmbo
Input Capacitance	$e_{IN} < 10$ mV rms, f $\leq$ 5 MHz		7.0	16.0	pF
Output Capacitance	f $\leq$ 5 MHz		2.0	3.0	pF
Output Conductance	$e_O \leq 100$mV rms, f $\leq$ 5 MHz		0.02	0.04	mmbo
The following specifications apply for $-55°C \leq T_A \leq +125°C$					
Quiescent Output Current	$e_{IN} = 0$	1.7		3.1	mA
Peak-to-Peak Output Current	$e_{IN} = 400$ mV rms, f = 1 kHz	3.2			mA
Output Saturation Voltage				1.8	V
Forward Transadmittance	$e_{IN} = 10$ mV rms, f $\leq$ 1 kHz	21			mmbo
Input Conductance	$e_{IN} < 10$ mV rms, f $\leq$ 5 MHz			1.2	mmbo
Output Conductance	$e_O \leq 100$ mV rms, f $\leq$ 5 MHz			0.05	mmbo

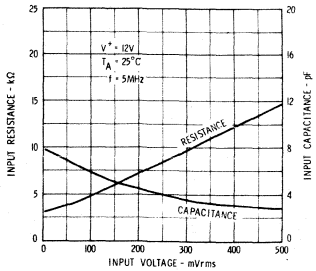
μA703C

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_+ = 12$ V unless otherwise specified)

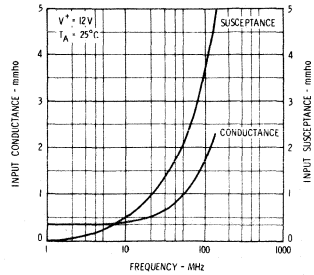
CHARACTERISTICS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$e_{IN} = 0$		9.0	14	mA
Power Consumption	$e_{IN} = 0$		110	170	mW
Quiescent Output Current	$e_{IN} = 0$	1.5	2.5	3.3	mA
Peak-to-Peak Output Current	$e_{IN} = 400\ mV_{rms}$, f = 1 kHz	3.0			mA
Output Saturation Voltage	$I_7 = 2.5$ mA			1.7	V
Forward Transadmittance	$e_{IN} = 10\ mV_{rms}$, f = 1 kHz	29	33		mmho
Input Conductance	$e_{IN} < 10\ mV_{rms}$, f = 10.7 MHz		0.35	1.0	mmho
Input Capacitance	$e_{IN} < 10\ mV_{rms}$, f = 10.7 MHz		9.0	18	pF
Output Conductance	$e_{OUT} = 100\ mV_{rms}$, f = 10.7 MHz		0.03	0.05	mmho
Output Capacitance	$e_{OUT} = 100\ mV_{rms}$, f = 10.7 MHz		2.0	4.0	pF
Noise Figure	f = 10.7 MHz, $R_S = 500\ \Omega$		6.0		dB
	f = 100 MHz, $R_S = 500\ \Omega$		8.0		dB

TYPICAL PERFORMANCE CURVES FOR μA703

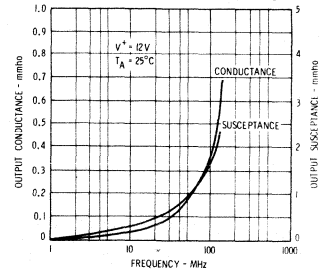
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



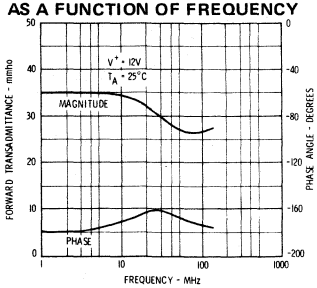
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



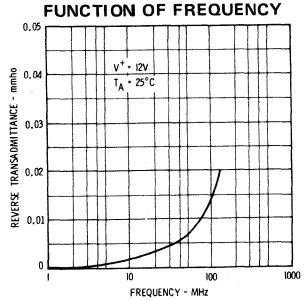
OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



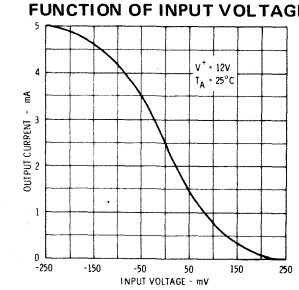
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



4

μA706

5 WATT AUDIO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA706 monolithic 5.0 W Audio Amplifier is constructed using the Fairchild Planar* epitaxial process. It is ideally suited as an audio amplifier in automobile radios. Provided with adequate heat sinking, the circuit is optimized to provide 5.5 W (continuous output) into a 4.0 Ω speaker using a single 14 V supply. The circuit operates over the full automobile battery range of 6.0 V to 16 V. The μA706 incorporates such special features as self-centering bias, direct coupling to the input, low quiescent current, high input impedance and low distortion. Operation as a 5.0 W audio amplifier is achieved with minimal external components.

Other applications for the μA706 are home audio equipment, TV receivers and many industrial applications.

- **OUTPUT POWER 5.5 W (14 V – 4 Ω)**
- **LOW DISTORTION**
- **LOW QUIESCENT CURRENT**
- **SELF CENTERING BIAS**
- **HIGH INPUT IMPEDANCE**
- **HIGH PEAK OUTPUT CURRENT**
- **HIGH IMMUNITY TO DAMAGE FROM SHORT-CIRCUITED LOAD†**
- **PIN-FOR-PIN REPLACEMENT FOR TBA641B**

†The device will withstand repetitive short circuits across the speaker load if the absolute maximum junction temperature is not exceeded.

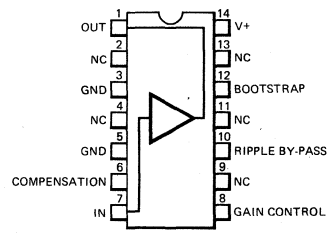
CONNECTION DIAGRAM

14-PIN DIP

(TOP VIEW)

PACKAGE OUTLINES 9H 9J

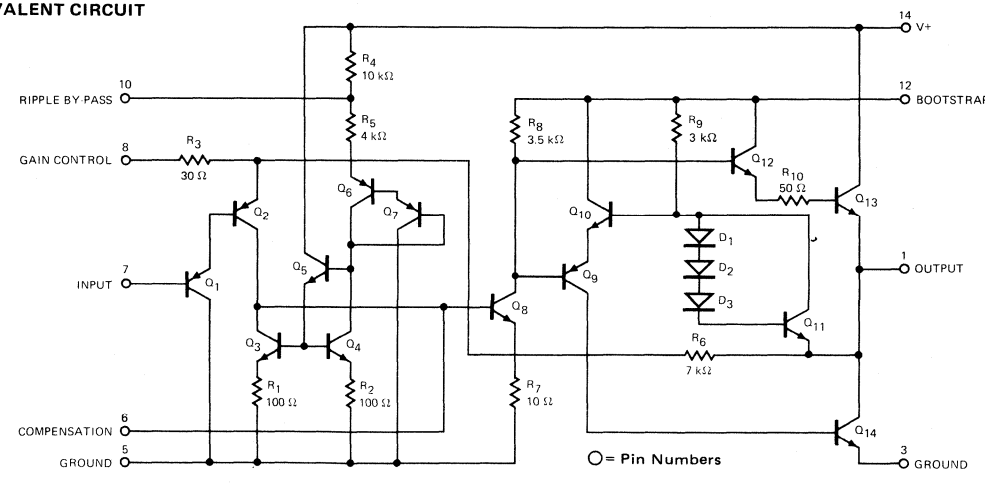
PACAKGE CODES AP BP



ORDER INFORMATION

TYPE	PART NO.
μA706AC	μA706APC
μA706BC	μA706BPC

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (No Signal)	25 V
Supply Voltage	16 V
Input Voltage	−0.5 V to V^+
Peak Output Current	2.5 A
Operating Temperature Range	−30°C to +85°C
Storage Temperature	−55°C to +125°C
Maximum Junction Temperature	150°C
Power Dissipation ($T_C \leq 85°C$)	5 W
Power Dissipation ($T_A \leq 25°C$)	
Package Type AP	1.7 W
Package Type BP	2.3 W
Power Dissipation ($T_A \leq 85°C$)	
Package Type AP	0.9 W
Package Type BP	1.2 W

PACKAGE THERMAL RESISTANCE

Thermal Resistance, Junction to Ambient	
Package Type AP	73°C/W
Package Type BP	55°C/W
Thermal Resistance, Junction to Case	
Package Type AP	11°C/W
Package Type BP	12°C/W

4

μA706C

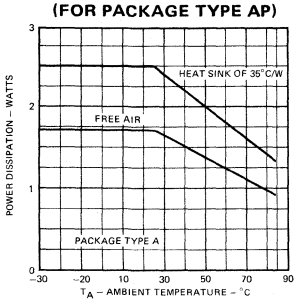
ELECTRICAL CHARACTERISTICS: $V_+ = 14V$, $R_L = 4\ \Omega$, $T_A = 25°C$, $\theta_{C-A} = 13°C/W$, Test Circuit 1, unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Total Supply Current	$P_{OUT} = 0$	10	18	30	mA
Quiescent Current in Output Transistors	$P_{OUT} = 0$	7	15	27	mA
Input Bias Current			200	950	nA
DC Output Level	$R_S = 22\ k\Omega$	6.55	7.0	7.45	V
Voltage Gain, A_V	$R_B = 0\ \Omega$	43	46	49	dB
Output Power, P_{OUT}	THD = 10%, f = 1 kHz, A_V = 46 dB	4.5	5.5		W
Total Harmonic Distortion	f = 1 kHz, A_V = 46 dB				
	P_{OUT} = 50 mW		0.3		%
	P_{OUT} = 2.0 W		0.5		%
	P_{OUT} = 4.5 W		3.0		%
Equivalent Input Noise Voltage	R_S = 22 kΩ, B.W. = 10 kHz		3.5		μV
Total Supply Current	P_{OUT} = 4.5 W		510		mA
Input Impedance	A_V = 46 dB, f = 1 kHz		3.0		MΩ

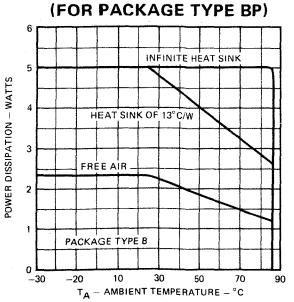
TYPICAL PERFORMANCE CURVES FOR μA706C

($T_A = 25°C$, $\theta_{C-A} = 13°C/W$, Test Circuit 1, A_V = 46 dB)

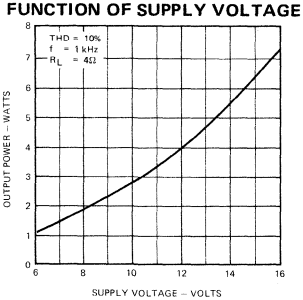
MAXIMUM ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (FOR PACKAGE TYPE AP)



MAXIMUM ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (FOR PACKAGE TYPE BP)

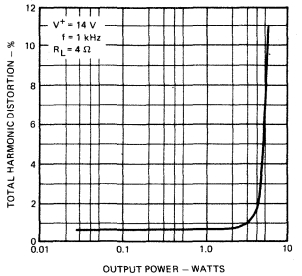


OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE

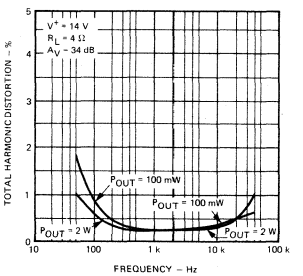


TYPICAL PERFORMANCE CURVES FOR μA706C (Cont'd)

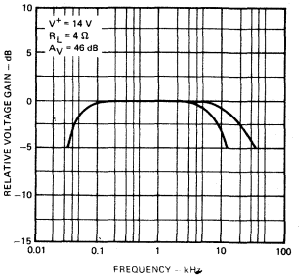
TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER



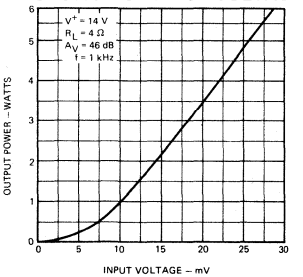
TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY



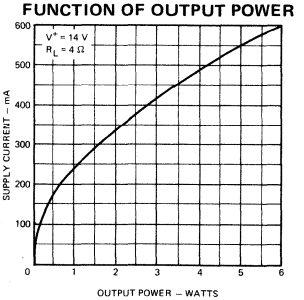
RELATIVE VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



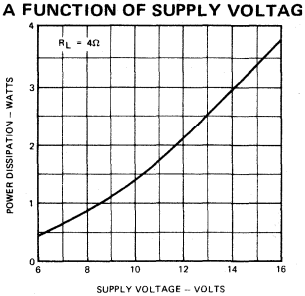
OUTPUT POWER AS A FUNCTION OF INPUT VOLTAGE



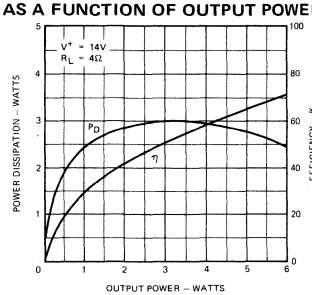
SUPPLY CURRENT AS A FUNCTION OF OUTPUT POWER



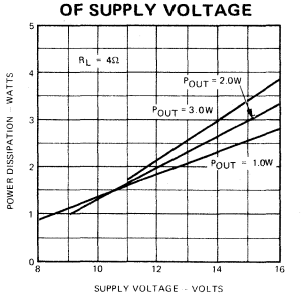
MAXIMUM POWER DISSIPATION BY THE INTEGRATED CIRCUIT AS A FUNCTION OF SUPPLY VOLTAGE



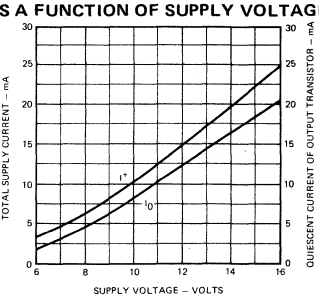
POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF OUTPUT POWER



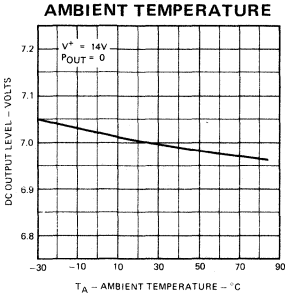
POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE



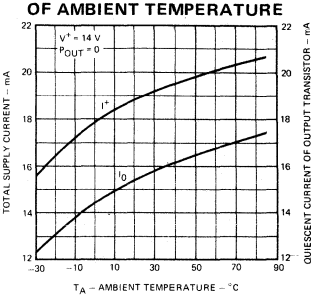
TOTAL SUPPLY CURRENT AND QUIESCENT CURRENT OF OUTPUT TRANSISTOR AS A FUNCTION OF SUPPLY VOLTAGE



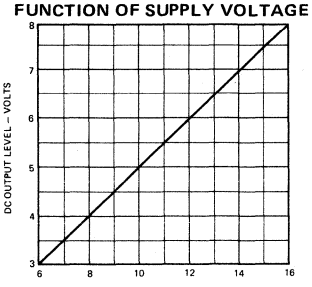
DC OUTPUT LEVEL AS A FUNCTION OF AMBIENT TEMPERATURE



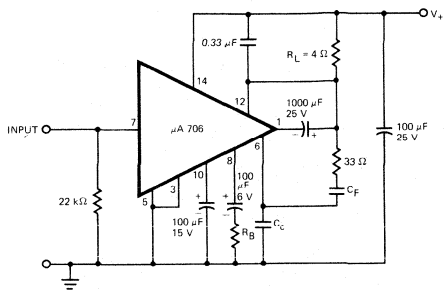
TOTAL SUPPLY CURRENT AND QUIESCENT CURRENT OF OUTPUT TRANSISTOR AS A FUNCTION OF AMBIENT TEMPERATURE



DC OUTPUT LEVEL AS A FUNCTION OF SUPPLY VOLTAGE

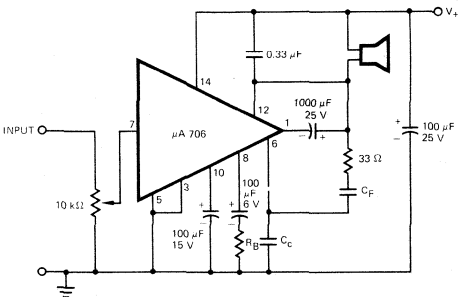


TEST CIRCUIT 1 (A_V = 46 dB, R_B = 0 Ω, C_c = 1.5 nF, C_F = 150 pF)



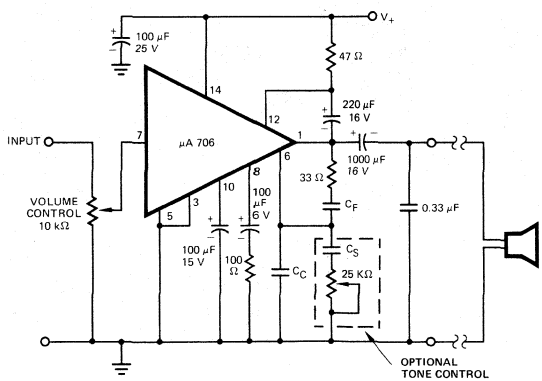
TYPICAL AUDIO APPLICATIONS

5 WATT AUDIO AMPLIFIER WITH MINIMUM COMPONENT COUNT



A_V	34 dB		46 dB	
BW	10 kHz	20 kHz	10 kHz	20 kHz
R_B	100 Ω	100 Ω	0 Ω	0 Ω
C_c	10 nF	6.8 nF	2.7 nF	1.5 nF
C_F	1 nF	470 pF	330 pF	150 pF

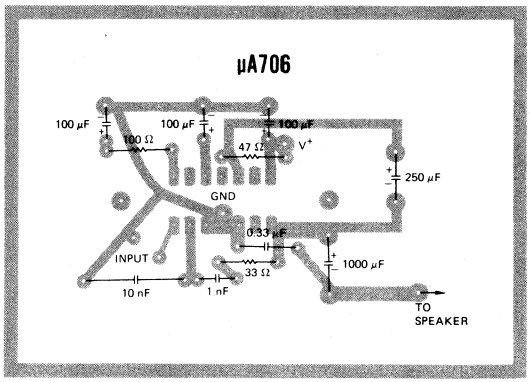
5 WATT AUDIO AMPLIFIER WITH LOAD CONNECTED TO GROUND



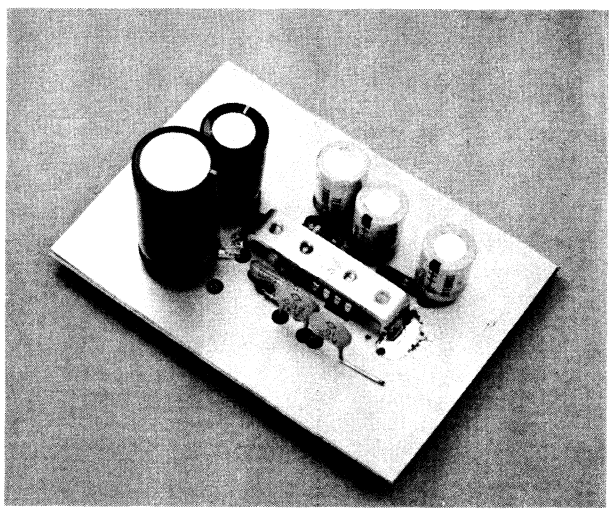
A_V	34 dB	46 dB
C_S	27 nF	5.6 nF

Note: C_S selected for 3 dB at 4 kHz.

A PC BOARD LAYOUT FOR THE 5 WATT AUDIO AMPLIFIER



PHOTOGRAPH OF THE μA706 IN A TYPICAL APPLICATION



μA720
AM RADIO SYSTEM
FAIRCHILD LINEAR INTEGRATED CIRCUIT

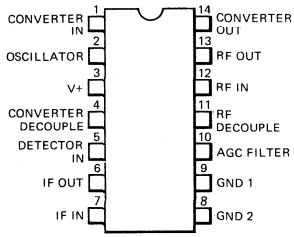
GENERAL DESCRIPTION – The μA720 is a monolithic AM Radio Receiver System made with the *patented Fairchild Planar* epitaxial process. The device contains two amplifiers, a mixer-oscillator, an* AGC detector and a voltage regulator. It is intended for superheterodyne AM receiver applications. Since all parts of the circuit are accessible separately, the μA720 can be used in a variety of other applications. The voltage regulator is protected against short term overvoltage transients.

- **AM-RF OSCILLATOR-CONVERTER, IF AMPLIFIER ON ONE CHIP**
- **REGULATED SUPPLY**
- **OVERVOLTAGE PROTECTION**
- **AMPLIFIERS SEPARATELY ACCESSIBLE**
- **AGC FOR RF STAGE**

ABSOLUTE MAXIMUM RATINGS

Operating Voltage	16V
Current into Supply Terminal (Pin 3)	40mA
Power Dissipation (Note 1)	670mW
Current into RF Output Terminal (Pin 13)	20mA
Current into RF Input Terminal (Pin 12)	10mA
Current into IF Input Terminal (Pin 7)	10mA
Current into or out of Detector Input Terminal (Pin 5)	±10mA
Current into AGC Filter Terminal (Pin 10)	10mA
Negative Voltage on RF Input, IF Input, and Detector Input Terminals	−5V
Negative Voltage on Converter Input Terminal	0V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature	
Molded DIP (Soldering, 10 s)	260°C

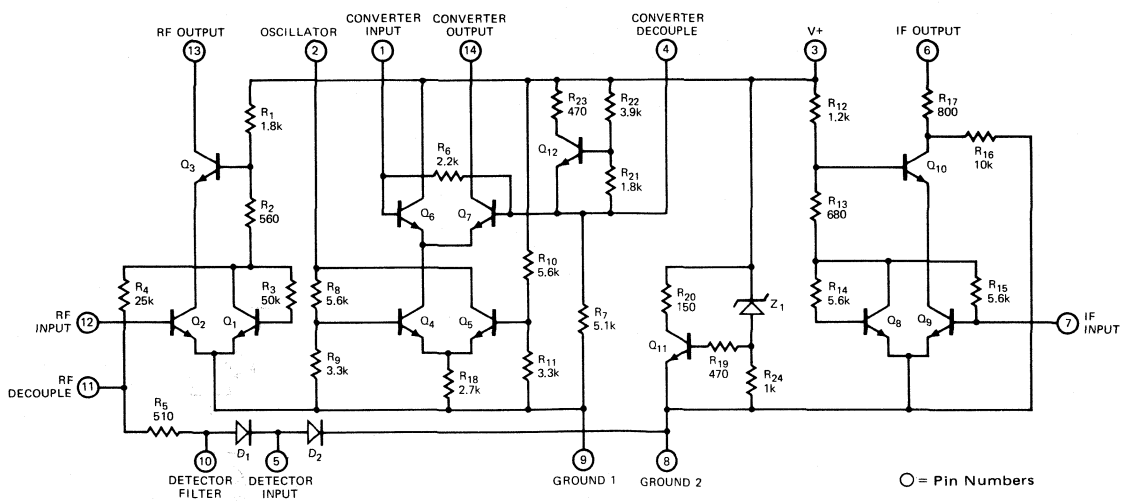
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9A
PACKAGE CODES P



ORDER INFORMATION

TYPE	PART NO.
μA720C	μA720PC

EQUIVALENT CIRCUIT



See notes on following page.

*Planar is a patented Fairchild process.

μA720C

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_+ = 12$ V, Test Circuit 1, unless otherwise indicated

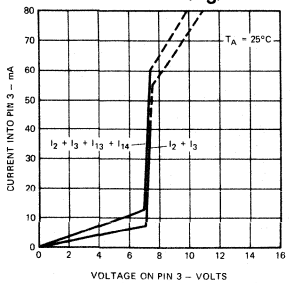
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS (Oscillator OFF, S_1 in Pos 2, S_3 in Pos 2, unless otherwise indicated)					
Voltage on Supply Terminal (V_3)	$I_2 + I_3 = 15$ mA	6.6	7.0	7.5	V
Voltage on Supply Terminal (V_3)	$I_2 + I_3 + I_{13} + I_{14} = 22$ mA, S_3 in Pos 1	6.6	7.0	7.5	V
Current into Oscillator and Supply Terminal ($I_2 + I_3$)	$V_3 = 5$ V, S_1 in Pos 1	4.0	6.0	8.0	mA
Current into Oscillator, Supply, RF Out, and Conv. Out Terminals ($I_2 + I_3 + I_{13} + I_{14}$)	$V_3 = 5$ V, S_1 in Pos 1, S_3 in Pos 1	6.0	9.0	12	mA
Oscillator Current (I_2)	$I_2 + I_3 = 15$ mA		1.2		mA
RF Output Current (I_{13})	$I_2 + I_3 = 15$ mA		4.0		mA
IF Output Current (I_6)	$I_2 + I_3 = 15$ mA		4.0		mA
Voltage on Converter Input (V_1)	$I_2 + I_3 = 15$ mA		5.8		V
Voltage on IF Input (V_7)	$I_2 + I_3 = 15$ mA		0.75		V
Voltage on RF Input (V_{12})	$I_2 + I_3 = 15$ mA		0.67		V
Internal Power Dissipation	$I_2 + I_3 + I_{13} + I_{14} = 22$ mA, S_3 in Pos 1		200		mW
AC CHARACTERISTICS (Signals are measured at the device pins)					
RF Transconductance ($gm_{RF} = i_{13}/e_{12}$)	$f_{12} = 1$ MHz, $e_{12} = 100\ \mu V_{RMS}$, $e_5 = 0$ Oscillator OFF	80	120	180	mmhos
RF Input Resistance (R_{IN12})	$f_{12} = 1$ MHz, $e_{12} = 100\ \mu V_{RMS}$, S_2 in Pos 2	500	1000		Ω
RF Input Capacitance (C_{IN12})	$f_{12} = 1$ MHz, $e_{12} = 100\ \mu V_{RMS}$, S_2 in Pos 2		50		pF
RF Output Resistance (R_{OUT13})	$f_{13} = 1$ MHz		50		kΩ
RF Output Capacitance (C_{OUT13})	$f_{13} = 1$ MHz		10		pF
RF Noise Voltage, $\sqrt{en^2}$	Referred to Input, $R_S = 50\ \Omega$, $f_{13} = 1$ MHz		3.0		$nV/\sqrt{Hz}$
Detector Input Voltage (e_5)	RF Stage Gain Reduction				
	$\Delta gm_{RF} = 3$ dB, $f_{13} = 1$ MHz, $f_5 = 260$ kHz	140	180	250	mV_{RMS}
	$\Delta gm_{RF} = 40$ dB, $f_{13} = 1$ MHz, $f_5 = 260$ kHz	220	270	330	mV_{RMS}
IF Tranconductance ($gm_{IF} = i_e/e_7$)	$f_7 = 260$ kHz, $e_7 = 1\ mV_{RMS}$	50	90	130	mmhos
IF Input Resistance (R_{IN7})	$f_7 = 260$ kHz	600	1000		Ω
IF Input Capacitance (C_{IN7})	$f_7 = 260$ kHz		70		pF
IF Output Resistance (R_{OUT6})	$f_6 = 260$ kHz		10		kΩ
IF Output Capacitance (C_{OUT6})	$f_6 = 260$ kHz		8		pF
Converter Transconductance ($gm_{CON} = i_{14}/e_1$)	$f_1 = 1$ MHz, $e_1 = 1\ mV_{RMS}$, $f_{14} = f_{oscillator} - f_1$	1.5	2.5	3.4	mmhos
Converter Input Resistance (R_{IN1})	$f_1 = 1$ MHz	1000	1400		Ω
Converter Input Capacitance (C_{IN1})	$f_1 = 1$ MHz		8		pF
Converter Output Resistance (R_{OUT14})	$f_{14} = 260$ kHz		50		kΩ
Converter Output Capacitance (C_{OUT14})	$f_{14} = 260$ kHz		10		pF
Oscillator Output Voltage (e_2)			1.2		V_{RMS}

Note 1. Rating applies for ambient temperatures to +70°C. Derate at 8.3 mW/°C between +70°C and +85°C.

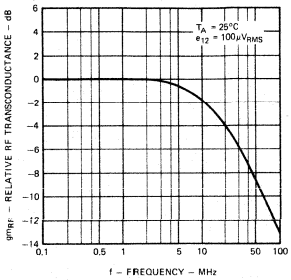
TYPICAL PERFORMANCE CURVES FOR μA720C

TEST CIRCUIT 1, unless otherwise specified.

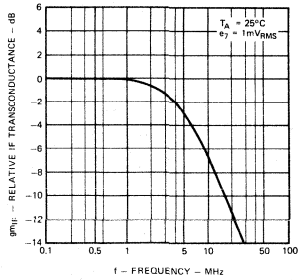
CURRENTS AS A FUNCTION OF VOLTAGE (V_3)



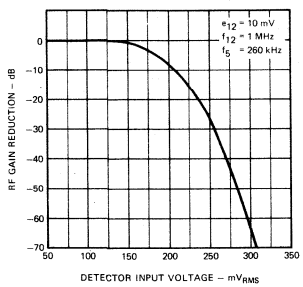
RF TRANSCONDUCTANCE AS A FUNCTION OF FREQUENCY



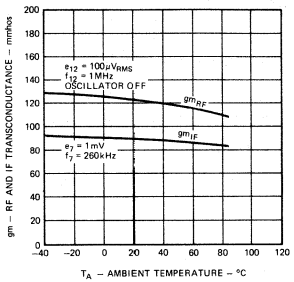
IF TRANSCONDUCTANCE AS A FUNCTION OF FREQUENCY



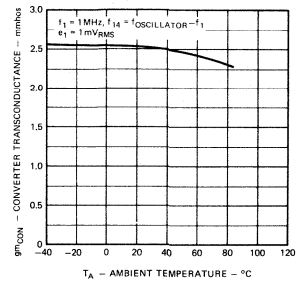
RF AGC CHARACTERISTIC



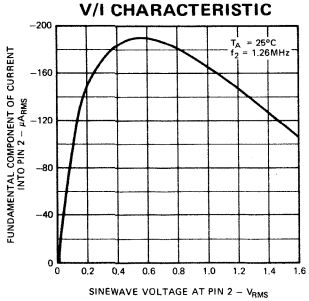
RF AND IF TRANSCONDUCTANCE AS A FUNCTION OF TEMPERATURE



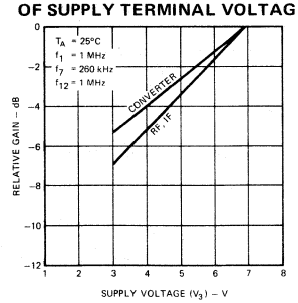
CONVERTER TRANSCONDUCTANCE AS A FUNCTION OF TEMPERATURE



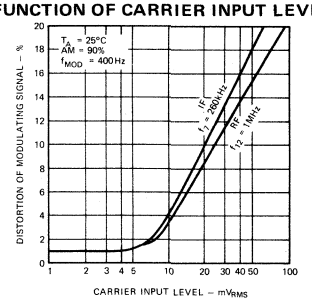
OSCILLATOR TERMINAL (PIN 2) V/I CHARACTERISTIC



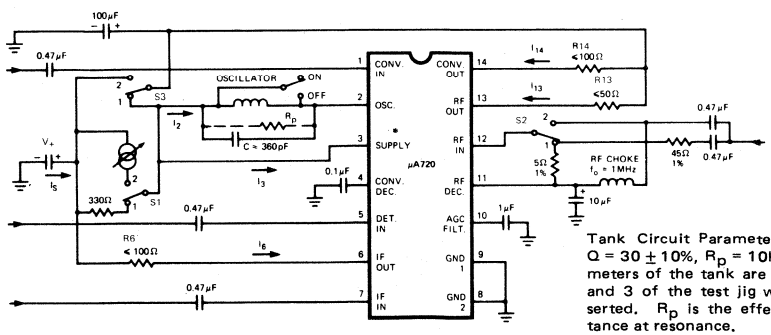
RELATIVE GAIN AS A FUNCTION OF SUPPLY TERMINAL VOLTAGE



TOTAL HARMONIC DISTORTION OF THE MODULATING SIGNAL AS A FUNCTION OF CARRIER INPUT LEVEL

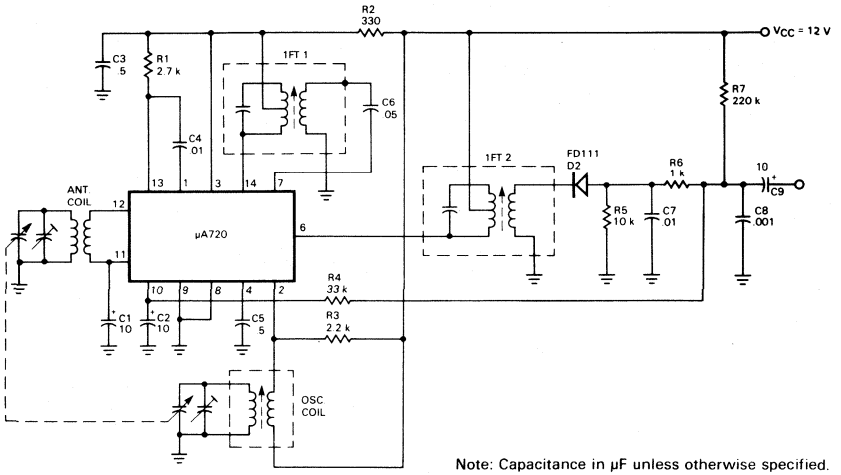


TEST CIRCUIT 1



Tank Circuit Parameters: f_o = 1.26MHz, Q = 30 ± 10%, R_p = 10kΩ ± 5%. The parameters of the tank are measured at pins 2 and 3 of the test jig without a device inserted. R_p is the effective parallel resistance at resonance.

HOME RADIO APPLICATION (Capacitor Tuned)

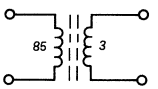


Note: Capacitance in μF unless otherwise specified.

PARTS LIST

Ferrite Antenna Bar: Q2BAR 1080/TDK Electronics
Lenght: 80mm
Diameter: 10mm

Antenna Coil:

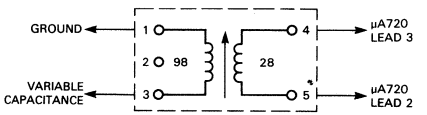


Variable Capacitance: PVC — LX20T/MITSUMI ELECTRIC
Antenna: 5–140 pF
Oscillator: 4.5–82 pF

OSCILLATOR COIL (BOTTOM VIEW)

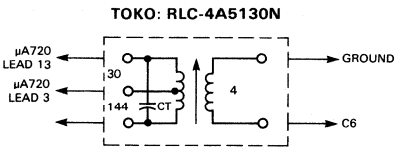
$L_{(1-3)}$ = 360 μH
Q_U = 140
f = 796 kHz

TOKO: RBO-6A5105BM



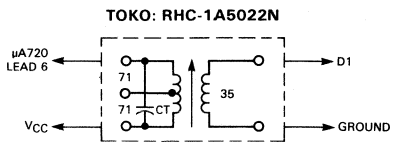
1FT 1 (BOTTOM VIEW)

TOKO: RLC-4A5130N

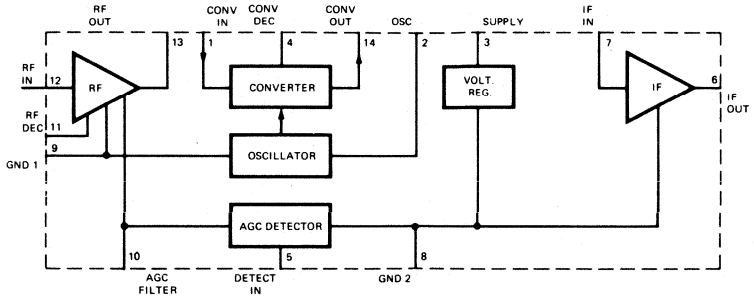


1FT 2 (BOTTOM VIEW)

TOKO: RHC-1A5022N

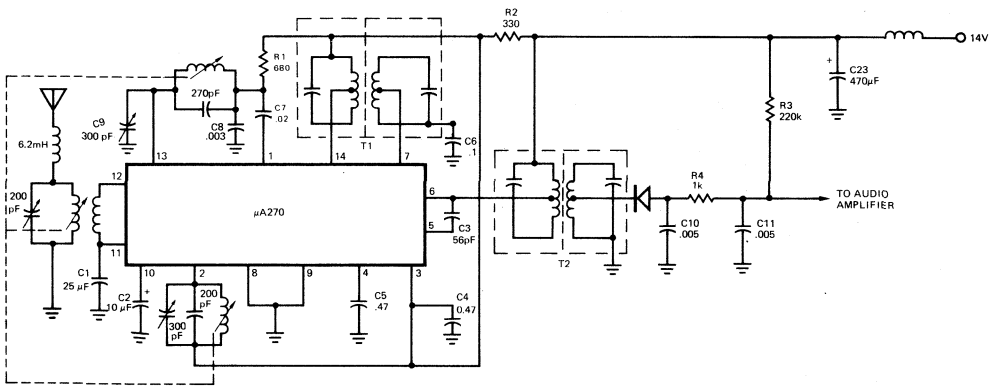


BLOCK DIAGRAM AND TYPICAL APPLICATIONS

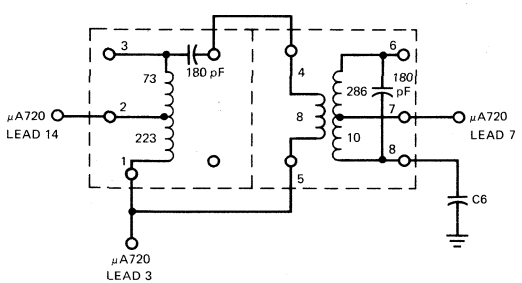


4

AM CAR RADIO APPLICATION (SLUG TUNED)

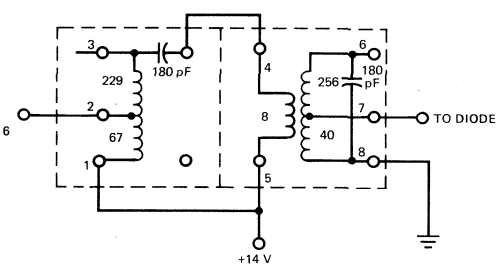


TRANSFORMER (T1)



Q_o = 60, f = 262.5 kHz
TOKO: WYOC–60021QAN
WYOC–60022SDG

TRANSFORMER (T2)



Q_o = 60, f = 262.5 kHz
TOKO: WYOC–60025QAN
WYOC–60026SDG

μA721

AM/FM RADIO SYSTEM

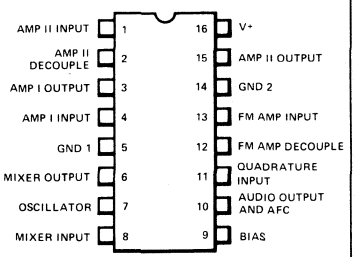
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA721 is a monolithic AM/FM radio receiver system manufactured using the Fairchild Planar* epitaxial process. Several gain blocks are available to perform AM conversion, RF and IF or FM IF amplification. The FM limiter and quadrature detector are also included.

The μA721 is designed to operate over a very wide voltage range (3.5-16 V) making it useful in a wide variety of applications including portable, home and auto AM/FM radios, and industrial communications system.

- **AM-RF, OSCILLATOR CONVERTER AND IF AMPLIFIERS**
- **FM-IF, LIMITER AND QUADRATURE DETECTOR**
- **WIDE SUPPLY VOLTAGE RANGE (3.5-16 V)**
- ***MINIMUM EXTERNAL COMPONENTS***
- **HIGH SENSITIVITY**
- **LOW QUIESCENT CURRENT (20 mA)**

CONNECTION DIAGRAM
16-PIN PACKAGE
PACKAGE OUTLINE 9B
PACKAGE CODE P



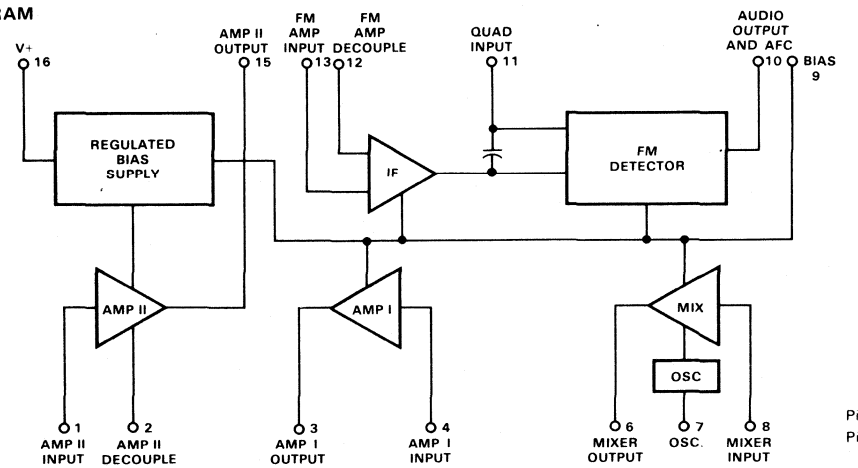
ORDER INFORMATION

TYPE	PART NO.
μA721	μA721PC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18 V
Peak Voltage (Pin 15)	36 V
Power Dissipation $T_A \leq 70°C$	800 mW
Derate at $70°C \leq T_A \leq 85°C$	14.5 mW/°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

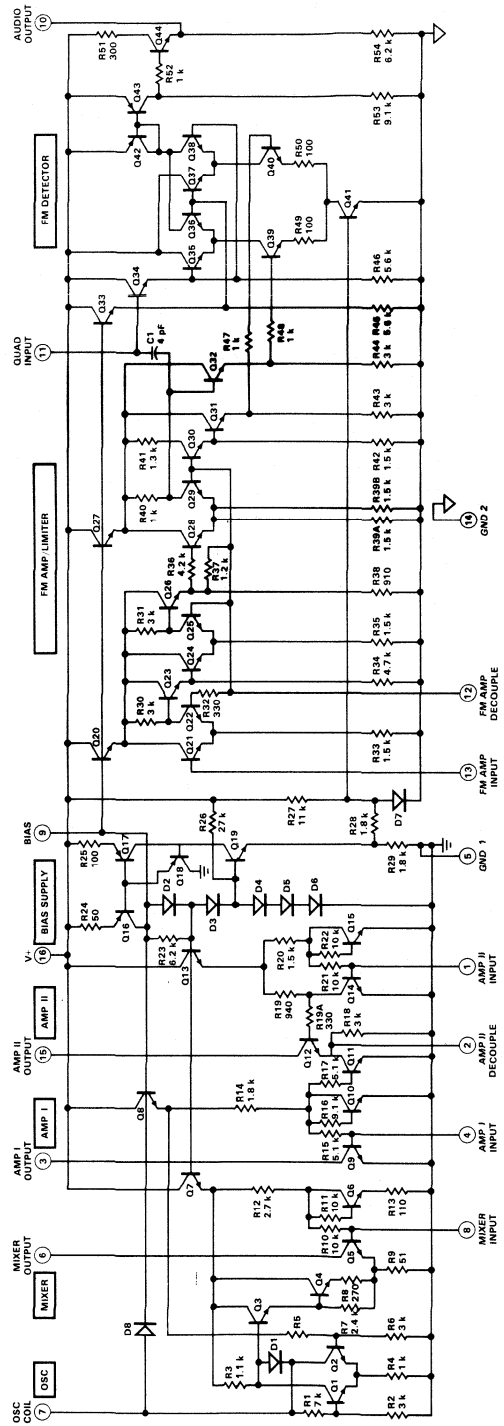
BLOCK DIAGRAM



Pin 5 GND 1
Pin 14 GND 2

*Planar is a patented Fairchild process.

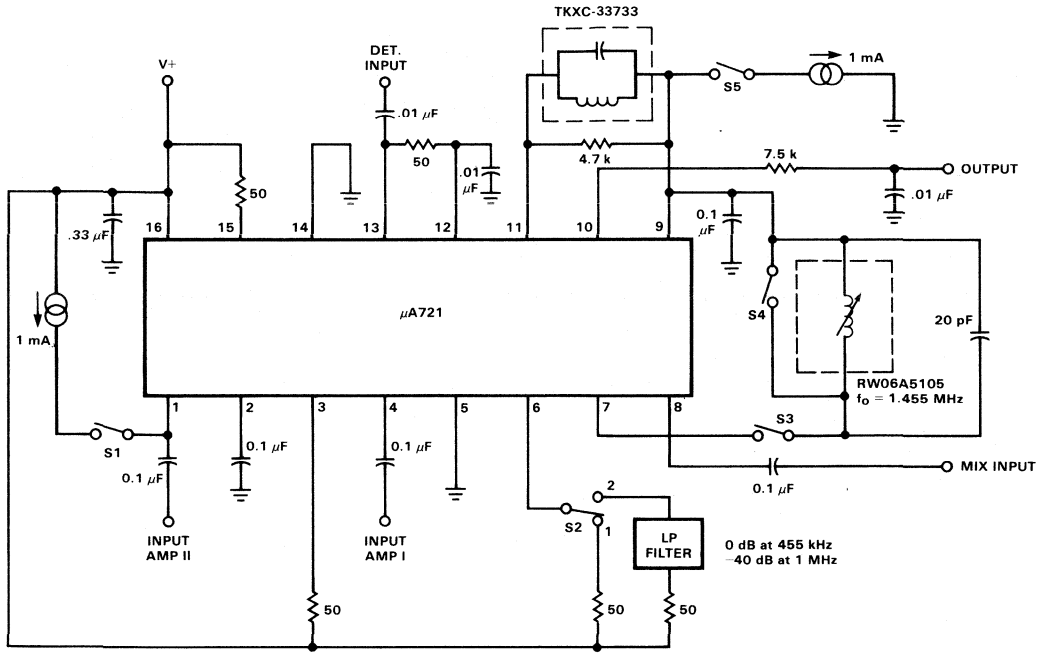
EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, V+ = 8.2 V unless otherwise specified (See Test Circuit)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
Supply Current			20	30	mA
Voltage at Pin 1		600	700	800	mV
Voltage at Pin 2		300	500	700	mV
Voltage at Pin 4		600	700	800	mV
Voltage at Pin 9	S3, S4 and S5 closed	3.0	3.3	3.6	V
Voltage at Pin 10		2.5	4.0	5.5	V
Difference (V4–V1)		–20		+20	mV
Current into Pin 3		1.5	2.2	3.0	mA
Current into Pin 6 (LOW)	S3 and S4 closed	100	300	650	μA
Current into Pin 6 (HIGH)		400	580	850	μA
Current into Pin 15		1.5	2.1	3.0	mA
Voltage at Pin 12, 13			1.3		V
AC CHARACTERISTICS					
AMP I					
Transconductance	f = 1 MHz, V_{IN} = 1.0 mV_{RMS}	40	70	100	mmhos
Transconductance	f = 10.7 MHz, V_{IN} = 1.0 mV_{RMS}	35	60	90	mmhos
Input Resistance	f = 1 MHz		2.0		kΩ
Input Capacitance	f = 1 MHz		20		pF
Output Resistance	f = 1 MHz		60		kΩ
Output Capacitance	f = 1 MHz		4.0		pF
AMP II					
Transconductance	f = 455 kHz, V_{IN} = 500 μV_{RMS}	600	1200	1700	mmhos
Transconductance	f = 10.7 MHz, V_{IN} = 500 μV_{RMS}	250	500	650	mmhos
Input Resistance	f = 1 MHz		3.5		kΩ
Input Capacitance	f = 1 MHz		20		pF
Output Resistance	f = 1 MHz		60		kΩ
Output Capacitance	f = 1 MHz		4		PF
MIXER/OSC.					
Mixer Transconductance	f = 10.7 MHz, V_{IN} = 5.0 mV_{RMS}	5.5	9.0	12.0	mmhos
Mixer Conversion Gain	f = 1.0 MHz, f_{osc} = 1.455 MHz, V_{IN} = 5 mV_{RMS}, S3 – closed, S2 – pos 2	1.2	2.2	3.2	mmhos
Oscillator Voltage	f = 1.455 MHz, S3 – closed	1.4	1.9		V_{pk-pk}
Oscillator Voltage	f = 1.455 MHz, V+ = 3.5 V, S3 – closed	1.3	1.8		V_{pk-pk}
Mixer Input Resistance	f = 1 MHz		6.5		kΩ
Mixer Input Capacitance	f = 1 MHz		7.0		pF
Mixer Output Resistance	f = 1 MHz		200		kΩ
Mixer Input Capacitance	f = 1 MHz		4.0		pF
FM LIMITER/DETECTOR					
Input limiting Sensitivity (–3.0 dB)	f = 10.7 MHz,		500	800	μV_{RMS}
Recovered Audio	f = 10.7 MHz	400	520	640	mV_{RMS}
Amplitude Mudulation Rejection	V_{IN} = 100 mV_{RMS},	40	46		dB
Total Harmonic Distortion	Deviation = ±75 kHz, f_{mod} = 400 Hz		0.9	2.0	%
Signal plus Noise to Noise Ratio		60	75		dB
Input Resistance	f = 10.7 MHz		10		kΩ
Input Capacitance	f = 10.7 MHz		8.0		pF
Output Resistance	f = 400 Hz		100		Ω

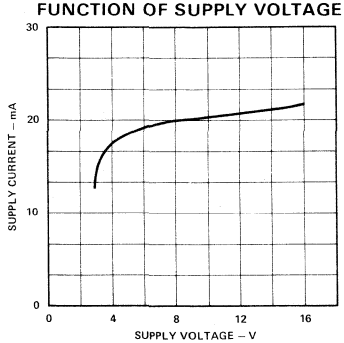
TEST CIRCUIT



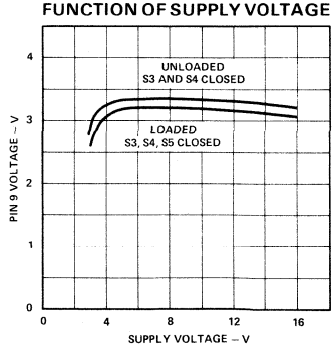
*See Applications Data for Coil Manufacturers.

TYPICAL PERFORMANCE CURVES

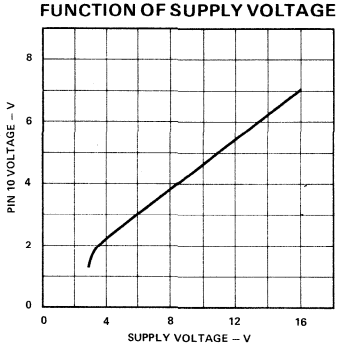
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



PIN 9 DC VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

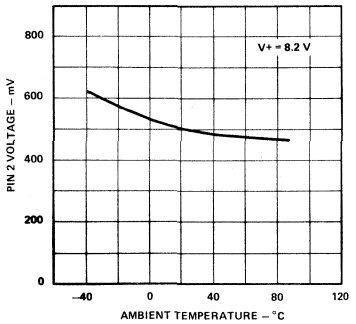


PIN 10 DC VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

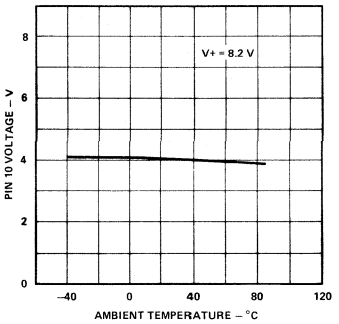


TYPICAL PERFORMANCE CURVES (Cont'd)

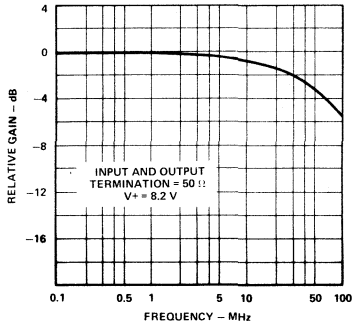
PIN 2 DC VOLTAGE AS A FUNCTION OF TEMPERATURE



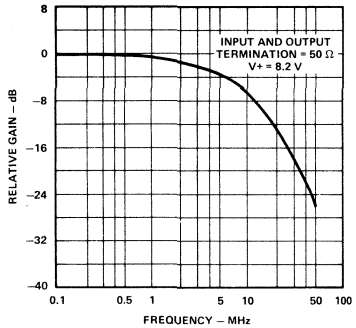
PIN 10 DC VOLTAGE AS A FUNCTION OF TEMPERATURE



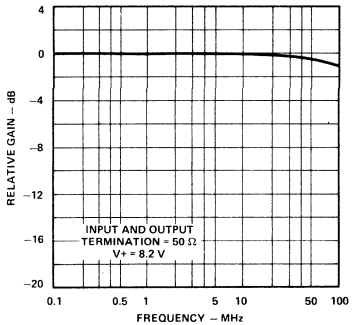
AMP I RELATIVE GAIN AS A FUNCTION OF FREQUENCY



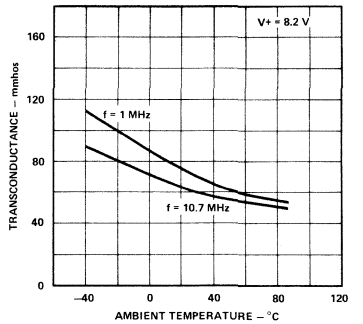
AMP II RELATIVE GAIN AS A FUNCTION OF FREQUENCY



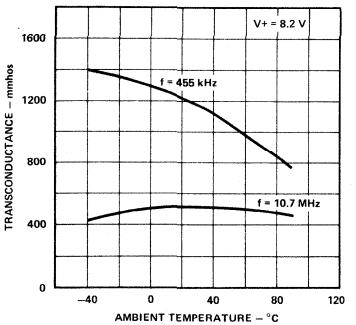
MIXER RELATIVE GAIN AS A FUNCTION OF FREQUENCY



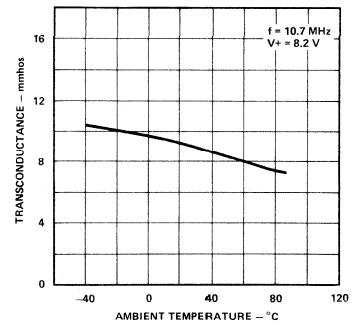
AMP I TRANSCONDUCTANCE AS A FUNCTION OF TEMPERATURE



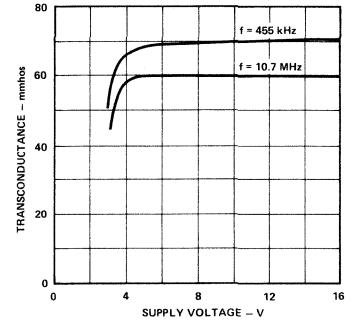
AMP II TRANSCONDUCTANCE AS A FUNCTION OF TEMPERATURE



MIXER TRANSCONDUCTANCE AS A FUNCTION OF TEMPERATURE

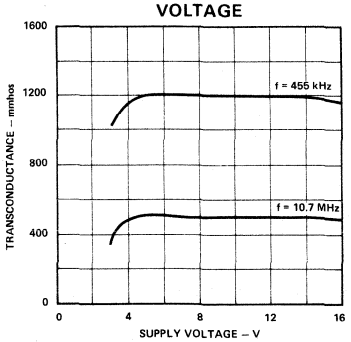


AMP I TRANSCONDUCTANCE AS A FUNCTION OF SUPPLY VOLTAGE

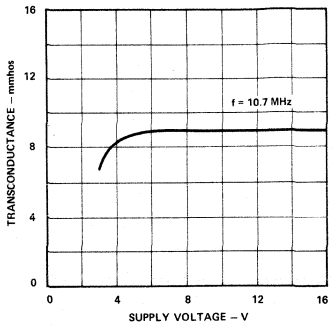


TYPCIAL PERFORMANCE CURVES (Cont'd)

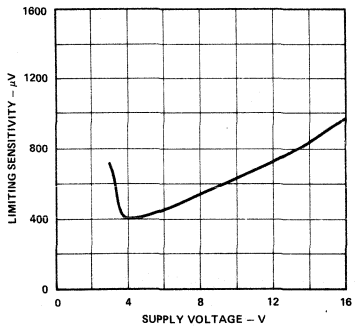
AMP II TRANSCONDUCTANCE AS A FUNCTION OF SUPPLY VOLTAGE



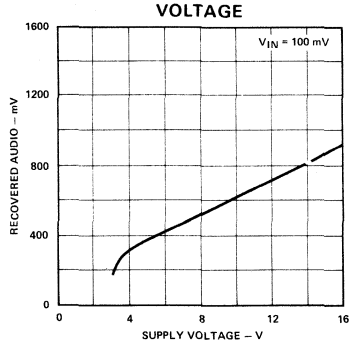
MIXER TRANSCONDUCTANCE AS A FUNCTION OF SUPPLY VOLTAGE



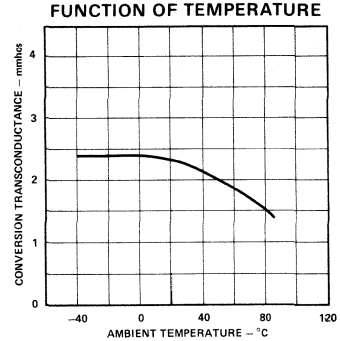
3dB LIMITING SENSITIVITY (DETECTOR) AS A FUNCTION OF SUPPLY VOLTAGE



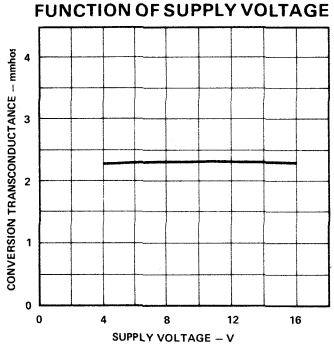
RECOVERED AUDIO (DETECTOR) AS A FUNCTION OF SUPPLY VOLTAGE



MIXER CONVERSION TRANSCONDUCTANCE AS A FUNCTION OF TEMPERATURE



MIXER CONVERSION TRANSCONDUCTANCE AS A FUNCTION OF SUPPLY VOLTAGE



APPLICATIONS INFORMATION

The independent functional blocks of the μA721 can be arranged for a variety of AM and FM receiver applications. Amplifier I, amplifier II, and the AM oscillator-mixer have open-collector output circuits which give complete flexibility for selecting load impedances. The FM IF amplifier-limiter and detector section needs only a few external components. It can be designed to be free of alignment, if ceramic filters are used for selectivity and the conventional quadrature coil replaced by a ceramic resonator. With appropriate external circuit arrangements, these four functional blocks can be combined to cover the FM IF amplification, FM detection, and all AM functions in most AM/FM receivers.

Two ground systems are used in the μA721 to minimize the chance of high frequency instability due to common ground impedances. However, for any application, care must be taken in the selection and placement of external components and in the layout of the printed circuit board to insure stable system operation.

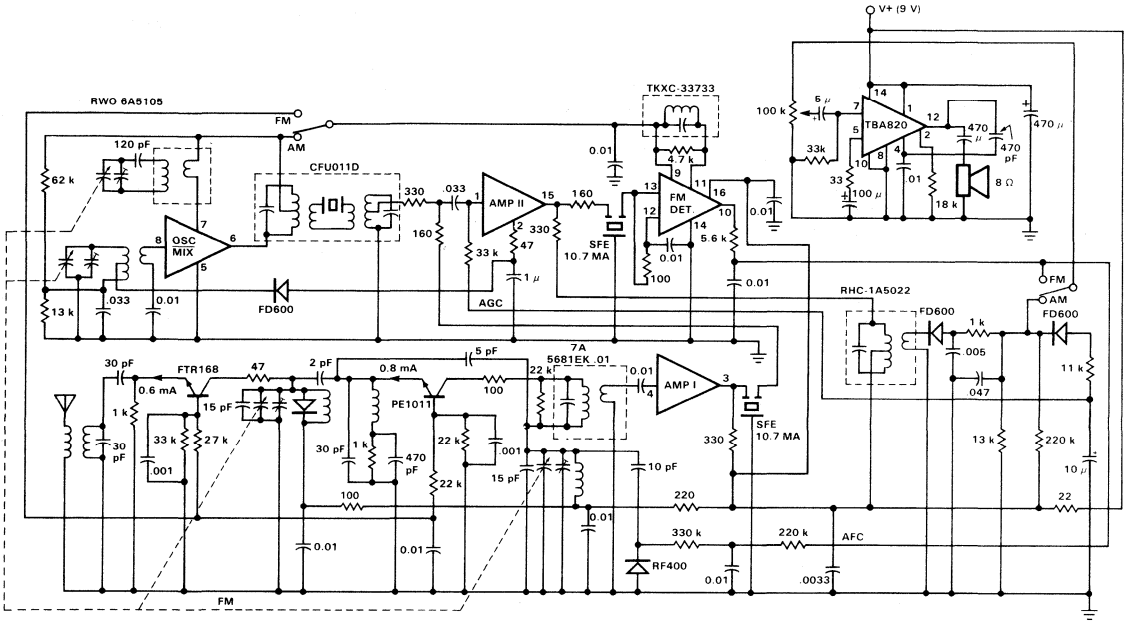
Home Radio Application – The home radio application shown in Figure 1 uses the oscillator mixer sections and amplifier II for the AM radio section. For the FM section two transistors are used for the tuner and amplifier I, II and the FM detector sections are used. Amplifier II is common for both FM and AM IF. This is accomplished without switching by paralleling the tuned circuits and ceramic filters at the input and output of amplifier II.

AGC for AM operation is applied to Pin 1 through the FD600 AGC diode. Since AGC is applied to Pin 1, the voltage at Pin 2 is proportional to the level of the incoming signal. By connecting a diode (FD600) from Pin 2 to the center tap of the antenna coil, additional AGC action is obtained as this diode conducts and reduces the Q of the antenna coils. This results in excellent overload performance.

The AFC for the FM section is applied from the Pin 10 voltage to the RF400 AFC diode. A TBA820 is used for the audio output amplifier resulting in a complete AM/FM radio using two IC's and two transistors.

Typical AM performance curves are shown in Figure 2, and the FM performance curves are shown in Figure 3. The printed circuit board layout for this circuit is shown in Figure 4.

TYPICAL AM/FM HOME RADIO



PARTS VENDOR:
Coils: Toko America Inc.: 5520 West Touhy Avenue, Skokie, Ill. 60076
Filter: Murata Corporation of America: 1148 Franklin Road, S.E. Marietta, Georgia 30067

Fig. 1

HOME RADIO PERFORMANCE AM SECTION

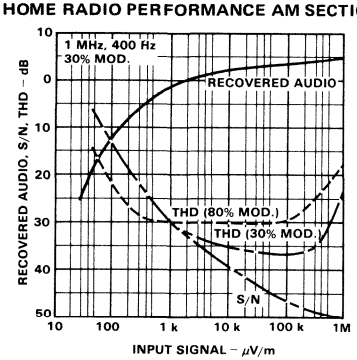


Fig. 2

HOME RADIO PERFORMANCE FM SECTION

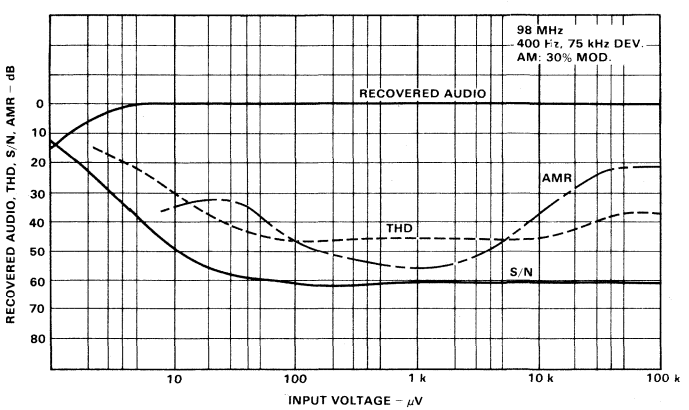


Fig. 3

μA721 HOME RADIO PC BOARD LAYOUT

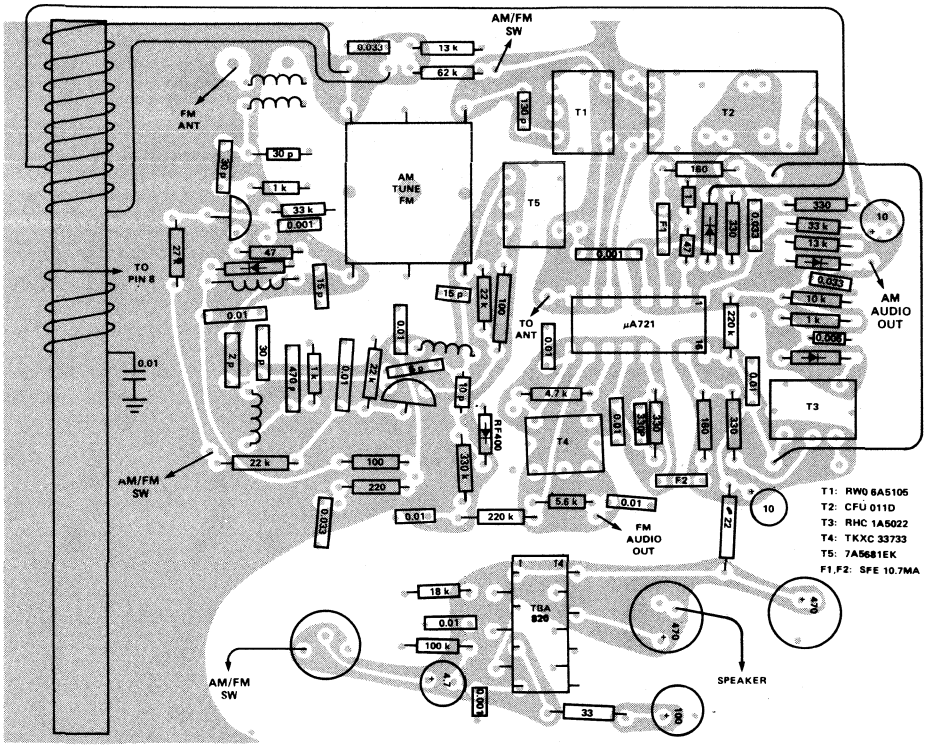


Fig. 4

Car Radio Application – The car radio application shown in Figure 5 uses amplifier I of the μA721 as the AM RF amplifier. The AM oscillator-mixer section is used as the AM converter and also as the first FM IF amplifier, when the AM oscillator is disabled. Amplifier II is used as the AM IF amplifier (which drives the separate AM detector diode) and also as the second FM IF amplifier. Additional FM IF amplification followed by FM detection is accomplished in the FM IF amplifier-limiter and detector section. High selectivity is achieved by using 262.5 kHz double-tuned coils, T1 and T2, in the AM IF amplifier, and by the two 10.7 MHz ceramic filters used in the FM IF amplifier.

AGC for AM reception is activated by the negative going voltage which is developed in the AM detector, D1, and coupled through D2. AGC action begins as D2 conducts, lowering the internally set bias voltage on Pins 1 and 4, and thereby lowering the gains in amplifiers I and II. Very large signal conditions are handled by this AGC scheme which supplies a negative bias voltage to the input of amplifier I, thus operating it in a fully cut-off mode. Distortion is kept at an acceptable level for high input signals by the RC network (62 Ω and 100 pF) connected across amplifier I.

The FM tuner front-end in the car radio application has a junction FET input stage and transistors for the oscillator and mixer stages. The AFC control voltage is derived from the FM detector output (Pin 10).

Typical AM performance curves of this radio are shown in Figures 6 and 7. FM performance curves are shown in Figure 8. The printed circuit board layout for the circuit shown in Figure 6 (exclusive of FM tuner) is shown in Figure 9.

AM/FM CAR RADIO

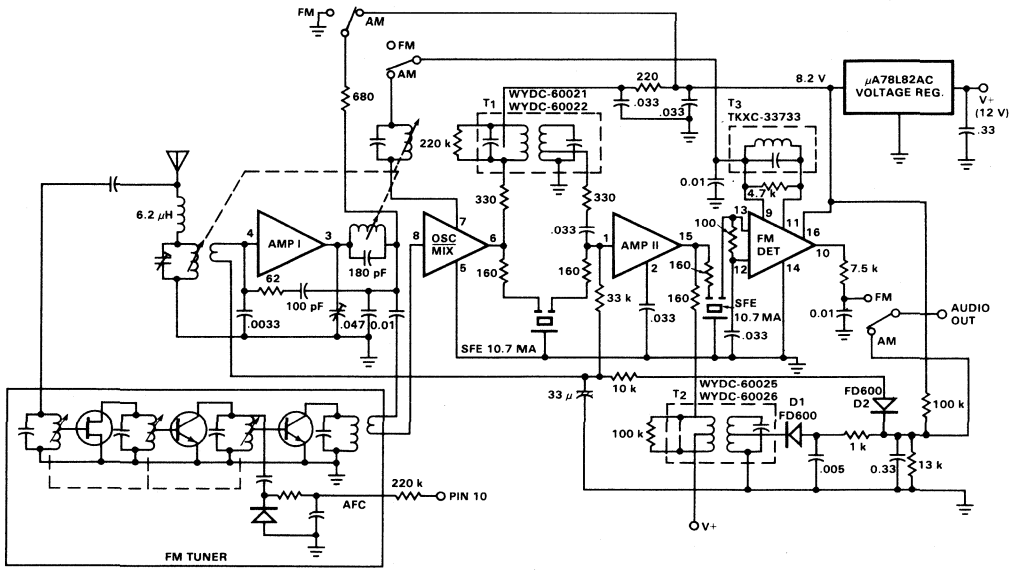


Fig. 5

PARTS VENDOR:
Coils: Toko America Inc.: 5520 West Touhy Avenue, Skokie, Ill. 60076
Filter: Murata Corporation of America: 1148 Franklin Road, S.E. Marietta, Georgia 30067

CAR RADIO PERFORMANCE AM SECTION

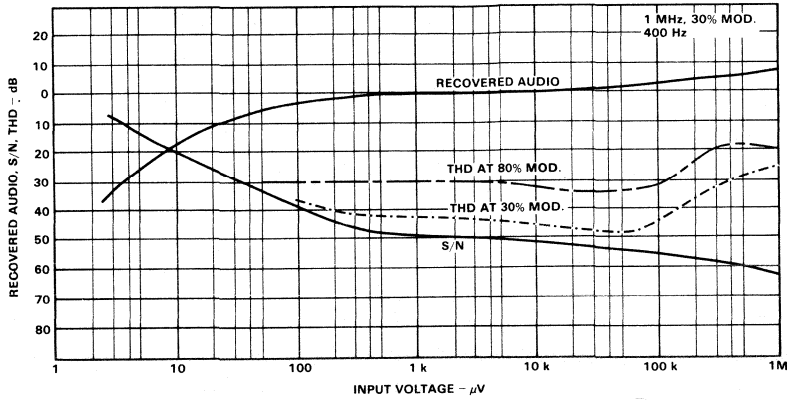


Fig. 6

CAR RADIO PERFORMANCE AM SECTION

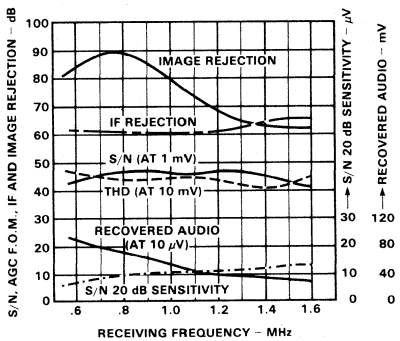


Fig. 7

CAR RADIO PERFORMANCE FM SECTION

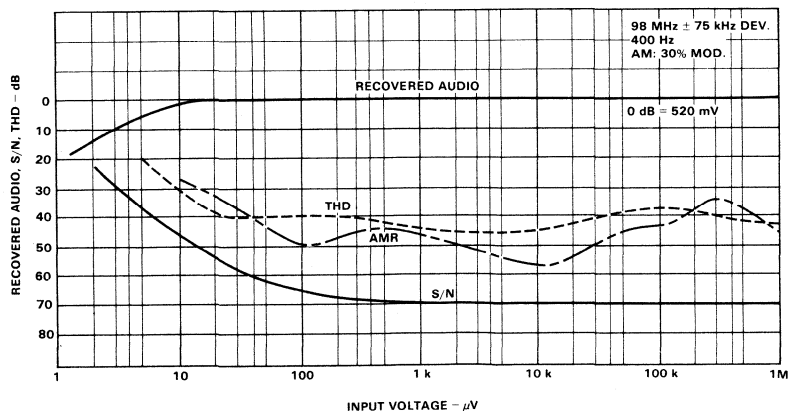


Fig. 8

μA721 CAR RADIO PC BOARD LAYOUT

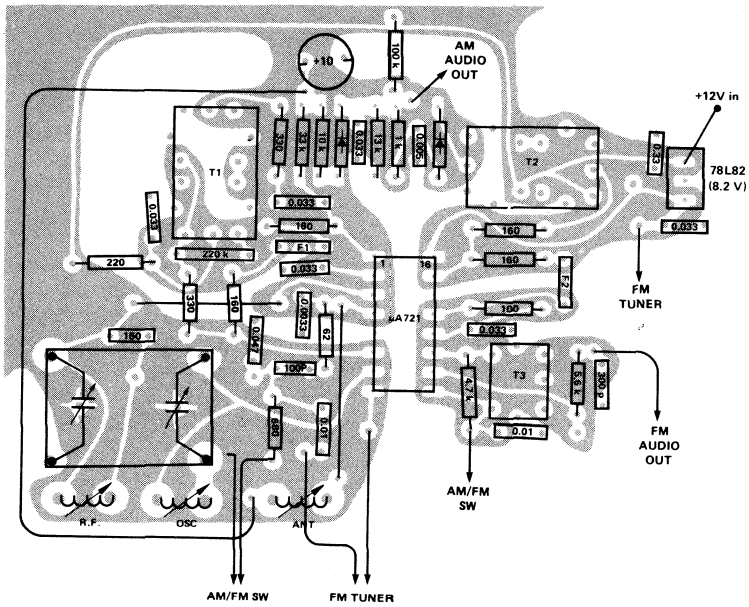


Fig. 9

μA732
FM STEREO MULTIPLEX DECODER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

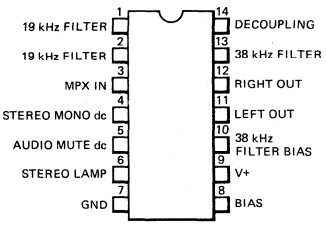
GENERAL DESCRIPTION – The μA732 is a monolithic FM Stereo Multiplex Decoder System constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This integrated circuit demodulates a stereo multiplex signal into the right and left audio channels while inherently suppressing SCA frequency components. Internal provision is made for interstation audio muting, stereo/mono mode switching and driving an external stereo mode indicator lamp. The excellent performance, wide supply range and low external parts requirement make the μA732 suitable for all line-operated and automotive FM stereo multiplex applications. See Note 1.

- **45 dB CHANNEL SEPARATION**
- **55 dB STORECAST REJECTION WITHOUT SCA FILTERS**
- **HIGH CURRENT STEREO INDICATOR LAMP DRIVER**
- **OPERATION WITH 8 V TO 14 V SUPPLIES**
- **INTERNAL STEREO SWITCHING AND AUDIO MUTING FUNCTIONS**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 2)	+15 V
Voltage at Stereo Lamp Driver Terminal	+22 V
Current into Stereo Lamp Driver (Note 3)	100 mA
Internal Power Dissipation	
Molded DIP	340 mW
Hermetic DIP	670 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	
Molded DIP	−55°C to +125°C
Hermetic DIP	−65°C to +150°C
Pin Temperature	
Molded DIP (Soldering, 10 s)	+260°C
Hermetic DIP (Soldering, 60 s)	+300°C

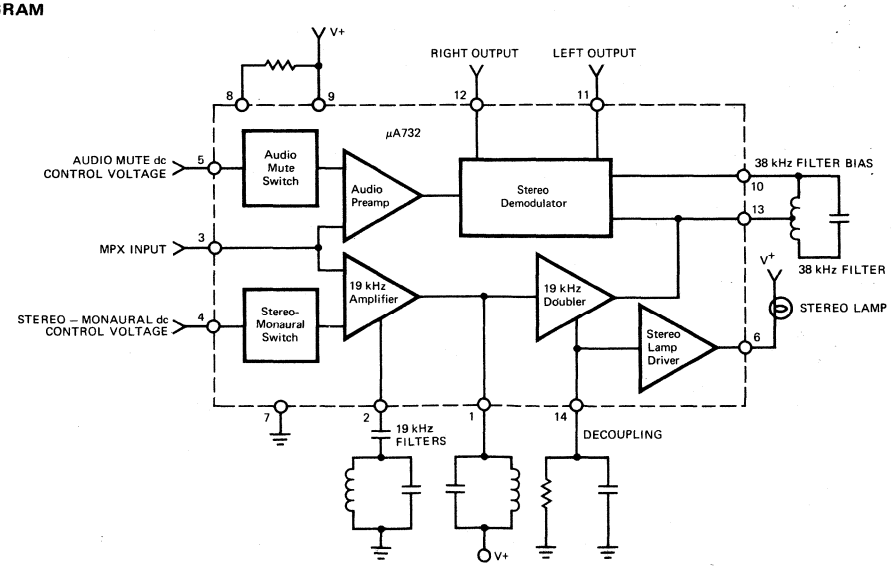
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9A
PACAKGE CODES P



ORDER INFORMATION

TYPE	PART NO.
μA732C	μA732PC

BLOCK DIAGRAM



Notes on following page.

*Planar is a patented Fairchild process.

μA732C

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, V+ = +12 V, 200 mV_{RMS} standard stereo multiplex signal applied to input, unless otherwise specified (Note 3). Refer to Test Circuit of Figure 1.

CHARACTERISTICS	MIN	TYP	MAX	UNITS
Supply Current		11	18	mA
Input Resistance	12	20		kΩ
Stereo Separation				
f = 100 Hz		40		dB
f = 1 kHz	30	45		dB
f = 10 kHz	20	40		dB
Channel Balance (Monaural Input)		0.2		dB
Total Harmonic Distortion		0.5	1.0	%
Voltage Gain		1.0		V/ V
67 kHz Storecast Rejection (Note 4)		55		dB
19 kHz Pilot Level Required at Input for:				
Stereo Indicator Lamp on		12	22	mV_{RMS}
Stereo Indicator Lamp off	4.0	8.0		mV_{RMS}
DC Voltage Required at Pin 4 for Stereo-Monaural Switching				
Stereo on	1.0	1.25	1.5	V dc
Stereo off	0.6	0.85	1.0	V dc
DC Voltage Required at Pin 5 for Audio Mute Switching				
Audio on	1.0	1.20	1.5	V dc
Audio off	0.6	0.85	1.0	V dc
Mute Attenuation of Audio	45	55		dB
High Frequency Audio Components in Left and Right Outputs (dB below 1 kHz output)				
19 kHz		30		dB
38 kHz		25		dB

NOTES:

(1) Power supply transients up to 22 V are permissible for periods of 15 seconds. However, extended operation at voltages greater than 15 V should be avoided as the maximum allowable internal power dissipation for this device may be exceeded.

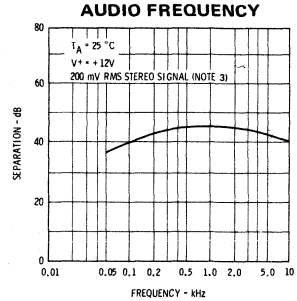
(2) Rating applies to steady state current. Maximum permissible surge current during turn-on of the Stereo Indicator Lamp is 500 mA.

(3) "Standard Stereo Multiplex Signal" here refers to a 200 mV RMS (0.56 V p-p) composite stereo signal including 10% pilot with L = 1 and R = 1 as described in the FCC Rules on FM Broadcasting.

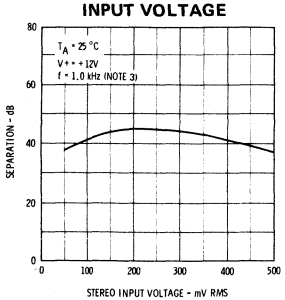
(4) Measured with a stereo composite signal consisting of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on FM Broadcasting.

TYPICAL PERFORMANCE CURVES

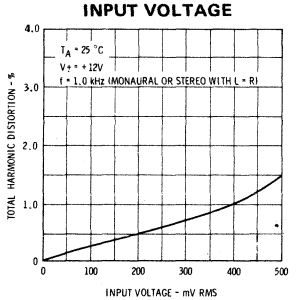
SEPARATION AS A FUNCTION OF AUDIO FREQUENCY



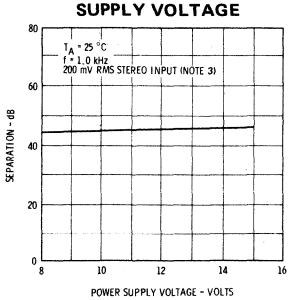
1kHz SEPARATION AS A FUNCTION OF COMPOSITE INPUT VOLTAGE



1kHz DISTORTION AS A FUNCTION OF INPUT VOLTAGE



1kHz SEPARATION AS A FUNCTION OF POWER SUPPLY VOLTAGE



FM STEREO MULTIPLEX DECODER TEST CIRCUIT AND TYPICAL APPLICATION

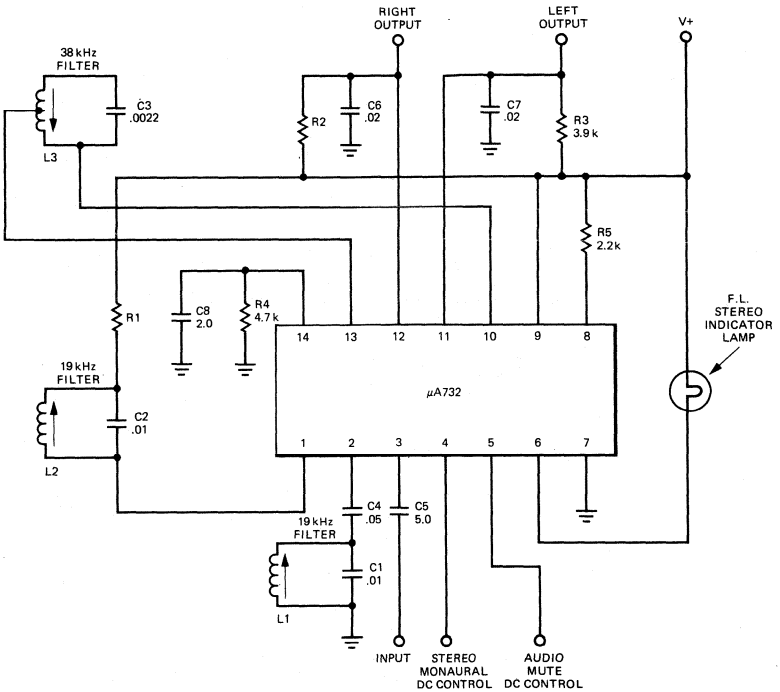


Fig. 1

NOTES:

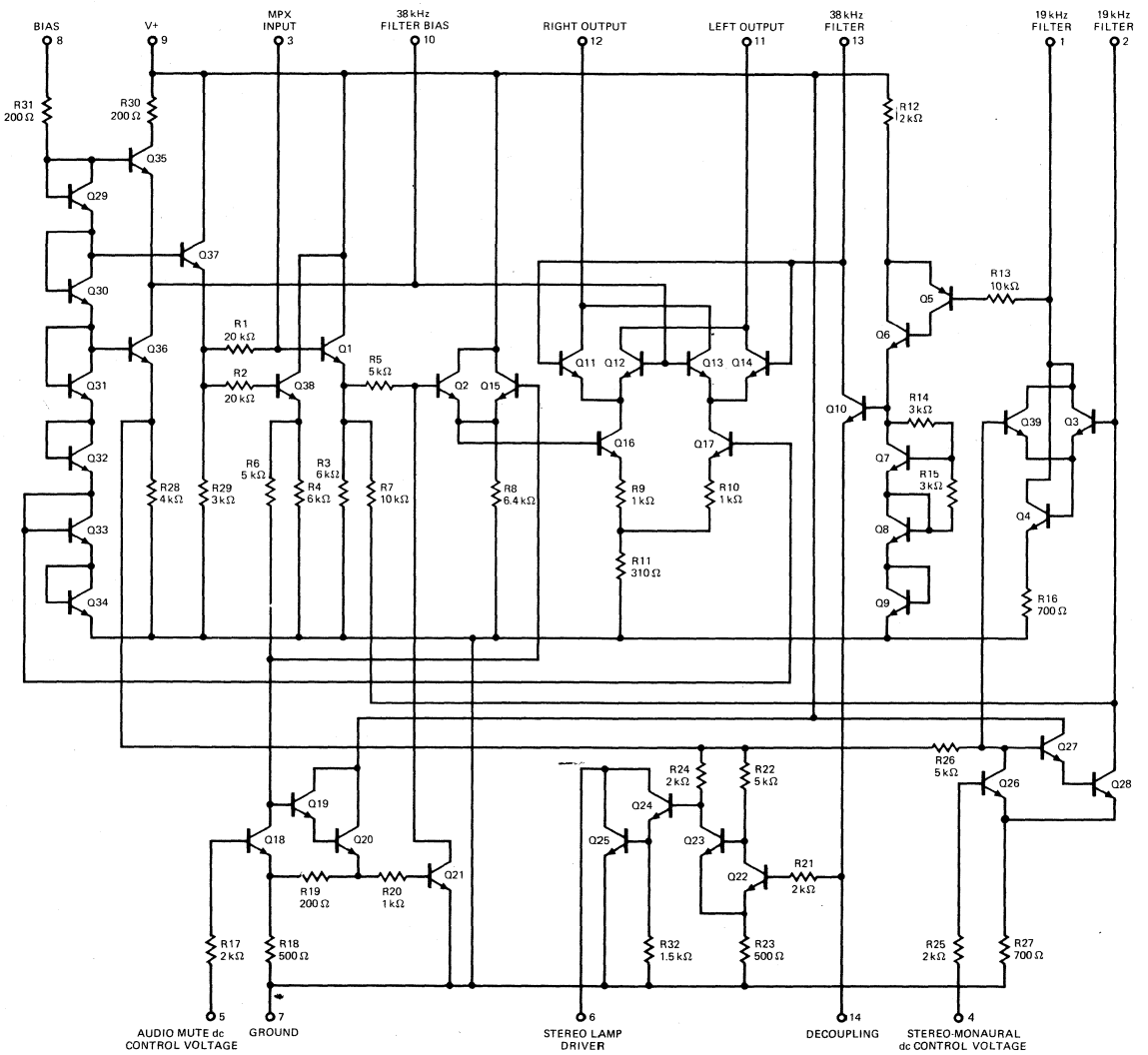
(1) Capacitors C1, C2 and C3 should be polystyrene or mylar.

(2) Coils L1 and L2 are 7.0 mH nominal with Q = 60 (Miller #1361 or equivalent).

(3) Coil L3 is 8.0 mH nominal with Q = 80, tapped at 10:1 turns ratio. (Miller #1362 or equivalent).

(4) Resistor R1 can be increased (or decreased) in value to increase (or decrease) the 19 kHz sensitivity.

FM STEREO MULTIPLEX DECODER EQUIVALENT CIRCUIT



μA739

DUAL LOW NOISE AUDIO PREAMPLIFIER/OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

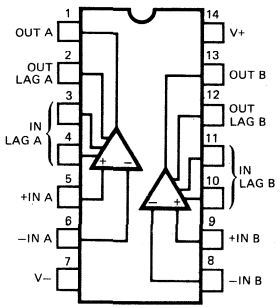
GENERAL DESCRIPTION – The μA739 consists of two identical monolithic Operational Amplifiers using the Fairchild Planar* epitaxial process. These low noise, high gain amplifiers exhibit extremely stable operating characteristics over a wide range of supply voltages and temperatures. The device is intended for a variety of applications requiring two high performance operational amplifiers.

- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW NOISE FIGURE, 2.0 dB**
- **HIGH GAIN, 20,000 V/V**
- **LARGE COMMON MODE RANGE, ±11 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	670 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Hermetic	−65°C to +150°C
Molded	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Pin Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Output Short-Circuit Duration, T_A = 25°C (Note 3)	30 seconds

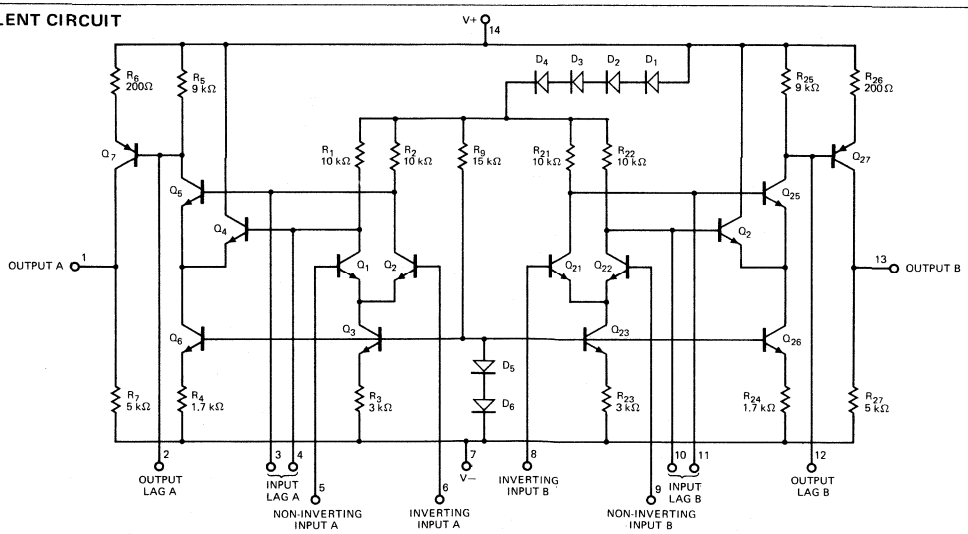
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA739C	μA739DC
μA739C	μA739PC

EQUIVALENT CIRCUIT



Notes on following page

*Planar is a patented Fairchild process.

μA739C

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15V$, $R_L = 50\ k\Omega$ to Pin 7, $T_A = 25°C$ unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300	2000	nA
Input Resistance		37	150		kΩ
Large Signal Voltage Gain	$V_{OUT} = \pm 5.0V$	6500	20,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	f = 1.0kHz		5.0		kΩ
Input Voltage Range		±10	±11		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		50		μV/V
Power Consumption	$V_{OUT} = 0$		270	420	mW
Supply Current	$V_{OUT} = 0$		9.0	14	mA
Broadband Noise Figure	$R_S = 5.0k\Omega$, BW = 10Hz to 10kHz		2.0		dB
Turn On Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20mV$		0.2		μs
Turn Off Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20mV$		0.3		μs
Slew Rate (unity gain) [See Figure 2]	$C_1 = 0.1\mu F$, $R_1 = 4.7\Omega$		1.0		V/μs
Channel Separation (See Figure 3)	$R_S \leq 10k\Omega$, f = 10kHz		140		dB
The following specifications apply for $V_S = \pm 4.0V$, $T_A = 25°C$					
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300		nA
Supply Current	$V_{OUT} = 0$		2.5		mA
Power Consumption	$V_{OUT} = 0$		20		mW
Large Signal Voltage Gain	$V_{OUT} = \pm 1.0V$	2500	15,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

NOTES:

1. Rating applies at ambient temperature below 70°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply.

PULSE RESPONSE WAVEFORMS

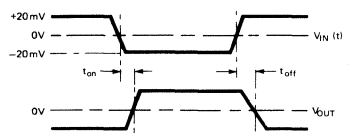


Fig. 1

FREQUENCY RESPONSE TEST CIRCUIT

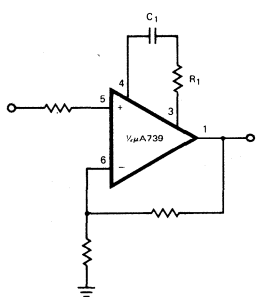


Fig. 2

CHANNEL SEPARATION TEST CIRCUIT

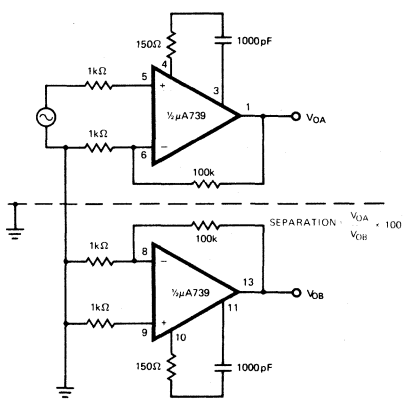
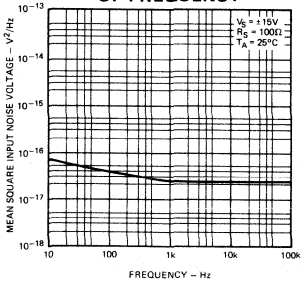


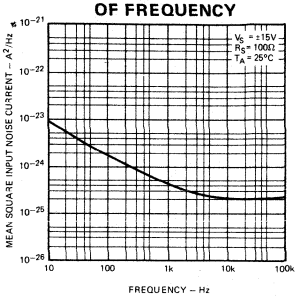
Fig. 3

TYPICAL PERFORMANCE CURVES FOR μA739C

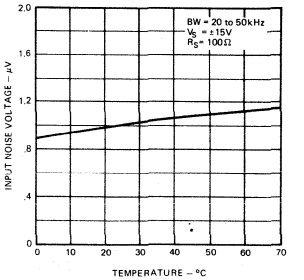
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



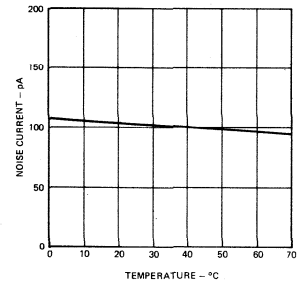
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



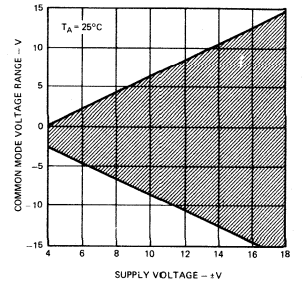
WIDE BAND INPUT NOISE VOLTAGE AS A FUNCTION OF TEMPERATURE



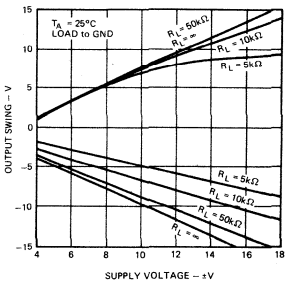
WIDE BAND INPUT NOISE CURRENT AS A FUNCTION OF TEMPERATURE



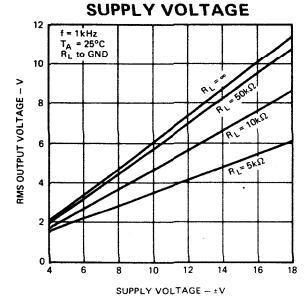
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



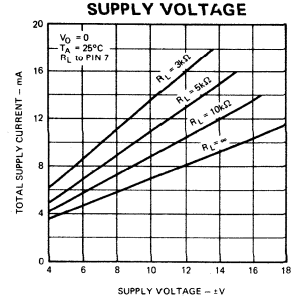
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



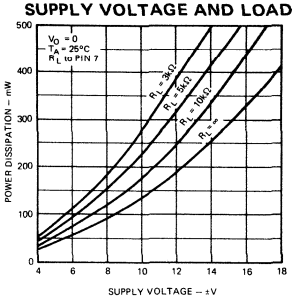
OUTPUT CAPABILITY AS A FUNCTION OF SUPPLY VOLTAGE



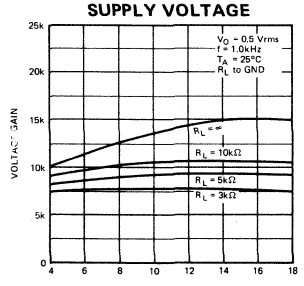
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



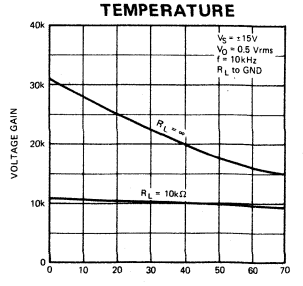
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



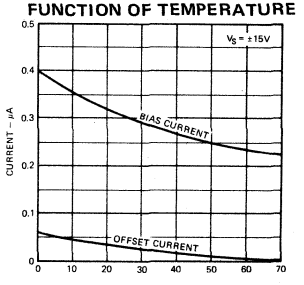
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



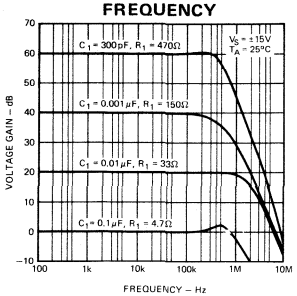
INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTION OF TEMPERATURE



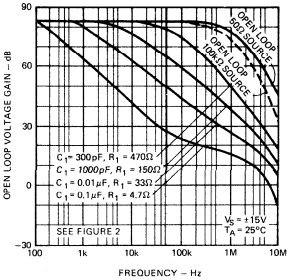
4

TYPICAL PERFORMANCE CURVES FOR μA739C

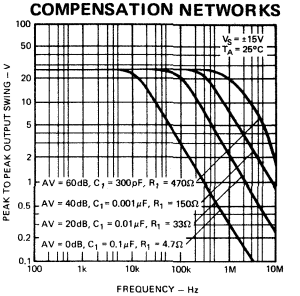
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



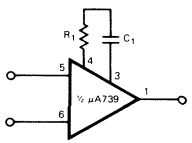
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



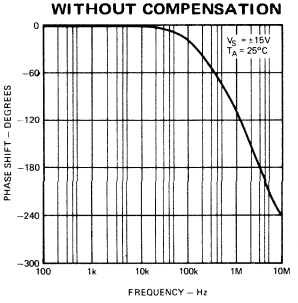
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



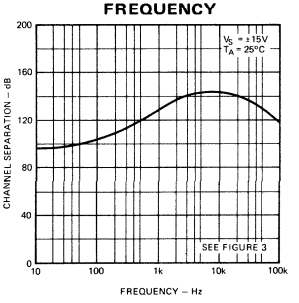
FREQUENCY COMPENSATION NETWORK



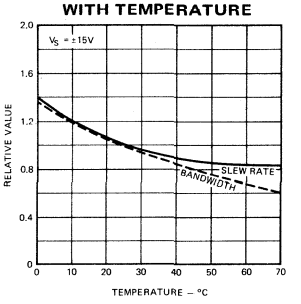
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY

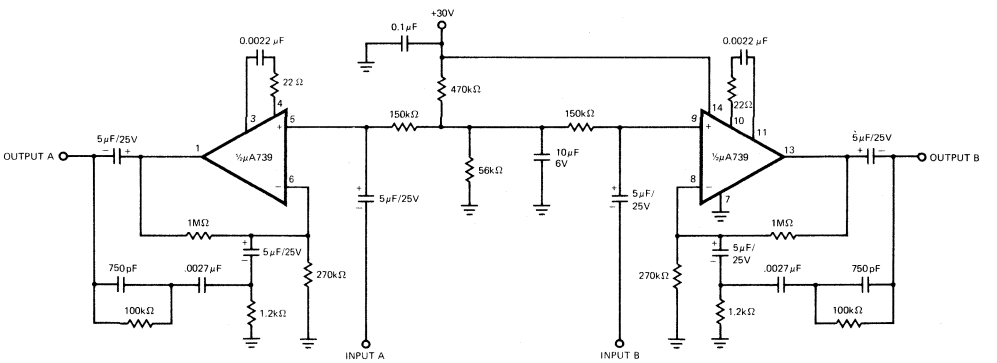


CHANGE OF AC CHARACTERISTICS WITH TEMPERATURE



TYPICAL APPLICATION

STEREO PHONO PREAMPLIFIER – RIAA EQUALIZED



TYPICAL PERFORMANCE

Gain 40dB at 1kHz, RIAA equalized
Input overload point, 80mV rms
Noise level, 2μV referred to input
Signal to noise ratio, 74dB below 10mV
Channel separation @ 1kHz, 80dB

μA742

ZERO CROSSING AC TRIGGER-TRIGAC

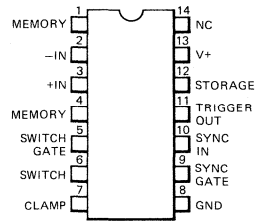
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA742 is a monolithic Zero Crossing AC Trigger (TRIGAC) utilizing the Fairchild Planar* Epitaxial Process. It is intended for use in ac power control circuits for operation directly off the ac line or with a separate ac or dc power supply. The TRIGAC functions as a threshold detector and a driver for triacs and SCR's. As a threshold detector, it senses level changes at the inputs and as a driver it supplies high energy pulses for thyristor triggering. The trigger pulses occur at the zero crossing of the load current and therefore minimize RFI generation for either resistive or inductive loads

- **DESIGNED FOR APPLICATIONS IN 60Hz TO 400 Hz AC POWER CONTROL SYSTEMS HAVING RESISTIVE OR INDUCTIVE LOADS**
- **OPERATES DIRECTLY FROM AN AC LINE OR FROM A DC SUPPLY**
- **INPUT COMPATIBLE WITH A WIDE RANGE OF SENSOR IMPEDANCES**
- **BRIDGE SENSING WITH ADJUSTABLE HYSTERESIS SET POINTS**
- **PROVISIONS FOR TIME PROPORTIONING OPERATION**
- **PROVIDES ZERO CROSSING THYRISTOR TRIGGERING FOR MINIMUM RFI**
- **EVEN NUMBER OF CONSECUTIVE HALF-CYCLE TRIGGERINGS FOR TRIACS AND INVERSE PARALLEL SCR's IN MOST APPLICATIONS**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



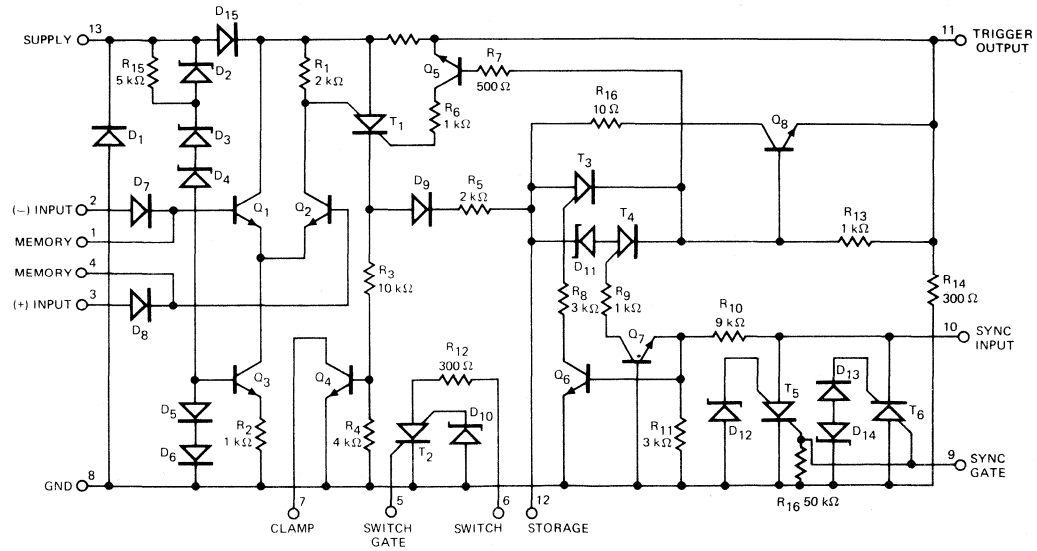
ORDER INFORMATION

TYPE	PART NO.
μA742C	μA742PC
μA742C	μA742DC

ABSOLUTE MAXIMUM RATINGS

Peak Current into Supply Terminal (ac Operation)	±30mA
Continuous Current into Supply Terminal (dc Operation)	20mA
RMS Current into Sync Input Terminal	15mA
Current into Switch Terminal	10mA
Power Dissipation	670mW
Voltage at (+) or (–) Input Terminal	(Note 1)
Differential Voltage between (+) and (–) Input Terminals	±7V
Current into Clamp Terminal (Clamp ON)	20mA
Voltage at Clamp Terminal (Clamp OFF)	25V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Pin Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Trigger Output Short-Circuit Duration (Note 2)	Continuous

EQUIVALENT CIRCUIT



Notes on following pages.

*Planar is a patented Fairchild process.

μA742C

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, Voltage Range at the (+) and (–) Input Terminals 2.5V to 17V; $V_{(+)\ Input} - V_{(-)\ Input} \geq 50mV$, Test Circuit 1, unless otherwise specified.

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Peak Supply Voltage	S_1 in dc position	19	21	26	V
	S_1 in ac position, positive half cycles of ac line	19	21	26	V
	S_1 in ac position, negative half cycle of ac line	-1.6	-0.95	-0.8	V
Peak Trigger Output Pulse	S_1 in ac position, beginning of positive half cycles	0.6	0.9		A
	S_1 in ac or dc position, beginning of negative half cycles	1.0	1.3		A
	S_1 in dc position beginning of positive half cycles	1.6	2.0		A
Bias Current at (+) and (–) Terminals			15	25	μA
Input Threshold Voltage for Output Pulse Enable		-50	-35	50	mV
ON Voltage at Clamp Terminal	$I_7 = 1$ mA		85	200	mV
ON Voltage at Switch Terminal	$I_6 = 5$ mA		2.6	3.0	V
Switching Voltage at Switch Terminal		6.0	7.2		V
Switching Current at Switch Terminal			15		μA
Holding Current at Switch Terminal			23	200	μA
ON Voltage at Sync Input Terminal	$I_{10} = 10$ mA		1.9	2.2	V
	$I_{10} = -10$ mA	-2.2	-1.9		V
Switching Voltage at Sync Input Terminal	$I_{10} = 2$ mA, positive half cycles, $V_{(-)\ Input} - V_{(+)\ Input} > 50$ mV	4.5	5.8		V
	$I_{10} = -2$ mA, negative half cycles, $V_{(-)\ Input} - V_{(+)\ Input} > 50$ mV		-7.0	-4.5	V
Sync Input Threshold Current for Trigger Output	Beginning of positive half cycles	180	410	500	μA
	Beginning of negative half cycles	-500	-280	-180	μA
Sync Input Threshold Voltage for Trigger Output	Beginning of positive half cycles	2.0	2.7	4.0	V
	Beginning of negative half cycles	-4.0	-3.3	-2.0	V

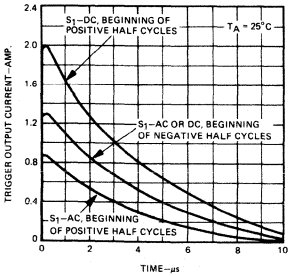
DEFINITIONS

VOLTAGE RANGE: The range of voltage on the (+) or (–) input terminals, which, if exceeded, could cause the TRIGAC to cease functioning.
BIAS CURRENT: The average of the two currents into the (+) and (–) input terminals.

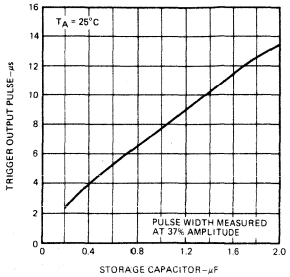
NOTES:
(1) The maximum voltage should not exceed the instantaneous supply voltage of the μA742.
(2) Rating applies for an external storage capacitor having a value of not more than 2μF.

TYPICAL PERFORMANCE CURVES FOR μA742C
(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)

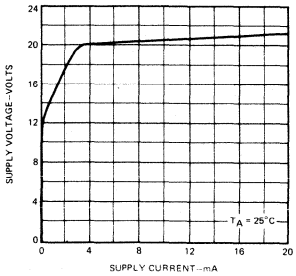
TRIGGER OUTPUT PULSE WAVE FORMS



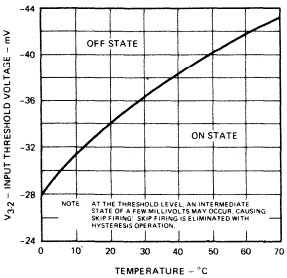
TRIGGER OUTPUT PULSE WIDTH AS A FUNCTION OF STORAGE CAPACITOR



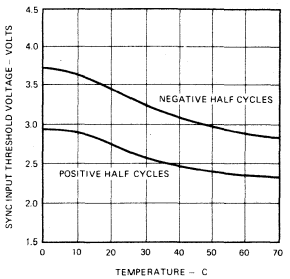
SUPPLY VOLTAGE AS A FUNCTION OF SUPPLY CURRENT



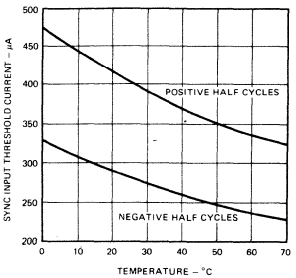
INPUT THRESHOLD VOLTAGE AS A FUNCTION OF TEMPERATURE



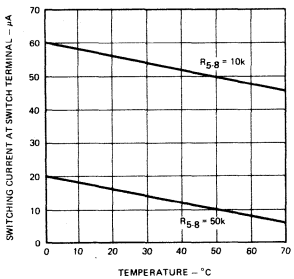
SYNC INPUT THRESHOLD VOLTAGE AS A FUNCTION OF TEMPERATURE



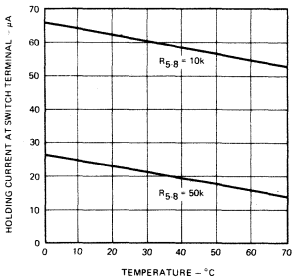
SYNC INPUT THRESHOLD CURRENT AS A FUNCTION OF TEMPERATURE



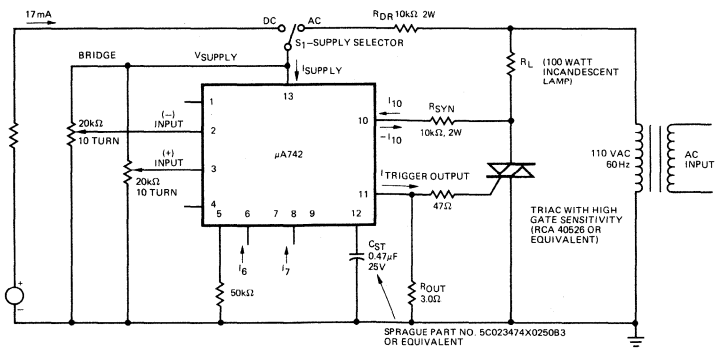
SWITCHING CURRENT AT SWITCH TERMINAL AS A FUNCTION OF TEMPERATURE



HOLDING CURRENT AT SWITCH TERMINAL AS A FUNCTION OF TEMPERATURE



TEST CIRCUIT 1



TYPICAL APPLICATIONS FOR μA742C

NOTES

*Recommended Values

AC Supply Voltage 60Hz Volts - RMS	R_{DR}	R_{SYN}	C_{ST}
24	1.0 kΩ	2.2 kΩ	0.47 μF/25V
110	10 kΩ	10 kΩ	0.47 μF/25V
220	22 kΩ	22 kΩ	0.47 μF/25V

FOR SUPPLY VOLTAGE FREQUENCY OF 400Hz REDUCE C_{ST} TO .047μF/25V.

**Necessary with inductive loads.

***The sensor resistance will determine the values of the bridge resistors. For the values of R_{DR} shown, the total current into the bridge should not exceed 5mA at 20V.

ZERO CROSSING CIRCUIT WITH DC SUPPLY

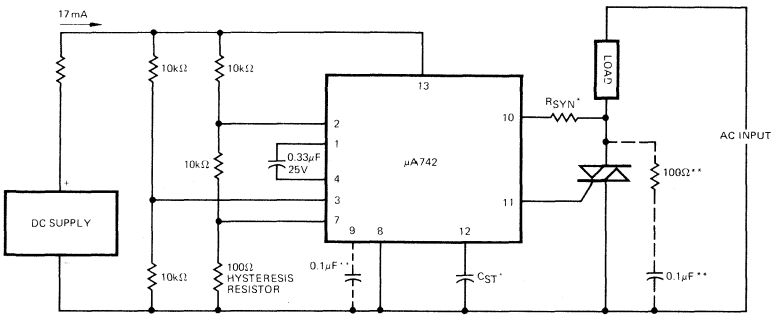


Fig. 1

ZERO CROSSING CIRCUIT

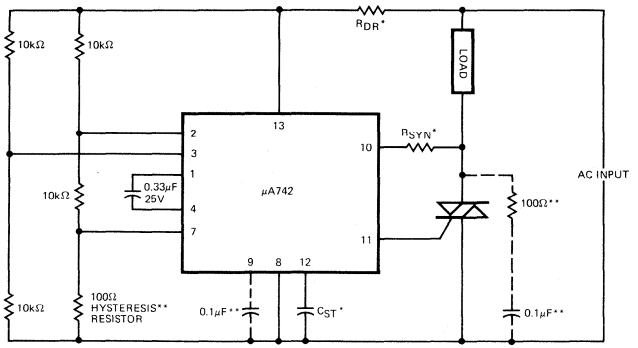


Fig. 2

TYPICAL APPLICATIONS FOR μA742 (Cont'd)

SCR – HALF WAVE

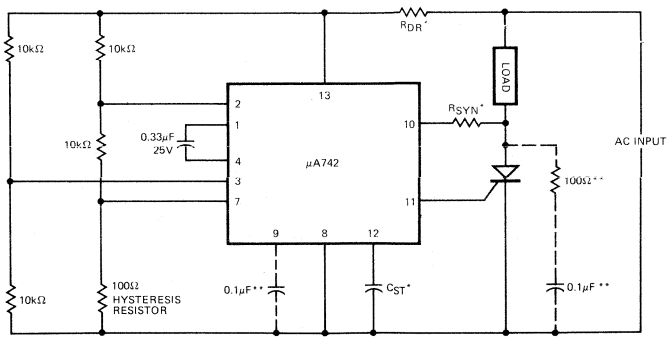


Fig. 3

INVERSE PARALLEL SCR PAIR FIRING WITH A PULSE TRANSFORMER

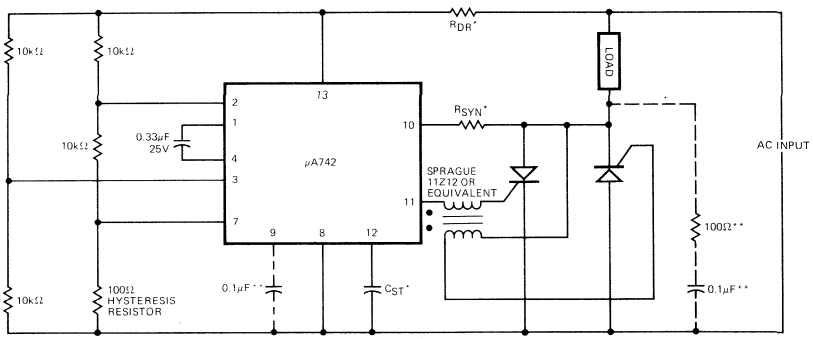


Fig. 4

INVERSE PARALLEL SCR PAIR FIRING WITH A THIRD SCR

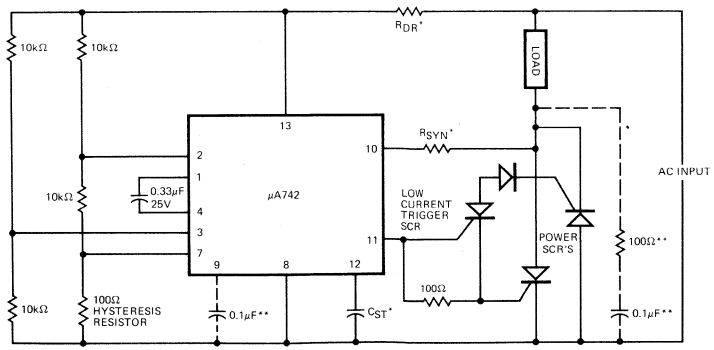


Fig. 5

TYPICAL APPLICATIONS FOR μA742 (Cont'd)

ZERO CROSSING WITH PROPORTIONAL CONTROL

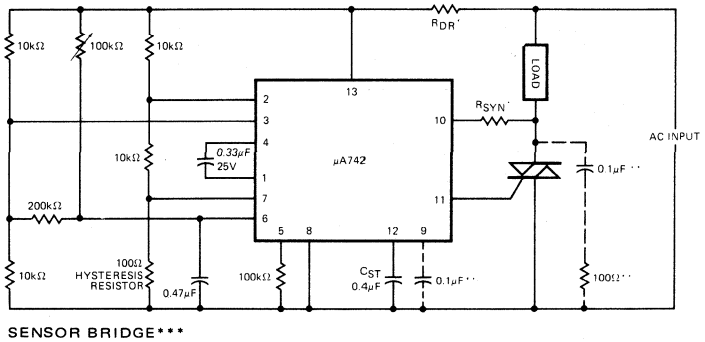


Fig. 6

ZERO CROSSING CONTROL CIRCUIT WITHOUT HYSTERESIS

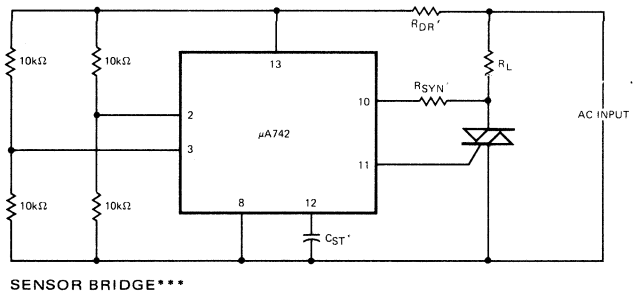


Fig. 7

μA746

CHROMA DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

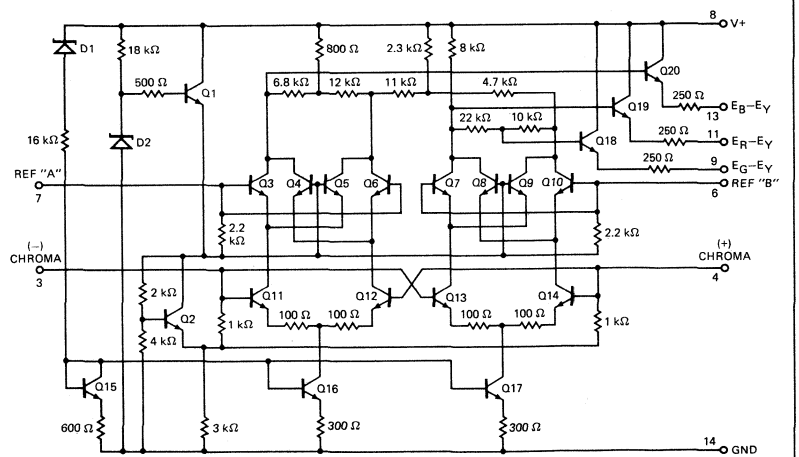
GENERAL DESCRIPTION – The μA746 is a monolithic Chroma Demodulator constructed using the Fairchild Planar* epitaxial process. This device demodulates the chroma subcarrier information contained in a color television video signal and provides color-difference signals at the outputs. The low voltage drift of the dc output insures excellent performance in direct-coupled chrominance output circuitry.

- **LOW OUTPUT VOLTAGE DRIFT WITH TEMPERATURE**
- **DOUBLY BALANCED DEMODULATION**
- ***INTERNAL COLOR-DIFFERENCE MATRIX FOR NTSC COLOR TV***
- **10 VOLT PEAK-TO-PEAK E_B-E_Y OUTPUT**

ABSOLUTE MAXIMUM RATINGS

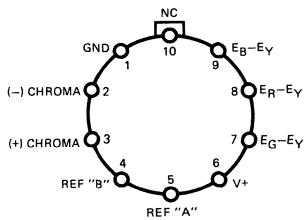
Supply Voltage	+28V
Minimum Load Resistance	3kΩ
Peak-to-Peak Reference Input Voltage	5.0V
Peak-to-Peak Chroma Input Voltage	5.0V
Internal Power Dissipation	
Metal Can	500mW
DIP	670mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	
Molded DIP	−55°C to +125°C
Metal Can and Hermetic DIP	−65°C to +150°C
Pin Temperature	
Metal Can (soldering, 60 s)	300°C
Molded DIP (soldering, 10s)	260°C

EQUIVALENT CIRCUIT



Pin numbers shown for Dual In-line Package.

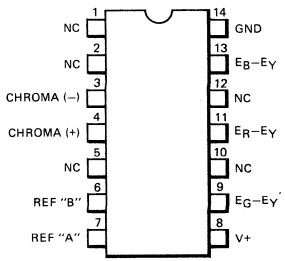
CONNECTION DIAGRAMS
10-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5Q
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA746C	μA746HC

14 PIN-DIP
(TOP VIEW)
PACKAGE OUTLINES 9A
PACKAGE CODES P



ORDER INFORMATION

TYPE	PART NO.
μA746C	μA746PC

*Planar is a patented Fairchild process.

μA746C

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, V+ = 24V, Test Circuit 1 unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	$e_C = 0$, $R_L = 1M\Omega$	5.5	9.0	12.5	mA
	$e_C = 0$, $R_L = 1M\Omega$, $T_A = 70°C$		9.0	13.0	mA
	$e_C = 0$	16.5	22	25.5	mA
	$e_C = 0$, $T_A = 70°C$		22		mA
Internal Power Dissipation	$e_C = 0$		340	430	mW
	$e_C = 0$, $T_A = 70°C$		340	445	mW
DC Voltage at any Output Terminal	$e_C = 0$	13.2	14.5	15.8	V
	$e_C = 0$, $T_A = 70°C$	13.0	14.5	16.0	V
Temperature Coefficient of DC Voltage at any Output Terminal	$e_C = 0$	−5.0	−0.3	+5.0	mV/°C
Absolute Value of DC Difference Voltage between any Two Outputs	$e_C = 0$		0.15	0.6	V
DC Voltage at either Reference Terminal	$e_A = e_B = e_C = 0$		5.8		V
DC Voltage at either Chroma Terminal	$e_C = 0$		3.2		V
Reference Input Resistance	$e_C = 0$		1.7		kΩ
Reference Input Capacitance	$e_C = 0$		6.0		pF
Chroma Input Resistance			0.8		kΩ
Chroma Input Capacitance			5.0		pF
Peak-to-Peak Chroma Input Voltage	$E_B - E_Y = 5Vp\text{-}p$		0.4	0.7	V
Peak-to-Peak $E_R - E_Y$ Output Voltage	$E_B - E_Y = 5Vp\text{-}p$	3.5	3.8	4.2	V
Peak-to-Peak $E_G - E_Y$ Output Voltage	$E_B - E_Y = 5Vp\text{-}p$	0.75	1.0	1.25	V
Maximum Peak-to-Peak $E_B - E_Y$ Output Voltage	$e_C = 1.5Vp\text{-}p$	8.0	10		V
$E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5Vp\text{-}p$		3		Degrees
$E_R - E_Y$ Demodulation Angle	$E_B - E_Y = 5Vp\text{-}p$		109		Degrees
$E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5Vp\text{-}p$		259		Degrees
$E_R - E_Y$ Demodulation Angle relative to $E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5Vp\text{-}p$	101	106	111	Degrees
$E_B - E_Y$ Demodulation Angle relative to $E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5Vp\text{-}p$	96	104	112	Degrees
Highest AC Unbalance Voltage at any Output Terminal	$e_C = 0$		0.3	0.8	$V_{p\text{-}p}$

DEFINITIONS

Color-Difference Demodulation Angle — A color-difference demodulation angle is defined as the instantaneous phase of the (+) Chroma input signal which produces the most positive voltage at the respective color-difference output with the phase of Reference "A" taken at 3 degrees and the phase of Reference "B" taken at 106 degrees.

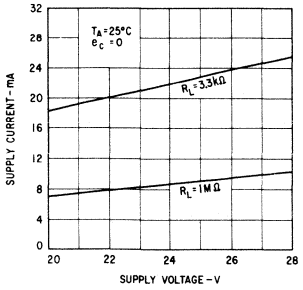
(+) Chroma Input — A composite chroma signal containing the burst at a phase of 180 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (+) Chroma input.

(—) Chroma Input — A composite chroma signal containing the burst at a phase of 0 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (—) Chroma input.

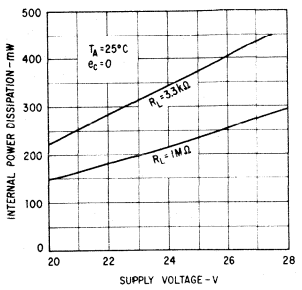
TYPICAL PERFORMANCE CURVES FOR μA746C

(Test Circuit 1 Unless Otherwise Specified)

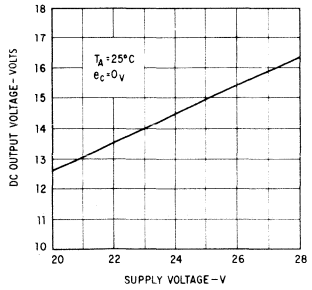
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



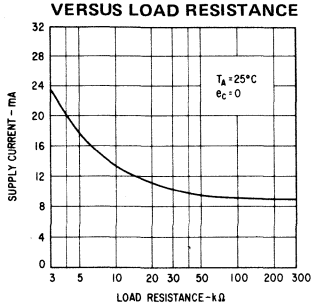
INTERNAL POWER DISSIPATION VERSUS SUPPLY VOLTAGE



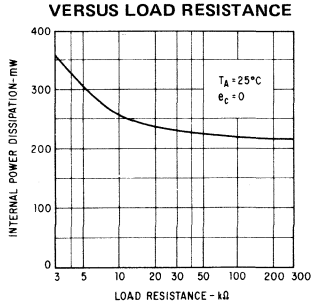
DC VOLTAGE AT ANY OUTPUT VERSUS SUPPLY VOLTAGE



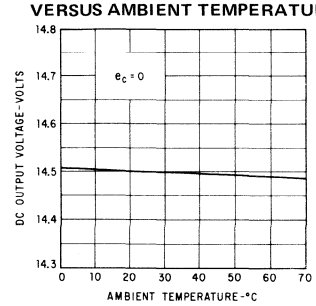
SUPPLY CURRENT VERSUS LOAD RESISTANCE



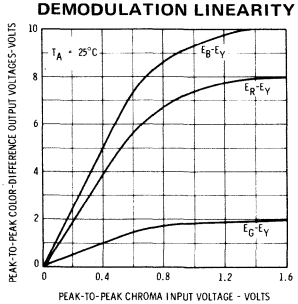
INTERNAL POWER DISSIPATION VERSUS LOAD RESISTANCE



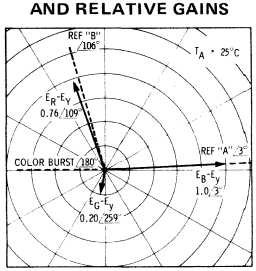
DC VOLTAGE AT ANY OUTPUT VERSUS AMBIENT TEMPERATURE



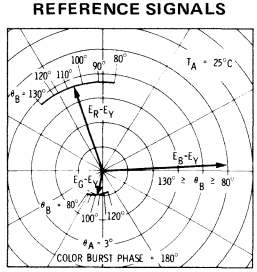
DEMODULATION LINEARITY



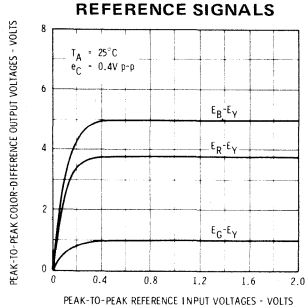
DEMODULATION ANGLES AND RELATIVE GAINS



DEMODULATION SENSITIVITY TO RELATIVE PHASING OF REFERENCE SIGNALS



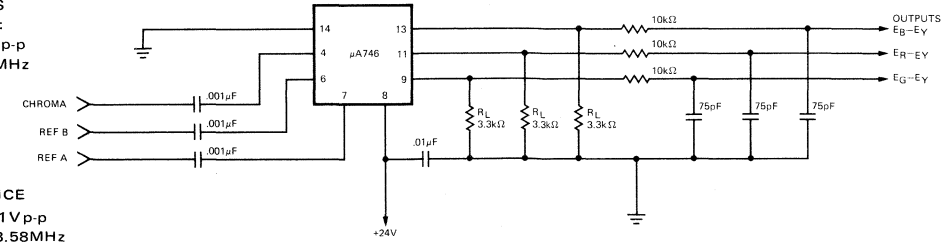
DEMODULATION SENSITIVITY TO AMPLITUDE OF REFERENCE SIGNALS



TEST CIRCUIT 1

INPUTS
CHROMA:
$e_C \leq 1.5$Vp-p
f_C = 3.59MHz

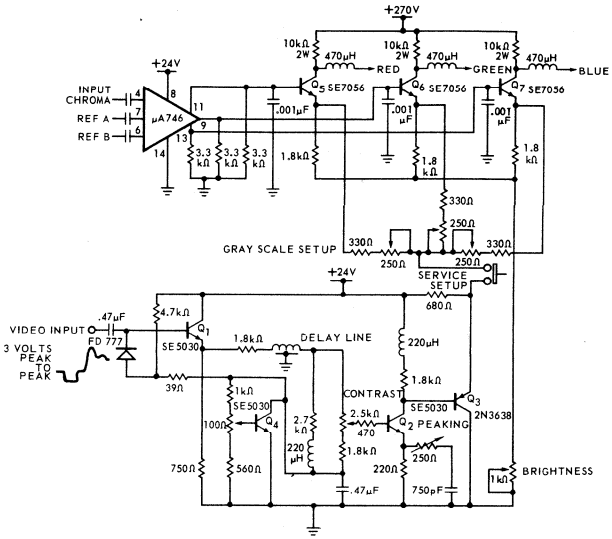
REFERENCE
$e_A = e_B$ = 1Vp-p
$f_A = f_B$ = 3.58MHz
$\theta_B = \theta_A + 103°$



Pin numbers shown for Dual In-line Package only.

TYPICAL APPLICATION

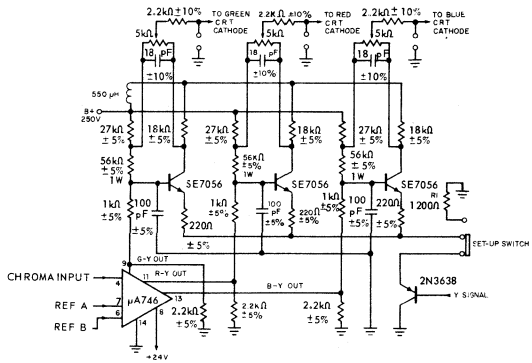
COMPLETE R-G-B VIDEO OUTPUT STAGE



Pin numbers shown for Dual In-line Package only.

Fully dc coupled circuit exhibits negligible drift with temperature, eliminates interaction between contrast and brightness controls, and minimizes gray-scale set-up time.

ALTERNATIVE R-G-B VIDEO OUTPUT STAGE



Pin numbers shown for Dual In-line Package only.

From:

"A Semiconductor Video Output Amplifier for a Red Blue Green Large Screen Color Television Receiver", by D. Poppy. IEEE Transactions on Broadcast and Television Receivers, BTR-15, #2, pp. 167-70, July 1969.

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μA749

DUAL AUDIO OPERATIONAL AMPLIFIER/AUDIO PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

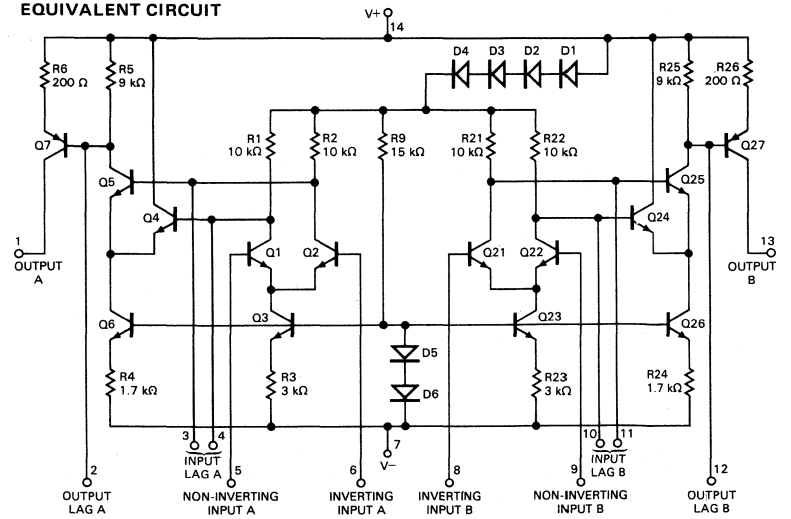
GENERAL DESCRIPTION – The μA749 consists of Two Identical High Gain Operational Amplifiers constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These three-stage amplifiers use Class A PNP transistor output stages with uncommitted collectors. This enables a variety of loads to be employed for general purpose applications from dc to 10 MHz, where two high performance operational amplifiers are required. In addition, the outputs may be wired-OR for use as a dual comparator or they may function as diodes in low threshold rectifying circuits such as absolute value amplifiers and peak detectors.

- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW POWER CONSUMPTION**
- **HIGH GAIN, 25,000 V/V**
- **LARGE COMMON MODE RANGE, +11 V, −13 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

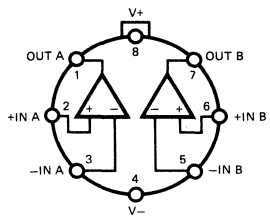
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (μA749 and μA749C)	±18 V
(μA749D)	±12 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	650 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2) (μA749 and μA749C)	±15 V
(μA749D)	±12 V
Storage Temperature Range	
Metal Can, Hermetic DIP	−65°C to +150°C
Molded DIP (μA749PC)	−55°C to +125°C
Operating Temperature Range	
Military (μA749)	−55°C to +125°C
Commercial (μA749C and μA749D)	0°C to +70°C
Pin Temperature	
Metal Can, Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Output Short-Circuit Duration, T_A = 25°C (Note 3)	30 seconds

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

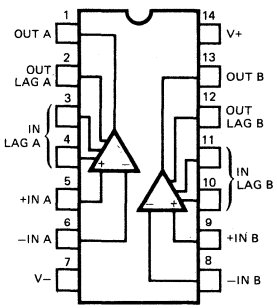


Note: Pin 4 is connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA749D	**μA749DHC**

14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA749	**μA749DM**
μA749C	**μA749DC**
μA749C	**μA749PC**

Notes on following pages.

*Planar is a patented Fairchild process.

μA749

ELECTRICAL CHARACTERISTICS: V+ = ±15 V, R_L = 5 kΩ to Pin 7, T_A = 25°C unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	R_S = 200 Ω		1.0	3.0	mV
Input Offset Current			50	400	nA
Input Bias Current			0.30	0.75	μA
Input Resistance		100	150		kΩ
Large Signal Voltage Gain	V_{OUT} = ±10 V	20,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	f = 1.0 kHz		5.0		kΩ
Common Mode Rejection Ratio	R_S = 200 Ω, V_{IN} = +11.5 V to -13.5 V	70	90		dB
Positive Supply Voltage Rejection Ratio	R_S = 200 Ω		50	200	μV/V
Negative Supply Voltage Rejection Ratio	R_S = 200 Ω		50	200	μV/V
Input Voltage Range		−13		+11	V
Internal Power Dissipation	V_{OUT} = 0		180	220	mW
Supply Current	V_{OUT} = 0		9.0	10.4	mA
Broadband Noise Figure	R_S = 10 kΩ, BW = 10 Hz to 10 kHz		2.5		dB
Turn On Delay (See Fig. 3)	Open Loop, V_{IN} = ±20 mV		0.2		μs
Turn Off Delay (See Fig. 3)	Open Loop, V_{IN} = ±20 mV		0.3		μs
Slew Rate (unity gain) (See Fig. 2)	C_1 = 0.02 μF, R_1 = 33 Ω, C_2 = 10 pF		2.0		V/μs
Channel Separation (See Fig. 4)	R_S = 1 kΩ f = 10 kHz		140		dB
The following specifications apply for V+ = ±4.0 V, R_L = 10 kΩ to Pin 7, T_A = 25°C					
Input Offset Voltage	R_S = 200 Ω		1.0	3.0	mV
Input Offset Current			50	300	nA
Input Bias Current			0.15	0.75	μA
Supply Current	V_{OUT} = 0		2.5	4.8	mA
Internal Power Dissipation	V_{OUT} = 0		20	36	mW
Large Signal Voltage Gain	V_{OUT} = ±2.0 V	20,000	60,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V
The following specifications apply for −55°C ≤ T_A ≤ +125°C, V+ = ±15 V, R_L = 5 kΩ to Pin 7:					
Large Signal Voltage Gain	V_{OUT} = ±10 V, T_A = +125°C	6,500	20,000		V/V
	V_{OUT} = ±10 V, T_A = −55°C	20,000	30,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Input Offset Voltage	R_S = 200 Ω		1.0	6.0	mV
Input Offset Current	T_A = +125°C		0.05	1.0	μA
	T_A = −55°C		0.05	1.5	μA
Input Bias Current	T_A = +125°C		0.15	0.75	μA
	T_A = −55°C		0.3	3.0	μA
Input Offset Voltage Drift	R_S = 200 Ω, +25°C ≤ T_A ≤ +125°C		3.0		μV/°C
	R_S = 200 Ω, −55°C ≤ T_A ≤ +25°C		3.0		μV/°C
Input Offset Current Drift	+25°C ≤ T_A ≤ +125°C		0.5		nA/°C
	−55°C ≤ T_A ≤ +25°C		2.0		nA/°C
Input Bias Current Drift	−55°C ≤ T_A ≤ +125°C		5.0		nA/°C
Supply Current	V_{OUT} = 0, T_A = +125°C			9.7	mA
	V_{OUT} = 0, T_A = −55°C			13	mA
Internal Power Dissipation	V_{OUT} = 0, T_A = +125°C			200	mW
	V_{OUT} = 0, T_A = −55°C			300	mW
The following specifications apply for −55°C ≤ T_A ≤ +125°C, V+ = ±4.5 V, R_l = 10 kΩ to Pin 7:					
Input Offset Voltage	R_S = 200 Ω		1.5	6.0	mV
Input Offset Current			50	750	nA
Large Signal Voltage Gain	V_{OUT} = ±2.0 V, T_A = +125°C	5,000			V/V
	V_{OUT} = ±2.0 V, T_A = −55°C	20,000			V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 8.3 mW/°C for the DIP.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply.

μA749C

ELECTRICAL CHARACTERISTICS: V+ = ±15 V, R_L = 5 kΩ to Pin 7, T_A = 25°C unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	R_S = 200 Ω		1.0	6.0	mV
Input Offset Current			50	750	nA
Input Bias Current			0.30	1.5	μA
Input Resistance		50	150		kΩ
Large Signal Voltage Gain	V_{OUT} = ±10 V	15,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	f = 1.0 kHz		5.0		kΩ
Common Mode Rejection Ratio	R_S = 200 Ω, V_{IN} = +11.5 V to −13.5 V	70	90		dB
Positive Supply Voltage Rejection Ratio	R_S = 200 Ω		50	350	μV/V
Negative Supply Voltage Rejection Ratio	R_S = 200 Ω		50	200	μV/V
Input Voltage Range		−13		+11	V
Internal Power Dissipation	V_{OUT} = 0		180	330	mW
Supply Current	V_{OUT} = 0		9.0	14	mA
Broadband Noise Figure	R_S = 10 kΩ, BW = 10 Hz to 10 kHz		2.5		dB
Turn On Delay (See Fig. 3)	Open Loop, V_{IN} = ±20 mV		0.2		μs
Turn Off Delay (See Fig. 3)	Open Loop, V_{IN} = ±20 mV		0.3		μs
Slew Rate (unity gain) (See Fig. 2)	C_1 = 0.02 μF, R_1 = 33 Ω, C_2 = 10 pF		1.0		V/μs
Channel Separation (See Fig. 4)	R_S = 1 kΩ, f = 10 kHz		140		dB

The following specifications apply for V+ = ±4.0 V, R_L = 10 kΩ to Pin 7, T_A = 25°C:

Input Offset Voltage	R_S = 200 Ω		1.0	6.0	mV
Input Offset Current			50	600	nA
Input Bias Current			0.3	1.5	μA
Supply Current	V_{OUT} = 0		2.5		mA
Internal Power Dissipation	V_{OUT} = 0		20		mW
Large Signal Voltage Gain	V_{OUT} = ±2.0 V	15,000	60,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

The following specifications apply for 0°C ≤ T_A ≤ +70°C, V+ = ±15 V, R_L = 5 kΩ to Pin 7:

Large Signal Voltage Gain	V_{OUT} = ±10 V, T_A = +70°C	8,000	40,000		V/V
	V_{OUT} = ±10 V, T_A = 0°C	15,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Input Offset Voltage	R_S = 200 Ω		1.0	9.0	mV
Input Offset Current			0.05	1.5	μA
Input Bias Current			0.3	3.0	μA
Input Offset Voltage Drift	R_S = 200 Ω, +25°C ≤ T_A ≤ +70°C		3.0		μV/°C
	R_S = 200 Ω, 0°C ≤ T_A ≤ +25°C		3.0		μV/°C
Input Offset Current Drift	+25°C ≤ T_A ≤ +70°C		0.5		nA/°C
	0°C ≤ T_A ≤ +25°C		2.0		nA/°C
Input Bias Current Drift	0°C ≤ T_A ≤ +70°C		4.0		nA/°C

The following specifications apply for 0°C ≤ T_A ≤ +70°C, V+ = ±4 V, R_L = 10 kΩ to Pin 7:

Input Offset Voltage	R_S = 200 Ω		1.5	9.0	mV
Input Offset Current			0.05	1.0	μA
Large Signal Voltage Gain	V_{OUT} = ±2.0 V, T_A = 70°C	8,000			V/V
Large Signal Voltage Gain	V_{OUT} = ±2.0 V, T_A = 0°C	15,000			V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

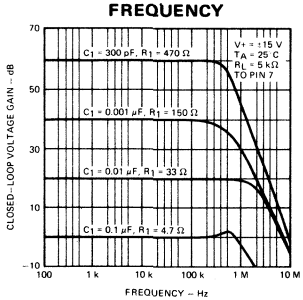
μA749D

ELECTRICAL CHARACTERISTICS: V+ = ±6 V, R_L = 10 kΩ to Pin 4, T_A = 25°C unless otherwise specified

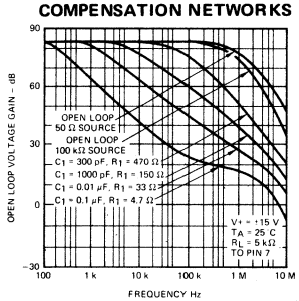
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	10	mV
Input Offset Current			50	600	nA
Input Bias Current			300	1500	nA
Input Resistance		50	150		kΩ
Large Signal Voltage Gain	V_{OUT} = ±4.0 V	10,000	20,000		V/V
Positive Output Voltage Swing		+4.5	+5.0		V
Negative Output Voltage Swing		−5.5	−6.0		V
Output Resistance	f = 1.0 kHz		10		kΩ
Input Voltage Range		−4.0		+2.5	V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		50	100	μV/V
Power Consumption (including load)	V_{OUT} = 0	24	36	54	mW
Supply Current (including load)	V_{OUT} = 0	2.0	3.0	4.5	mA
Turn On Delay (See Figure 5)	Open Loop, V_{IN} = ±20 mV, R_L = 5 kΩ		0.2		μs
Turn Off Delay (See Figure 5)	Open Loop, V_{IN} = ±20 mV, R_L = 5 kΩ		0.3		μs
Channel Separation (See Figure 7)	$R_S \leq 10$ kΩ, f = 10 kHz		140		dB

TYPICAL PERFORMANCE CURVES FOR μA749 AND μA749C

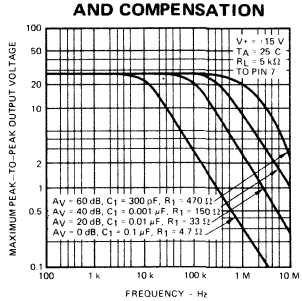
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



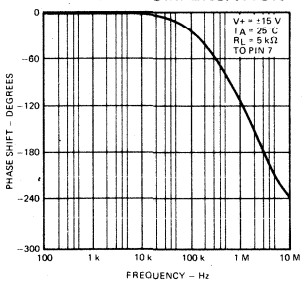
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



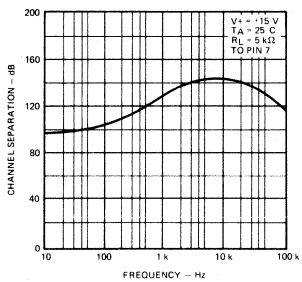
OUTPUT CAPABILITY AS A FUNCTION OF FREQUENCY AND COMPENSATION



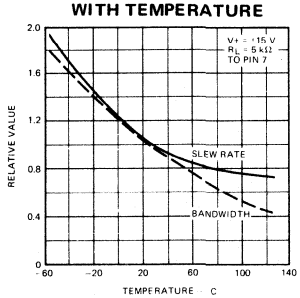
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY

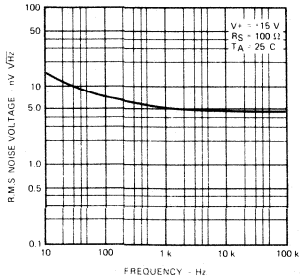


CHANGE OF AC CHARACTERISTICS WITH TEMPERATURE

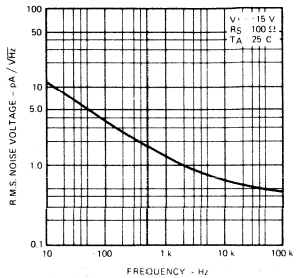


TYPICAL PERFORMANCE CURVES FOR μA749 AND μA749C

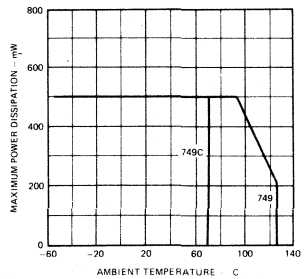
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



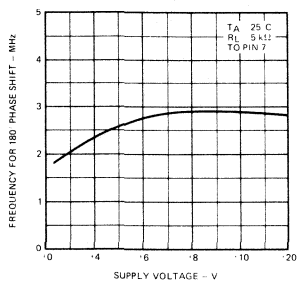
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



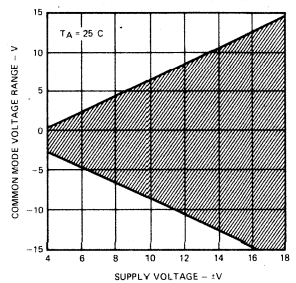
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



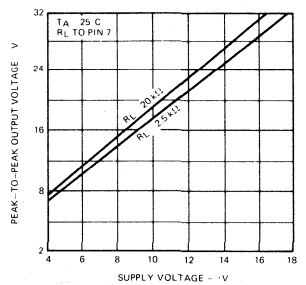
OPEN LOOP 180° PHASE SHIFT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



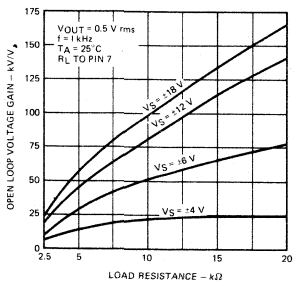
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



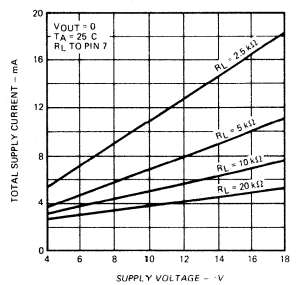
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



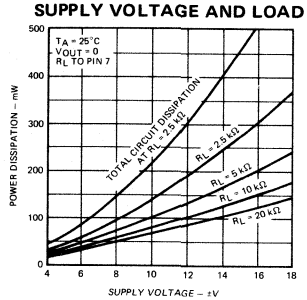
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



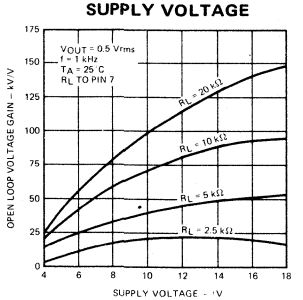
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



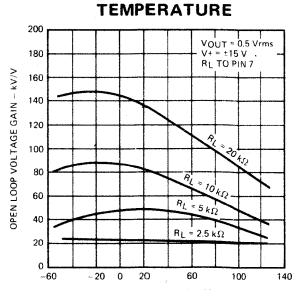
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



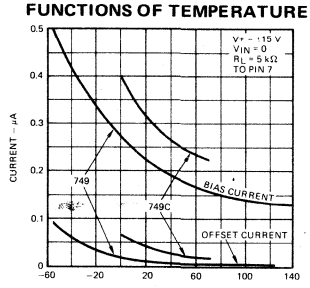
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE

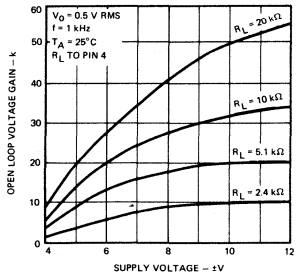


INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTIONS OF TEMPERATURE

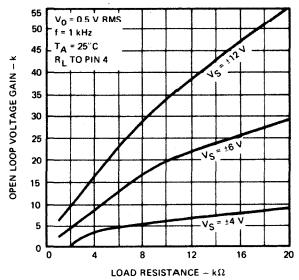


TYPICAL PERFORMANCE CURVES FOR μA749D

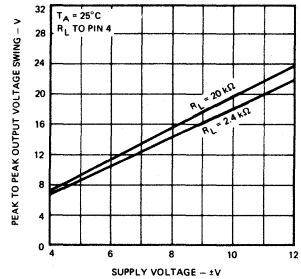
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



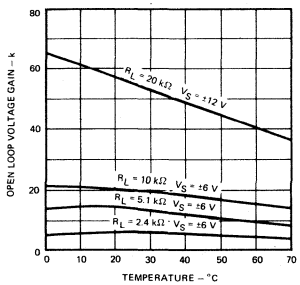
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



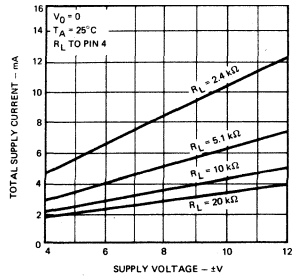
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



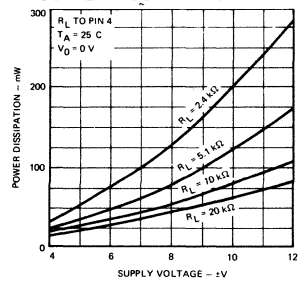
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



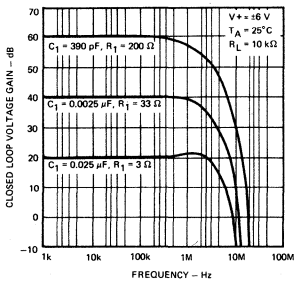
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



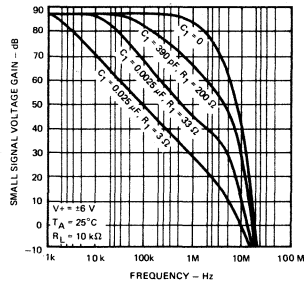
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



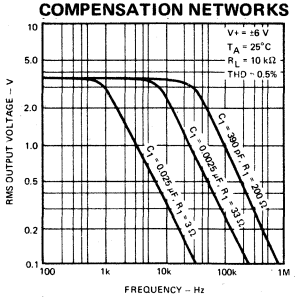
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



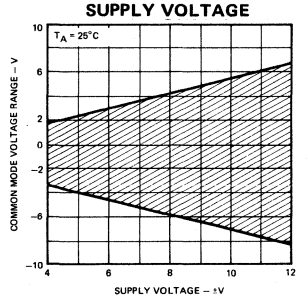
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OFFSET NULL* NETWORK μA749 AND μA749C

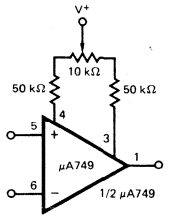


Fig. 1

FREQUENCY RESPONSE* TEST CIRCUIT μA749 AND μA749C

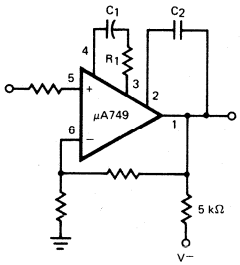


Fig. 2

PULSE RESPONSE WAVEFORMS μA749 AND μA749C

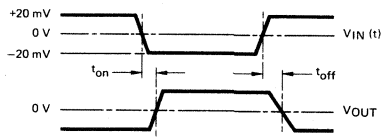


Fig. 3

CHANNEL SEPARATION* TEST CIRCUIT μA749 AND μA749C

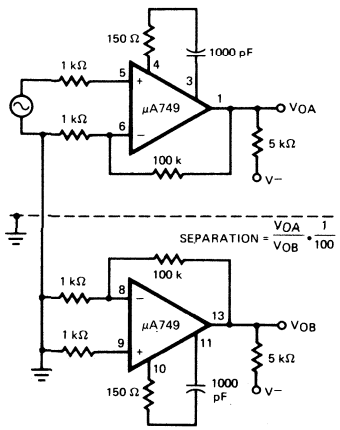


Fig. 4

PULSE RESPONSE WAVEFORMS μA749D

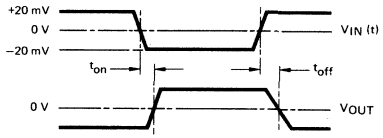


Fig. 5

FREQUENCY RESPONSE TEST CIRCUIT μA749D

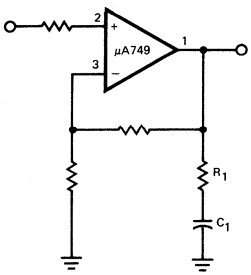


Fig. 6

CHANNEL SEPARATION TEST CIRCUIT μA749D

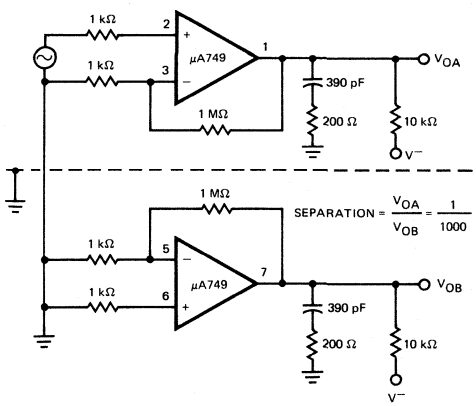
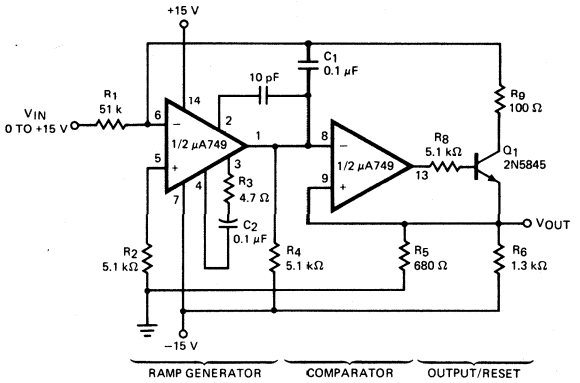


Fig. 7

*Pin numbers refer to Dual-in-line Package

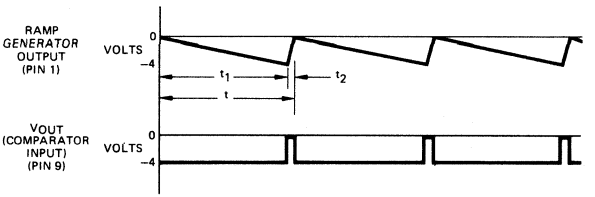
TYPICAL APPLICATIONS

VOLTAGE TO FREQUENCY CONVERTER



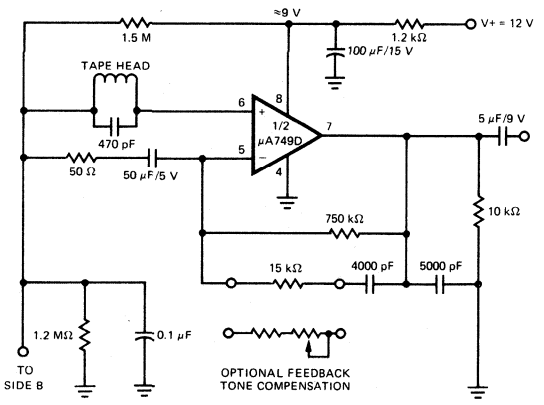
$R^* = R$ pin 1 + R9 + R_{CE} Q1 + R6 output stage.

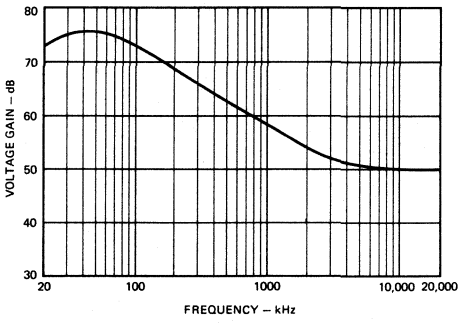
WAVEFORMS



$$t = t1 + t2 = 4\,\frac{R1\,C1}{V_{IN}} + \frac{4R^*\,C1}{15}$$

STEREO TAPE PREAMPLIFIER





TYPICAL PERFORMANCE

Gain at 1 kHz	60 dB
Output Voltage Swing	2.8 V rms
Power Consumption	30 mW

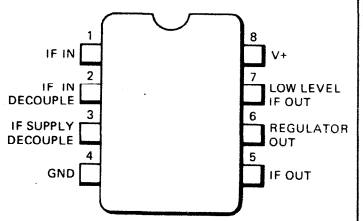
μA753
FM GAIN BLOCK
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA753 is a high performance monolithic FM Gain Block using the Fairchild Planar* epitaxial process. The FM gain block consists of a three stage direct coupled amplifier with 330Ω input and output terminations and the 7 pF shunting capacitance required for a 10.7 MHz FM IF strip utilizing commercially available ceramic filters. Included on the chip is a 7.8 V active regulator providing up to 10 mA of current to an external load such as an FM tuner.

The μA753 features full temperature compensation for the IF amplifier and the 7.8 V regulator. Excellent power supply rejection eliminates the need for an external regulated supply. An output from the second stage of the IF amplifier provides a means of external gain control without affecting the input or output terminations. The device is packaged in an 8-lead mini DIP.

- **50 dB VOLTAGE GAIN AT 10.7 MHz**
- **330Ω INPUT AND OUTPUT TERMINATIONS**
- **OPTIMIZED GAIN VS TEMPERATURE CHARACTERISTICS**
- **TEMPERATURE COMPENSATED 7.8 V ACTIVE REGULATOR PROVIDING UP TO 10 mA OF CURRENT**
- **SHORT CIRCUIT PROTECTION FOR ALL EXTERNAL CONNECTIONS**

CONNECTION DIAGRAM
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage at any terminal must not exceed V^+

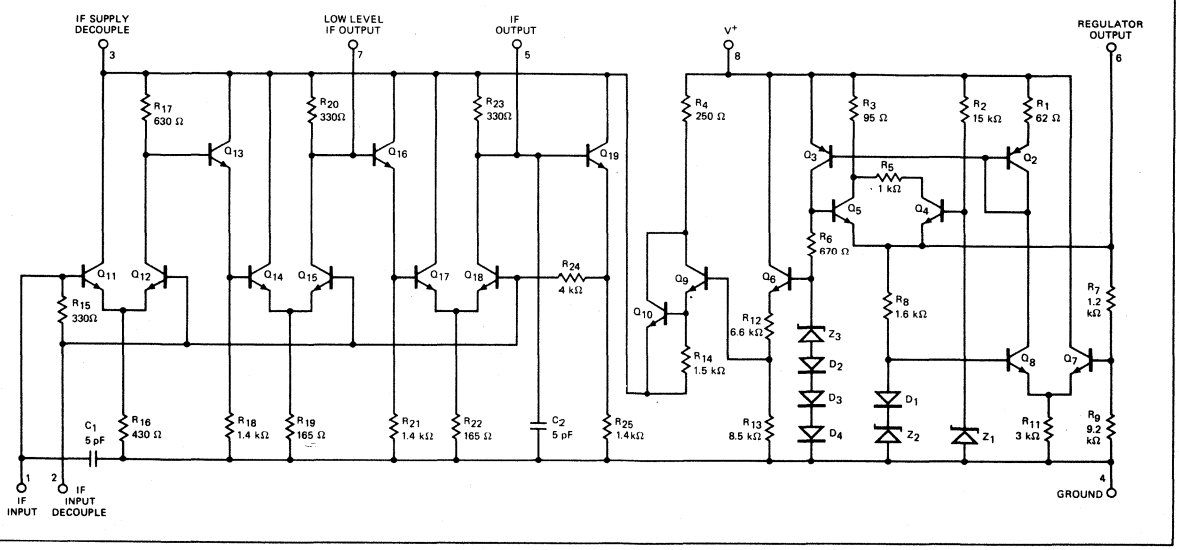
Supply Voltage (V^+)	18 V
Power Dissipation (P_D) (Note 1)	430 mW
Input Voltage (Pins 1 and 3)	±3 V
Regulator Output Current (I_{REG})	10 mA
Regulator Short Circuit Duration	Indefinite
Operating Temperature Range (T_A)	-40°C to +85°C
Storage Temperature Range (T_{STG})	-55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

Notes: 1. Rating applies for ambient temperatures to 70°C. Above 70°C derate linearly at 6.3 mW/°C

ORDER INFORMATION

TYPE	PART NO.
μA753C	μA753TC

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

μA753C

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_+ = +12$ V unless otherwise specified

CHARACTERISTICS	CONDITION	TEST CIRCUIT FIG. NO.	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Voltage Operating Range		3	10		16	V
Supply Current	$R_L = \infty$	3	11	16	19	mA
Power Dissipation	$R_L = \infty$	3		190	230	mW
	$I_L = 5$ mA	3		210	255	mW
Terminal Voltages	$I_L = 5$ mA	3				
Pin 1, 2				1.4		V
3				2.6		V
5				2.0		V
6			7.2	7.8	8.3	V
7				2.0		V
AC CHARACTERISTICS IF AMPLIFIER ($f_0 = 10.7$ MHz)						
−3 dB Limiting Threshold		1		900		μV
Output Voltage Swing	$V_{IN} = 100$ mV, $R_L = \infty$	1	1.1	1.4		V_{p-p}
Voltage Gain	$V_{OUT} = 100$ mV	1	40	50	56	dB
Voltage Gain Change	$-40°C \leq T_A \leq +25°C$	1		6.0		dB
	$+25°C \leq T_A \leq 85°C$	1		1.0		dB
Input Impedance:	Pin 1 to Pin 2					
Parallel Input Resistance			230	330	440	Ω
Parallel Input Capacitance				5.0	9.0	14	pF
Output Impedance:	Pin 5 to ground					
Parallel Output Resistance			230	330	440	Ω
Parallel Output Capacitance				5.0	9.0	14	pF
Output Noise Voltage		2		5.0		mV_{RMS}
AC CHARACTERISTICS REGULATOR SECTION						
Line Regulation (V_6)	$I_L = 5$ mA, $V^+ = 10$ V to 16 V	3		3.0	30	mV
Load Regulation (V_6)	$I_L = 0$ to 5 mA	3		−10		mV
Temperature Coefficient (V_6)	$I_L = 5$ mA, $-40°C \leq T_A \leq +85°C$	3		−0.15		mV/°C

TEST CIRCUIT FOR DYNAMIC CHARACTERISTICS

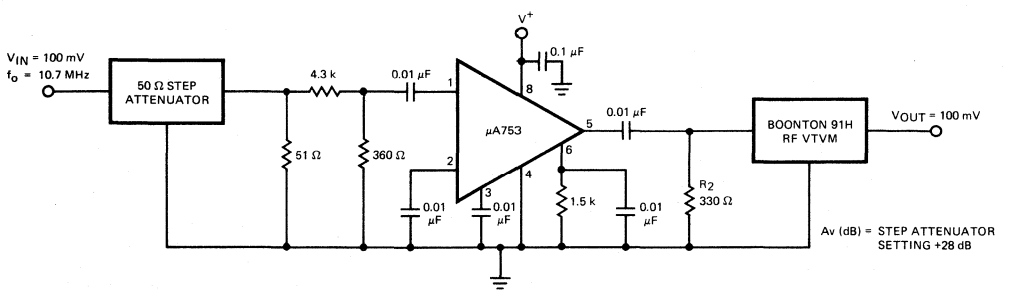


Fig. 1

NOISE MEASUREMENT TEST CIRCUIT

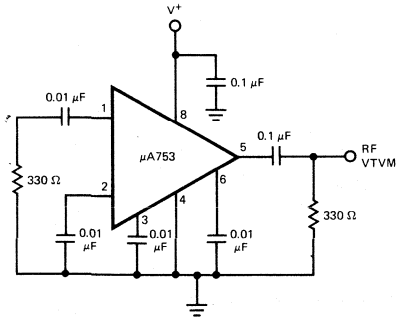


Fig. 2

TEST CIRCUIT STATIC CHARACTERISTICS

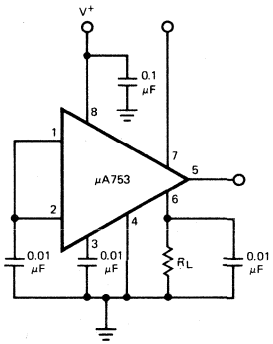
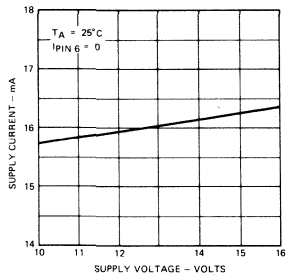


Fig. 3

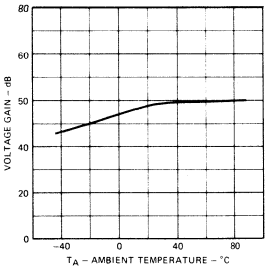
4

TYPICAL PERFORMANCE CURVES

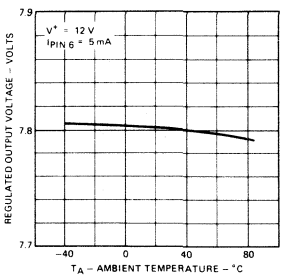
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



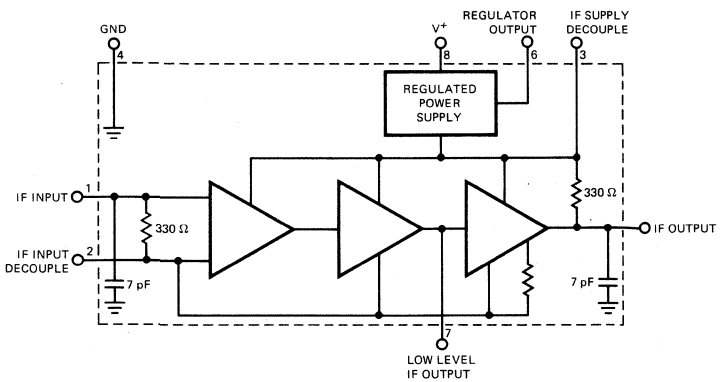
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



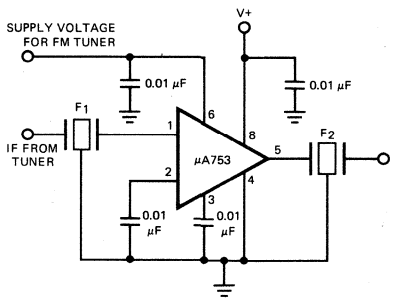
REGULATOR OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



BLOCK DIAGRAM



TYPICAL APPLICATION



F_1 AND F_2: VERNITRON FM4 OR EQUIVALENT
10.7 MHz CERAMIC FILTER

μA757

GAIN CONTROLLED IF AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

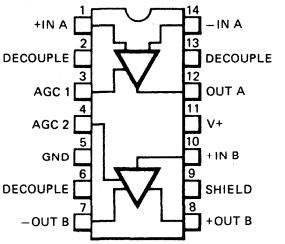
GENERAL DESCRIPTION – The μA757 is a monolithic high performance, Gain Controlled IF Amplifier constructed using the Fairchild Planar* epitaxial process. The amplifier contains two sections which may be operated independently, or in cascade, from audio frequencies to 25 MHz. The μA757 is intended primarily as a gain controlled, intermediate frequency amplifier in AM and FM communications receivers. It also has excellent performance when operated in FM receivers as a limiting amplifier.

- **70 dB GAIN AT 10.7 MHz**
- **70 dB AGC RANGE AT 10.7 MHz**
- **300 mV SIGNAL HANDLING CAPABILITY AT INPUT**
- **CONSTANT INPUT AND OUTPUT IMPEDANCE WITH AGC**
- **STABLE GAIN WITH SUPPLY VOLTAGE AND TEMPERATURE AT ALL LEVELS OF GAIN REDUCTION.**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+15V
Voltage at any Output Terminal	+24V
Voltage at either AGC Terminal (Note 1)	±12V
Differential Voltage at either Input (Pins 1 and 14, Pins 2 and 10)	±5V
Internal Power Dissipation (Note 2)	670 mW
Storage Temperature Range	
Hermetic DIP (μA757, μA757C)	−65°C to +150°C
Operating Temperature Range	
Military (μA757)	−55°C to +125°C
Commercial (μA757C)	0°C to +70°C
Pin Temperature	
Hermetic DIP (Soldering, 60 s) μA757	300°C

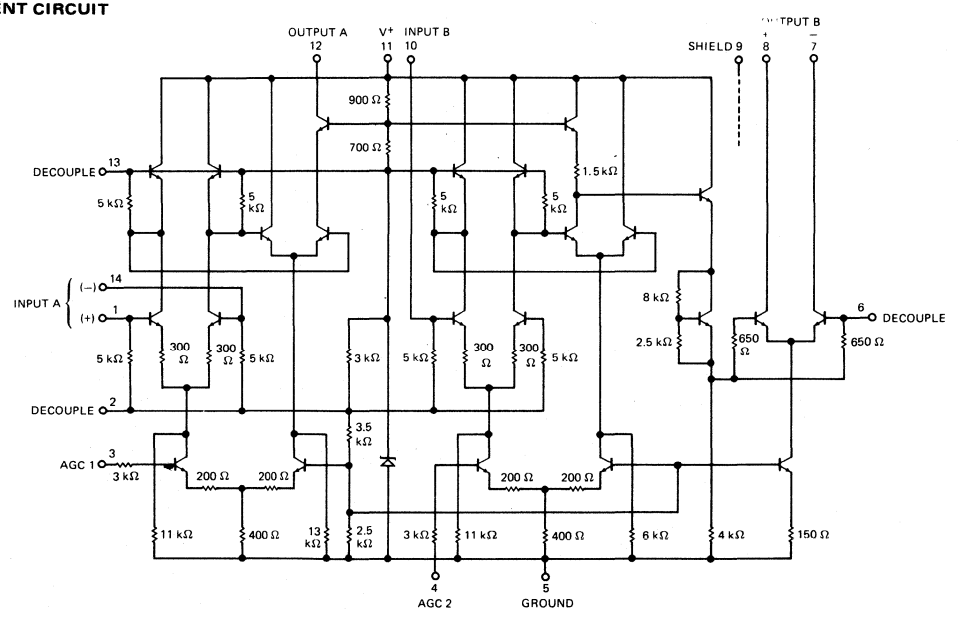
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA757	μA757DM
μA757C	μA757DC

EQUIVALENT CIRCUIT



Notes on following pages.

*Planar is a patented Fairchil process.

μA757

ELECTRICAL CHARACTERISTICS: $V_+ = +12$ V, $T_A = 25°C$, unless otherwise specified

CHARACTERISTICS	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
Supply Current	$V_{AGC\ 1,2} = +0.8$ V	1		13	17	mA
	$V_{AGC\ 1,2} = +3.0$ V			17	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2} = +0.8$ V	1		170	210	mW
	$V_{AGC\ 1,2} = +3.0$ V			200	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2} = +0.8$ V, f = 500 kHz	2	65	74		dB
	$V_{AGC\ 1,2} = +0.8$ V, f = 10.7 MHz	2	60	70		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2} = +1.7$ V, f = 500 kHz	2	20	39	46	dB
	$V_{AGC\ 1,2} = +1.7$ V, f = 10.7 MHz	2		37		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2} = +3.0$ V, f = 500 kHz	2		2.0	10	dB
	$V_{AGC\ 1,2} = +3.0$ V, f = 10.7 MHz	2		1.0	8	dB
Current into either AGC Terminal	$V_{AGC\ 1,2} = +3.0$ V	1		15	50	μA
Gain Reduction Sensitivity	$V_{AGC\ 1,2} = +1.7$ V, f = 500 kHz	2		50		dB/V
Input Voltage for −3 dB Limiting at Output	$V_{AGC\ 1,2} = +0.8$ V, f = 500 kHz	2		0.5		mV
Intermodulation Products	Two-tone signal f_1 = 500 kHz, e_1 = 100 mV f_2 = 510 kHz, e_2 = 100 mV I_{OUT} = 1 mA p-p	2		−50		dB
SECTION 1						
Input Resistance at either Input Terminal	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			4.5		kΩ
Input Capacitance at either Input Terminal	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			2.2		pF
Output Resistance	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz			100		kΩ
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			100		kΩ
Output Capacitance	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz			2.6		pF
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			2.2		pF
Forward Transadmittance	$V_{AGC\ 1} = +0.8$ V, f = 500 kHz			14		mmho
	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz			13		mmho
Peak-to-Peak Output Current	$V_{AGC\ 1} = +3.0$ V, f = 500 kHz Output in full limiting		0.25	0.4		mA
Output Saturation Voltage.	I_{OUT} = 0.1 mA, $V_{AGC\ 1} = +3.0$ V			8.0	9.0	V
Noise Figure	R_S = 1.0 kΩ, f = 10.7 MHz			8.0		dB
	R_S = 1.0 kΩ, f = 500 kHz			8.0		dB
Interfering Signal Voltage at Input for 1.0% Cross Modulation	Carrier signal, f_c = 500 kHz Interfering signal, f_i = 510 kHz I_{OUT} = 0.5 mA p-p, $V_{AGC\ 1} = +0.8$ V			15		mV
SECTION 2						
Input Resistance	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			4.5		kΩ
Input Capacitance	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			2.2		pF
Output Resistance at either Output Terminal	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz			26		kΩ
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			20		kΩ
Output Capacitance at either Output Terminal	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz			2.2		pF
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			2.5		pF
Forward Transadmittance	$V_{AGC\ 2} = +0.8$ V, f = 500 kHz			440		mmho
	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz			280		mmho
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V		1.7	2.4	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V, f = 500 kHz Output in full limiting		3.8	4.8	7.0	mA
Output Saturation Voltage at either Output Terminal	I_{OUT} = 1.0 mA, $V_{AGC\ 2} = +3.0$ V			5.0	6.0	V
Power Supply Sensitivity	V_S = 12 V to 15 V					
	0 dB Gain Reduction			0.5		dB/V
	30 dB Gain Reduction			0.8		dB/V
	60 dB Gain Reduction			1.0		dB/V

4

μA757

ELECTRICAL CHARACTERISTICS: $V_+ = +12$ V, $T_A = +125°C$, unless otherwise specified

CHARACTERISTICS	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
Supply Current	$V_{AGC\ 1,2} = +0.8$ V	1		14	17	mA
	$V_{AGC\ 1,2} = +3.0$ V			17	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2} = +0.8$ V	1		170	210	mW
	$V_{AGC\ 1,2} = +3.0$ V			200	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2} = +0.8$ V, f = 500 kHz	2	55	71		dB
	$V_{AGC\ 1,2} = +0.8$ V, f = 10.7 MHz	2		62		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2} = +1.7$ V, f = 500 kHz	2		35		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2} = +3.0$ V, f = 500 kHz	2		2.0	15	dB
	$V_{AGC\ 1,2} = +3.0$ V, f = 10.7 MHz	2		−1.0		dB
Current into either AGC Terminal	$V_{AGC\ 1,2} = +3.0$ V	1		15	50	μA
SECTION 1						
Peak-to-Peak Output Current	$V_{AGC\ 1} = +3.0$ V, f = 500 kHz Output in full limiting		0.2	0.4		mA
Output Saturation Voltage	$I_{OUT} = 0.1$ mA, $V_{AGC\ 1} = +3.0$ V			8.0	9.4	V
SECTION 2						
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V		1.7	2.8	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V, f = 500 kHz Output in full limiting		3.8	5.6	7.0	mA
Output Saturation Voltage at either Output Terminal	$I_{OUT} = 1.0$ mA, $V_{AGC\ 2} = +3.0$ V			6.0	7.0	V

μA757

ELECTRICAL CHARACTERISTICS: $V_+ = +12$ V, $T_A = -55°C$, unless otherwise specified

CHARACTERISTICS	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
Supply Current	$V_{AGC\ 1,2} = +0.8$ V	1		10	17	mA
	$V_{AGC\ 1,2} = +3.0$ V			14	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2} = +0.8$ V	1		120	210	mW
	$V_{AGC\ 1,2} = +3.0$ V			170	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2} = +0.8$ V, f = 500 kHz	2	55	68		dB
	$V_{AGC\ 1,2} = +0.8$ V, f = 10.7 MHz	2		64		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2} = +1.7$ V, f = 500 kHz	2		28		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2} = +3.0$ V, f = 500 kHz	2		2.0	15	dB
	$V_{AGC\ 1,2} = +3.0$ V, f = 10.7 MHz	2		−3.0		dB
Current into either AGC Terminal	$V_{AGC\ 1,2} = +3.0$ V	1		30	70	μA
SECTION 1						
Peak-to-Peak Output Current	$V_{AGC\ 1} = +3.0$ V, f = 500 kHz Output in full limiting		0.2	0.4		mA
Output Saturation Voltage	$I_{OUT} = 0.1$ mA, $V_{AGC\ 1} = +3.0$ V			8.0	9.0	V
SECTION 2						
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V		1.0	1.7	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V, f = 500 kHz Output in full limiting		2.3	3.4	7.0	mA
Output Saturation Voltage at either Output Terminal	$I_{OUT} = 1.0$ mA, $V_{AGC\ 2} = +3.0$ V			4.0	6.0	V

μA757C

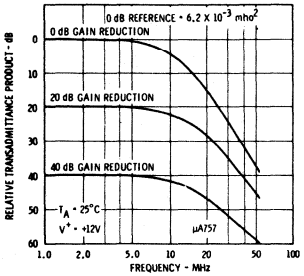
ELECTRICAL CHARACTERISTICS: $V_+ = +12V$, $T_A = +25°C$, unless otherwise specified

CHARACTERISTICS	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
Supply Current	$V_{AGC\ 1,2} = +0.8$ V	1		14	17	mA
	$V_{AGC\ 1,2} = +3.0$ V			18	22	mA
Internal Power Dissipation	$V_{AGC\ 1,2} = +0.8V$	1		170	210	mW
	$V_{AGC\ 1,2} = +3.0$ V			220	270	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2} = +0.8V$, f = 500 kHz	2	65	74		dB
	$V_{AGC\ 1,2} = +0.8$ V, f = 10.7 MHz	2	60	70		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2} = +1.7$ V, f = 500 kHz	2	20	39	46	dB
	$V_{AGC\ 1,2} = +1.7$ V, f = 10.7 MHz	2		37		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2} = +3.0$ V, f = 500 kHz	2		2.0	10	dB
	$V_{AGC\ 1,2} = +3.0$ V, f = 10.7 MHz	2		1.0	8	dB
Current into either AGC Terminal	$V_{AGC\ 1,2} = +3.0$ V	1		15	50	μA
Gain Reduction Sensitivity	$V_{AGC\ 1,2} = +1.7$ V, f = 500 kHz	2		50		dB/V
Input Voltage for −3 dB Limiting at Output	$V_{AGC\ 1,2} = +0.8$ V, f = 500 kHz	2		0.5		mV
Intermodulation Products	Two-tone signal f_1 = 500 kHz, e_1 = 100 mV f_2 = 510 kHz, e_2 = 100 mV I_{OUT} = 1 mA p-p	2		−50		dB
SECTION 1						
Input Resistance at either Input Terminal	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			4.5		kΩ
Input Capacitance at either Input Terminal	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			2.2		pF
Output Resistance	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz			100		kΩ
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			100		kΩ
Output Capacitance	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz			2.6		pF
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			2.2		pF
Forward Transadmittance	$V_{AGC\ 1} = +0.8$ V, f = 500 kHz			14		mmho
	$V_{AGC\ 1} = +0.8$ V, f = 10.7 MHz			13		mmho
Peak-to-Peak Output Current	$V_{AGC\ 1} = +3.0$ V, f = 500 kHz Output in full limiting		0.25	0.4		mA
Output Saturation Voltage	I_{OUT} = 0.1 mA, $V_{AGC\ 1} = +3.0$ V			8.0	9.0	V
Noise Figure	R_S = 1.0 kΩ, f = 10.7 MHz			8.0		dB
	R_S = 1.0 kΩ, f = 500 kHz			8.0		dB
Interfering Signal Voltage at Input for 1.0% Cross Modulation	Carrier signal, f_c = 500 kHz Interfering signal, f_i = 510 kHz I_{OUT} = 0.5 mA p-p, $V_{AGC\ 1} = +0.8$ V			15		mV
SECTION 2						
Input Resistance	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			4.5		kΩ
Input Capacitance	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			2.2		pF
Output Resistance at either Output Terminal	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz			26		kΩ
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			20		kΩ
Output Capacitance at either Output Terminal	$V_{AGC\ 2} = +0.8$ V f = 10.7 MHz			2.2		pF
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			2.5		pF
Forward Transadmittance	$V_{AGC\ 2} = +0.8$ V, f = 500 kHz			440		mmho
	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz			280		mmho
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V		1.7	2.4	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V, f = 500 kHz Output in full limiting		3.8	4.8	7.0	mA
Output Saturation Voltage at either Output Terminal	I_{OUT} = 1.0 mA, $V_{AGC\ 2} = +3.0$ V			5.0	6.0	V
Power Supply Sensitivity	V_S = 12 V to 15 V					
	0 dB Gain Reduction			0.5		dB/V
	30 dB Gain Reduction			0.8		dB/V
	60 dB Gain Reduction			1.0		dB/V

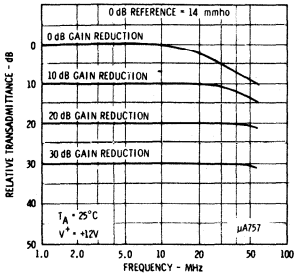
4

TYPICAL PERFORMANCE CURVES FOR μA757 AND μA757C

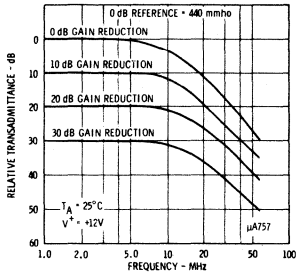
PRODUCT OF SECTIONS 1 AND 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



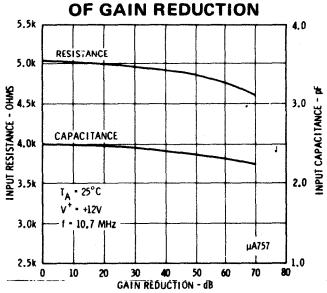
SECTION 1 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



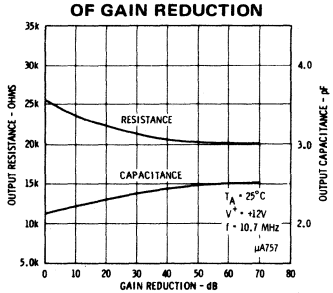
SECTION 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



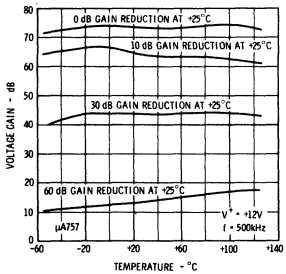
SECTION 1 AND 2 INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF GAIN REDUCTION



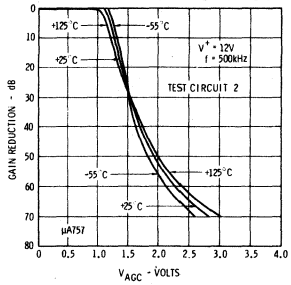
SECTION 2 OUTPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF GAIN REDUCTION



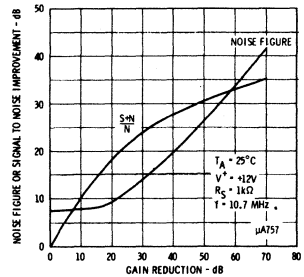
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



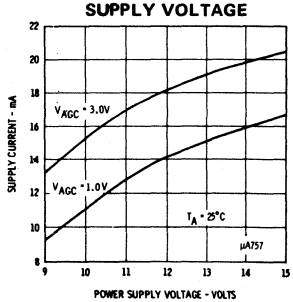
GAIN REDUCTION AS A FUNCTION OF GAIN CONTROL VOLTAGE



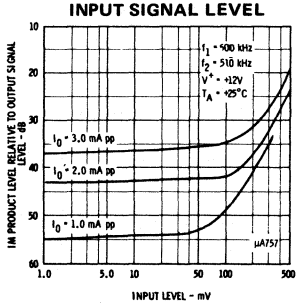
SIGNAL TO NOISE RATIO IMPROVEMENT AND NOISE FIGURE AS A FUNCTION OF GAIN REDUCTION



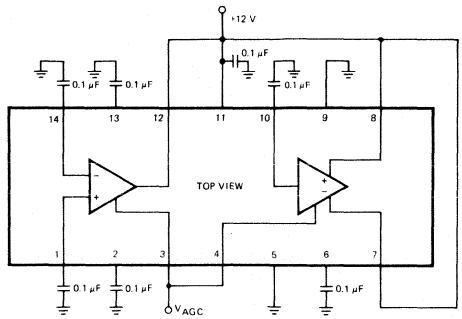
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



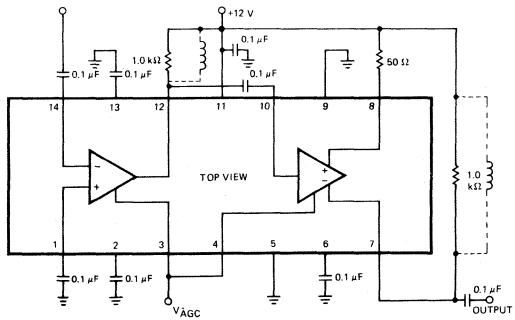
TWO TONE IM DISTORTION PRODUCTS AS A FUNCTION OF INPUT SIGNAL LEVEL



TEST CIRCUIT 1 (NOTE 3)



TEST CIRCUIT 2 (NOTE 2)



NOTES

1. For supply voltages less than +12 V, the absolute maximum voltage at either AGC terminal is equal to the supply voltage.
2. Rating applies to ambient temperatures up to 70° C. Above 70° C ambient derate linearly at 8.3 mW/° C.
3. For 10.7 MHz measurements, interstage capacitance and Section 2 output capacitance are tuned out. Pin 9 should be connected to GND.

μA758

PHASE LOCKED LOOP
FM STEREO MULTIPLEX DECODER

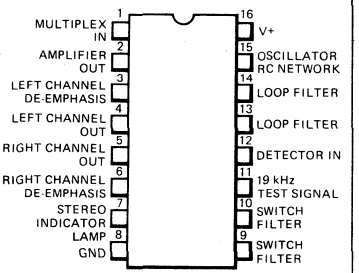
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA758 is a monolithic Phase Locked Loop FM Stereo Multiplex decoder using the Fairchild Planar* epitaxial process. This integrated circuit decodes an FM Stereo Multiplex Signal into Right and Left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. Internal functions include automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μA758 operates over a wide supply voltage range and uses a low number of external components. It has only one control to adjust: a potentiometer to set oscillator frequency. No external coils are required. The μA758 is suitable for all line-operated and automotive FM Stereo Receivers.

- **45 dB CHANNEL SEPARATION**
- **AUTOMATIC STEREO/MONO SWITCHING**
- **STEREO INDICATOR LAMP DRIVER WITH CURRENT LIMITING**
- **HIGH IMPEDANCE INPUT – LOW IMPEDANCE OUTPUTS**
- **70 dB SCA REJECTION**
- **ONE ADJUSTMENT FOR COMPLETE ALIGNMENT**
- **LOW NUMBER OF EXTERNAL PARTS – NO COILS**
- **10 V TO 16 V SUPPLY VOLTAGE RANGE**

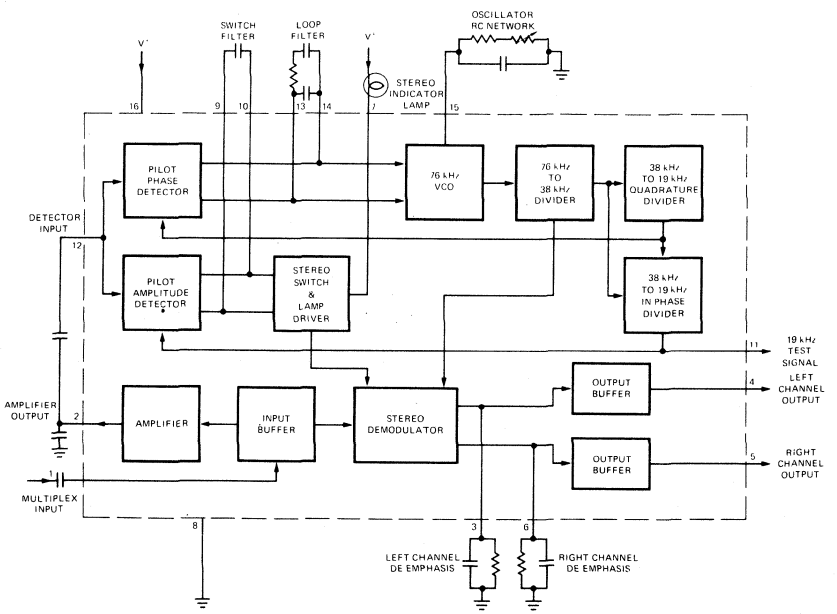
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9B
PACKAGE CODES P



ORDER INFORMATION

TYPE	PART NO.
μA758C	μA758PC

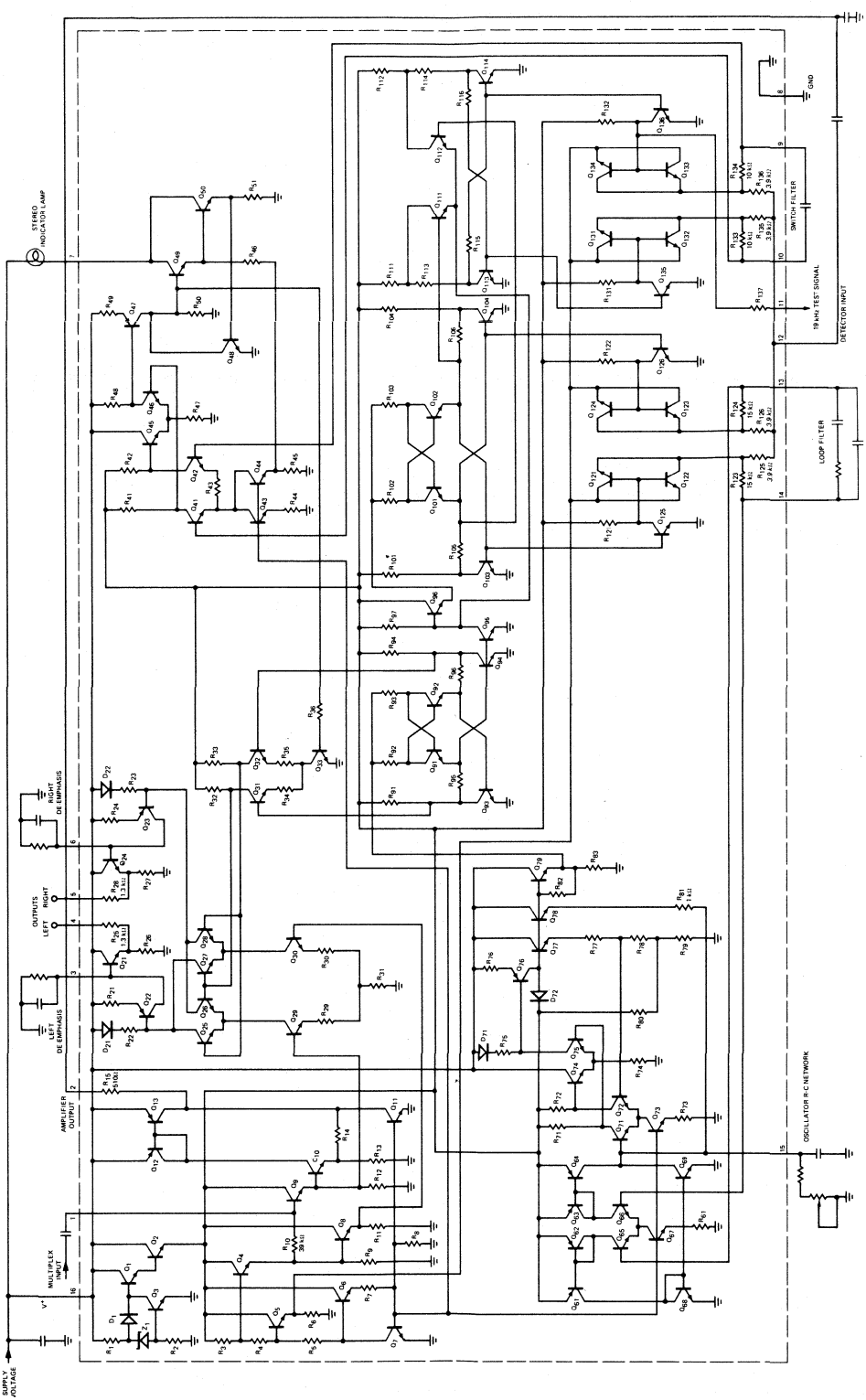
BLOCK DIAGRAM



Notes on following page.

*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



All resistance values are in ohms
All capacitance values are in picofarads

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18 V
Supply Voltage (≤ 15 Seconds)	+22 V
Voltage at Lamp Driver Terminal (Lamp OFF)	+22 V
Internal Power Dissipation (Note 1)	730 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature	
Molded DIP (Soldering, 10 seconds)	260°C

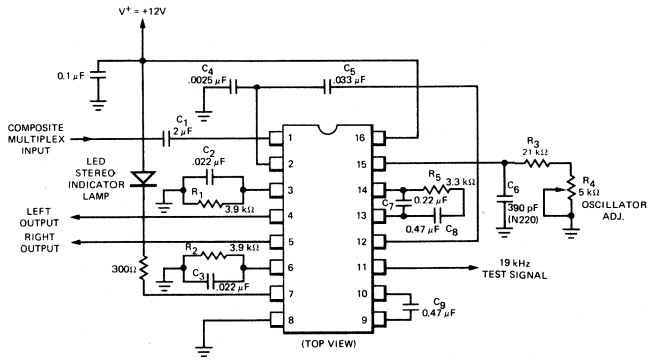
μA758C

ELECTRICAL CHARACTERISTICS: T_A = 25°C, V^+ = +12 V, 19 kHz pilot level = 30 mV_{RMS}, Multiplex Signal (L = R, pilot OFF) = 300 mV_{RMS}, Modulation Frequency = 400 Hz or 1 kHz, Test Circuit 1, unless otherwise specified

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Supply Current	Lamp OFF		26	35	mA
Maximum Available Lamp Current		75	150		mA
Voltage at Lamp Driver Terminal	I_{LAMP} = 50 mA		1.3	1.8	V
DC Voltage Shift at Either Output Terminal	Stereo to Mono Operation		30	150	mV
Power Supply Ripple Rejection	200 Hz, 200 mV_{RMS}	35	45		dB
Input Resistance		20	35		kΩ
Output Resistance		0.9	1.3	2.0	kΩ
Channel Separation	100 Hz		40		dB
	400 Hz	30	45		dB
	10 kHz		45		dB
Channel Balance			0.3	1.5	dB
Voltage Gain	1 KHz	0.5	0.9	1.4	V/V
Pilot Input Level	Lamp Turn-On		15	20	mV_{RMS}
	Lamp Turn-Off	2.0	7.0		mV_{RMS}
Pilot Input Level Hysteresis	Lamp Turn-Off to Turn-On	3.0	7.0		dB
Capture Range		2.0	4.0	6.0	%
Total Harmonic Distortion	Multiplex Level = 600 mV_{RMS} Pilot OFF		0.4	1.0	%
19 kHz Rejection		25	35		dB
38 kHz Rejection		25	45		dB
SCA Rejection (Note 2)			70		dB
VCO Tuning Resistance (Note 3)		21.0	23.3	25.5	kΩ
VCO Frequency Drift	0°C ≤ T_A ≤ 25°C		+0.1	±2	%
	25° ≤ T_A ≤ +70°C		−0.4	±2	%

NOTES:
(1) Rating applied for ambient temperatures to 70°C. Derate at 9.1 mW/°C from 70°C to 85°C.
(2) Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
(3) Total resistance from pin 15 to ground, in test circuit 1, required to set reference frequency at pin 11 to 19 kHz ±10 Hz.

TEST CIRCUIT 1 AND TYPICAL APPLICATION

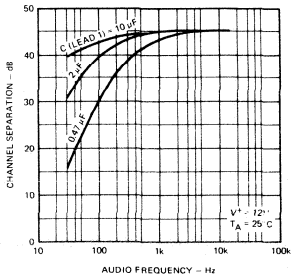


NOTE:
Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified.
C_1 Tolerance = +100%, −20%
C_6 Tolerance = ±1% in test circuit and ±5% in typical application
R_3 Tolerance = ±1%
R_4 Tolerance = ±10%
R_1 and R_2 Tolerances = ±1% in test circuit and ±5% in typical application.

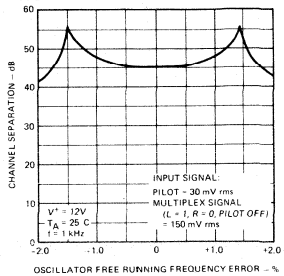
TYPICAL PERFORMANCE CURVES FOR μA758C

(Test Circuit 1 unless Otherwise Specified)

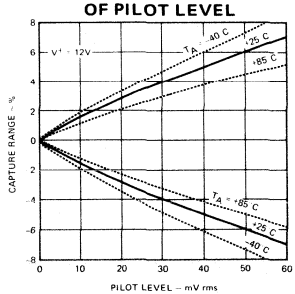
CHANNEL SEPARATION AS A FUNCTION OF AUDIO FREQUENCY



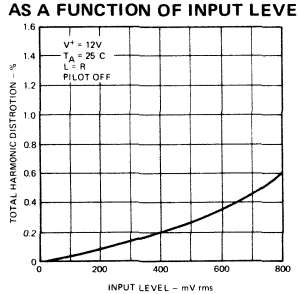
CHANNEL SEPARATION AS A FUNCTION OF OSCILLATOR FREE RUNNING FREQUENCY ERROR



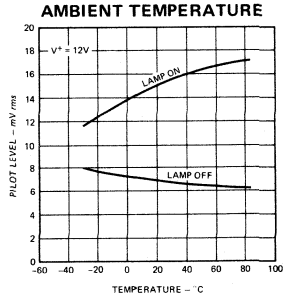
CAPTURE RANGE AS A FUNCTION OF PILOT LEVEL



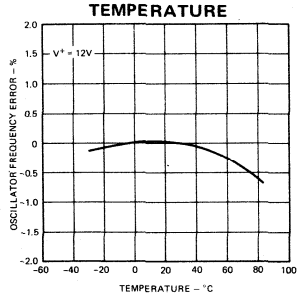
TOTAL HARMONIC DISTORTION AS A FUNCTION OF INPUT LEVEL



LAMP TURN ON AND TURN OFF SENSITIVITY AS A FUNCTION OF AMBIENT TEMPERATURE



OSCILLATOR FREE RUNNING FREQUENCY ERROR AS A FUNCTION OF AMBIENT TEMPERATURE



4

μA759

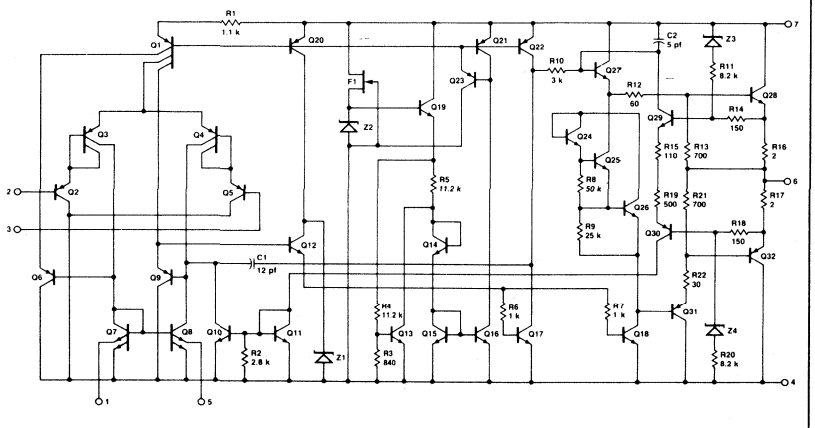
POWER OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA759 is a high performance monolithic operational amplifier constructed using the Fairchild Planar* Epitaxial process. The amplifier provides 325 mA output current and features small signal characteristics better than the μA741. The amplifier is designed to operate from a single or dual power supply and the input common mode range includes the negative supply. The high gain and high output power provide superior performance whenever an operational amplifier is needed. The μA759 employs internal current limiting, thermal shutdown and safe area compensation making it essentially indestructable. It is intended for a wide range of applications including voltage regulators, audio amplifiers, servo amplifiers and power drivers.

- **OUTPUT CURRENT — 325 mA MINIMUM**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL OUTPUT TRANSISTORS SAFE AREA PROTECTION**
- **INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND OR NEGATIVE SUPPLY**
- **AVAILABLE IN THREE PACKAGE STYLES**

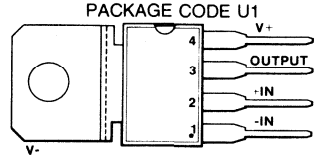
EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS

POWER WATT PACKAGE

(TOP VIEW)
PACKAGE OUTLINE 8Z
PACKAGE CODE U1

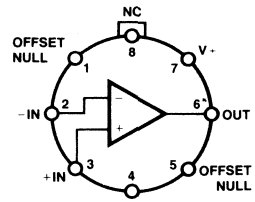


ORDER INFORMATION

TYPE	PART NO.
μA759C	μA759U1C

8-PIN METAL CAN

(TOP VIEW)
PACKAGE OUTLINE 5B
PACKAGE CODE H



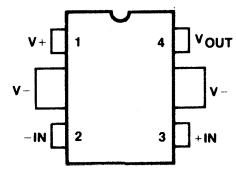
Note: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
μA759	μA759HM
μA759C	μA759HC

MINI BATWING

(TOP VIEW)
PACKAGE OUTLINE 9V
PACKAGE CODE T2



ORDER INFORMATION

TYPE	PART NO.
μA759C	μA759T2C

*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between V+ and V−	36 V
Differential Input Voltage (Note 1)	30 V
Input Voltage (Note 1)	(V− −0.3 V) to V+
Internal Power Dissipation (Note 2)	Internally Limited
Operating Junction Temperature Range	
Military (μA759)	−55°C to +150°C
Commercial (μA759C)	0°C to +125°C
Storage Temperature Range	
4-Pin Power Watt (U1)	−55°C to +150°C
4-Pin Mini Batwing (T2)	−55°C to +150°C
8-Pin TO-99 (H)	−65°C to +150°C
Pin Temperature	
4-Pin Power Watt (U1) (Soldering, 10 s)	260°C
4-Pin Mini Batwing (T2) (Soldering, 10 s)	260°C
8-Pin TO-99 (H) (Soldering, 60 s)	300°C

NOTES:
1. For a supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.

2. Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the thermal resistance values on page 3 should be used.:

4

μA759

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_J = 25°C$ unless otherwise specified

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10\ k\Omega$		1.0	3.0	mV
Input Offset Current				5.0	30	nA
Input Bias Current				50	150	nA
Input Resistance			0.25	1.5		MΩ
Input Voltage Range			+13 to $-V_S$	+13.5 to $-V_S$		V
Large Signal Voltage Gain		$R_L \geq 50\ \Omega$, $V_{OUT} = \pm 10$ V	50 k	200 k		V/V
Supply Current				12	18	mA
Peak Output Current		$3\ V \leq \lvert V_S - V_{OUT} \rvert < 10$ V	±325	±500		mA
Short Circuit Current		$\lvert V_S - V_{OUT} \rvert = 30$ V		±200		mA
Transient Response	Risetime	$R_L \geq 50\ \Omega$		300		ns
(Unity Gain)	Overshoot	$R_L \geq 50\ \Omega$		5.0		%
Slew Rate		$R_L \geq 50\ \Omega$		0.6		V/μs
Unity Gain Bandwidth				1.0		MHz
The following specifications apply for $-55°C \leq T_J \leq 150°C$						
Input Offset Voltage		$R_S \leq 10\ k\Omega$			4.5	mV
Input Offset Current					60	nA
Input Bias Current					300	nA
Common Mode Rejection Ratio		$R_S \leq 10\ k\Omega$	80	100		dB
Power Supply Rejection Ratio		$R_S \leq 10\ k\Omega$	80	100		dB
Large Signal Voltage Gain		$R_L \geq 50\ \Omega$, $V_{OUT} = \pm 10$ V	25 k	200 k		V/V
Output Voltage Swing		$R_L \geq 50\ \Omega$	±10	±12.5		V

μA759C

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_J = 25°C$ unless otherwise specified

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current				5.0	50	nA
Input Bias Current				50	250	nA
Input Resistance			0.25	1.5		MΩ
Input Voltage Range			+13 to $-V_S$	+13.5 to $-V_S$		V
Large Signal Voltage Gain		$R_L \geq 50$ Ω, $V_{OUT} = \pm 10$ V	25 k	200 k		V/V
Supply Current				12	18	mA
Peak Output Current		$3 \text{ V} \leq \lvert V_S - V_{OUT} \rvert \leq 10$ V	±325	±500		mA
Short Circuit Current		$\lvert V_S - V_{OUT} \rvert = 30$ V		±200		mA
Transient Response (Unity Gain)	Risetime	$R_L \geq 50$ Ω		300		ns
	Overshoot	$R_L \geq 50$ Ω		10		%
Slew Rate				0.5		V/μs
Unity Gain Bandwidth				1.0		MHz
The following specifications apply for $0°C \leq T_J \leq 125°C$						
Input Offset Voltage		$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current					100	nA
Input Bias Current					400	nA
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	70	100		dB
Power Supply Rejection Ratio		$R_S \leq 10$ kΩ	80	100		dB
Large Signal Voltage Gain		$R_L \geq 50$ Ω, $V_{OUT} = \pm 10$ V	25 k	200 k		V/V
Output Voltage Swing		$R_L \geq 50$ Ω	±10	±12.5		V

PACKAGE	TYP	MAX	TYP	MAX
	θ_{JC}	θ_{JC}	θ_{JA}	θ_{JA}
Power Watt (U1)	8.0°C/W	12°C/W	75°C/W	80°C/W
Mini Batwing (T2)	8.0°C/W	12°C/W	75°C/W	80°C/W
Metal Can (H)	30°C/W	40°C/W	120°C/W	185°C/W

$$P_{D\,(MAX)} = \frac{T_J\,(MAX) - T_A}{\theta_{JC} + \theta_{CA}} \quad \text{or} \quad \frac{T_J\,(MAX) - T_A}{\theta_{JA}} \quad \text{(Without a heat sink)}$$

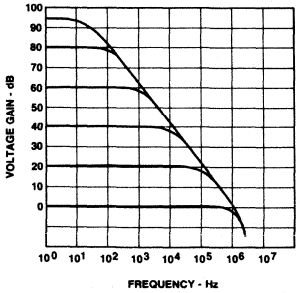
$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J: $T_J = T_A + P_D\,(\theta_{JC} + \theta_{CA})$ or $T_A + P_D\theta_{JA}$ (Without heat sink)

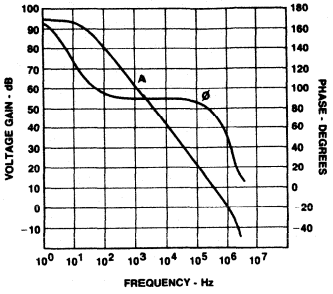
Where: T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JA} = Junction to ambient thermal resistance
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to ambient thermal resistance
θ_{CS} = Case to heat sink thermal resistance
θ_{SA} = Heat sink to ambient thermal resistance

TYPICAL PERFORMANCE CURVES

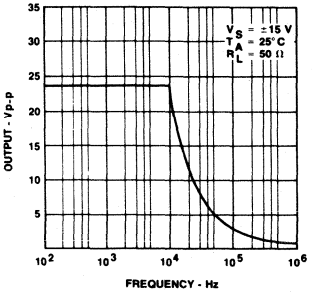
FREQUENCY RESPONSE AT VARIOUS CLOSED LOOP GAIN SETTINGS



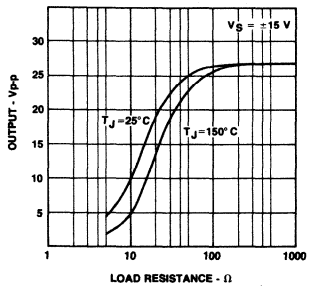
OPEN LOOP GAIN AND PHASE RESPONSE AS A FUNCTION OF FREQUENCY



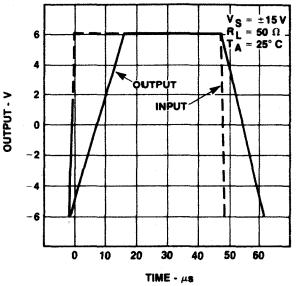
OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



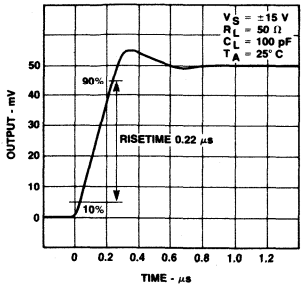
P-P OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE



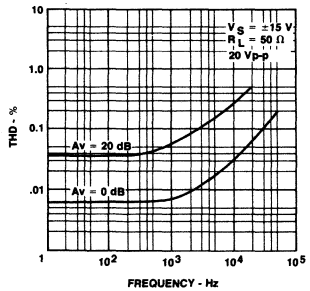
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



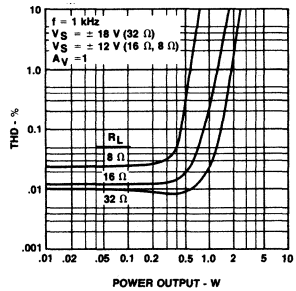
VOLTAGE FOLLOWER TRANSIENT RESPONSE



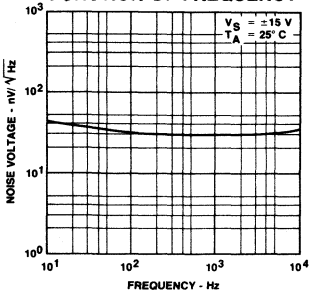
TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY



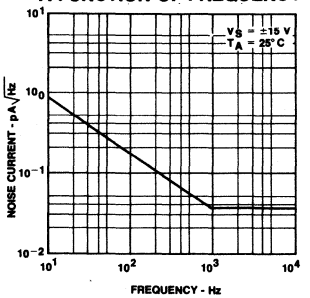
TOTAL HARMONIC DISTORTION AS A FUNCTION OF POWER OUTPUT



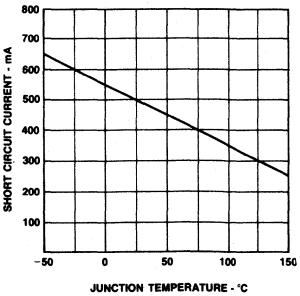
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



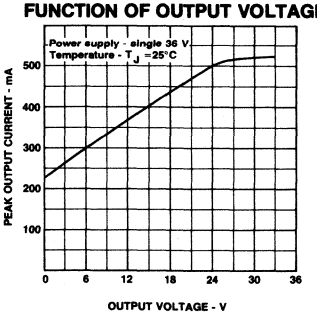
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



OUTPUT SHORT CIRCUIT CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE



PEAK OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



MOUNTING HINTS

Metal Can Package (μA759HC/μA759HM)

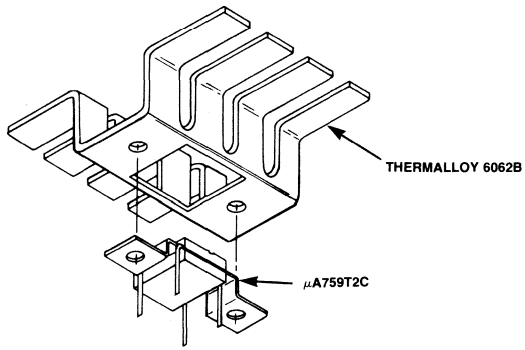
The μA759 in the 8-Pin TO-99 metal can package must be used with a heat sink. With ±15 V power supplies, the μA759 can dissipate up to 540 mW in its quiescent (no load) state. This would result in a 100°C rise in chip temperature to 125°C (assuming a 25°C ambient temperature). In order to avoid this problem, it is advisable to use either a slip on or stud mount heat sink with this package. If a stud mount heat sink is used, it may be necessary to use insulating washers between the stud and the chassis because the case of the μA759 is internally connected to the negative power supply terminal.

Power Watt Package (μA759U1C)

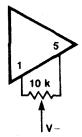
The μA759U1C is designed to be attached by the tab to a heat sink. This heat sink can be either one of the many heat sinks which are commercially available, a piece of metal such as the equipment chassis, or a suitable amount of copper foil as on a double sided PC board. The important thing to remember is that the negative power supply connection to the op amp must be made through the tab. Furthermore, adequate heat sinking must be provided to keep the chip temperature below 125°C under worst case load and ambient temperature conditions.

Power Mini Dip Package (μA759T2C)

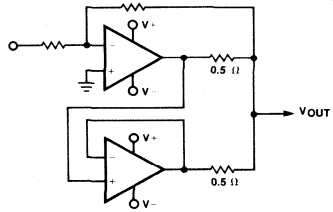
The μA759T2C is designed to conduct heat away from the chip by way of the two tabs or "batwings" on the sides of the package. These tabs can be bolted or soldered to copper foil on the top side of a double sided PC board. Alternatively, the tabs can be bolted to a commercially available heat sink such as the Thermalloy 6062B. As with the Power Watt package, the tabs on the T2C package are the terminals for the negative power supply.



OFFSET NULL CIRCUIT

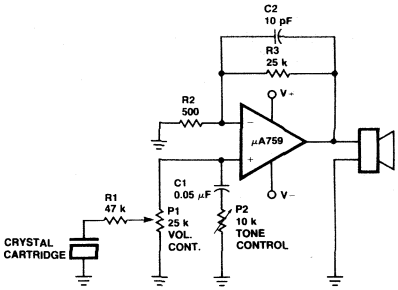


PARALLELING μA759 POWER OP AMPS

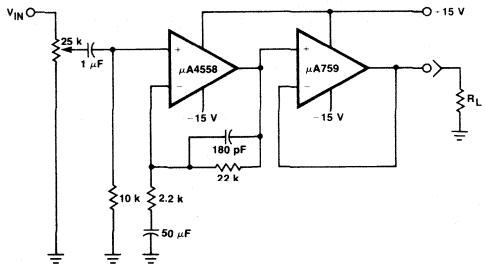


AUDIO APPLICATIONS

LOW COST PHONO AMPLIFIER

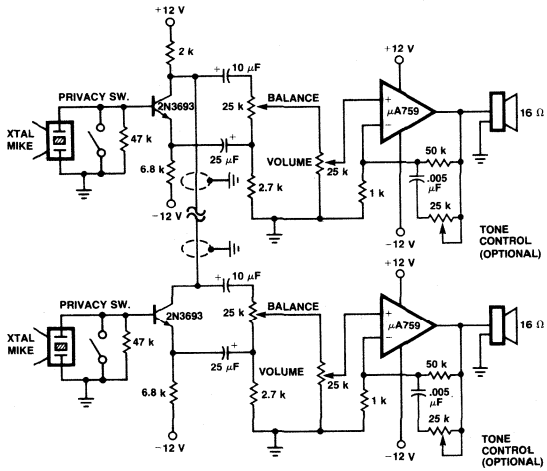


HEADPHONE AMPLIFIER



Speaker Impedance (ohms)	Output Power (watts)	Min Supply (volts)	V_{out} p-p (volts)
4	.18	9	2.4
8	.36	12	4.8
16	.72	15	9.6
32	1.44	25	19.2

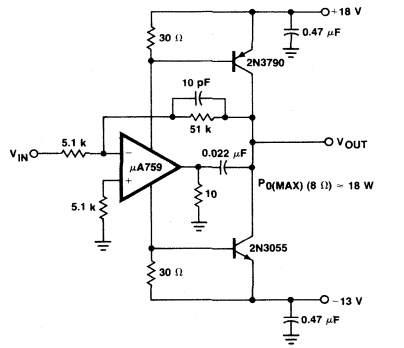
BIDIRECTIONAL INTERCOM SYSTEM USING THE μA759 POWER OP AMP



FEATURES

- Circuit Simplicity
- 1 Watt of Audio Output
- Duplex operation with only one two-wire cable as interconnect

HIGH SLEW RATE POWER OP AMP/AUDIO AMP



FEATURES

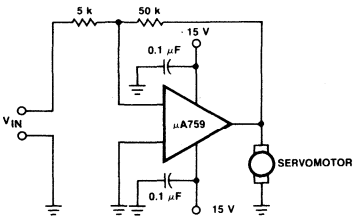
- High Slew Rate 9 V/μs
- High 3 dB Power Bandwidth 85 kHz
- 18 Watts Output Power Into An 8 Ω Load
- Low Distortion — .2%, 10 VRMS, 1 kHz Into 8 Ω

DESIGN CONSIDERATION

- $A_V \geq 10$

SERVO APPLICATIONS

DC SERVO AMPLIFIERS



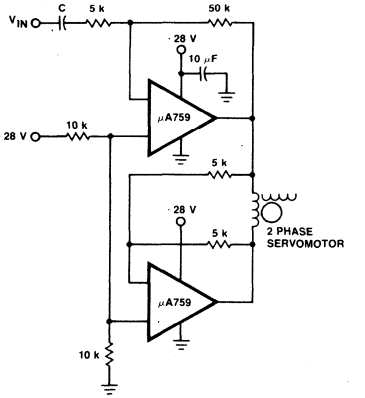
FEATURES

- Circuit Simplicity
- One Chip Means Excellent Reliability

DESIGN CONSIDERATIONS

- $I_{OUT} \leq 325$ mA

AC SERVO AMPLIFIER - BRIDGE TYPE



FEATURES

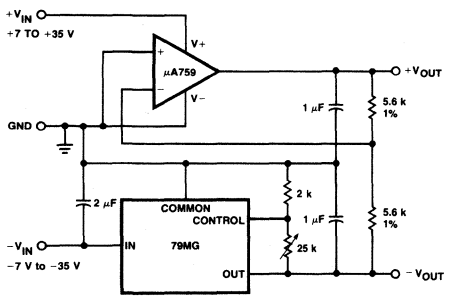
- Gain of 10
- Use of μA759 Means Simple Inexpensive Circuit

DESIGN CONSIDERATIONS

- 325 mA Max Output Current

REGULATOR APPLICATIONS

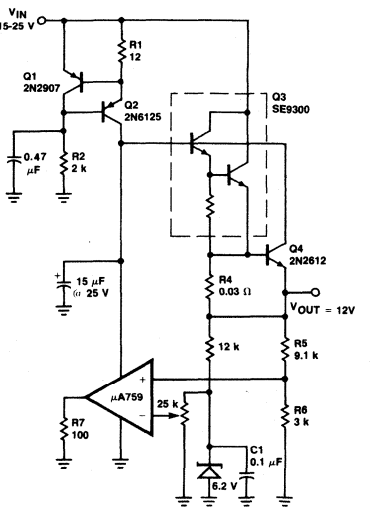
ADJUSTABLE DUAL TRACKING REGULATOR



FEATURES

- Wide Output Voltage Range (± 2.2 to ± 30 V)
- Excellent Load Regulation $\Delta V_{OUT} < \pm 5$ mV for $\Delta I_{OUT} = \pm 0.2$ A
- Excellent Line Regulation $\Delta_{OUT} < \pm 2$ mV for $\Delta V_{IN} = 10$ V

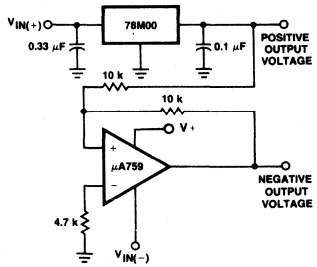
10 AMP - 12 VOLT REGULATOR



FEATURES

- Excellent Load and Line Regulation
- Excellent Temperature Coefficient-Depends Largely on Tempco of the Reference Zener

DUAL TRACKING REGULATOR



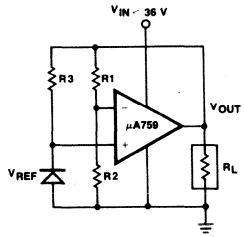
FEATURES

- Positive & Negative Outputs "Track"
- Inexpensive
- 500 mA Positive Output
- 325 mA Negative Output
- Any 78M Voltage Can be Used +5, +6, +8, +12, +15, +20, +24

DESIGN CONSIDERATIONS

- $V_{IN}(-)$ must not exceed −36 V
- $V_{IN}(-)$ must be at least 3 V more negative than $V_{OUT}(-)$

PRECISION ADJUSTABLE VOLTAGE REGULATOR



FEATURES

- Low Temperature Coefficient
  —Depends primarily on tempco of reference zener
- Excellent Load and Line Regulation
  —current through reference zener is independent of load and line
- Up to 325 mA Output Current

DESIGN CONSIDERATIONS

- $V_{IN} \leq 36$ V $\quad I_{REF} = \frac{V_{OUT} - V_{REF}}{R3}$
- $V_{IN} \geq V_{OUT} + 3$ V $\quad V_{OUT} = V_{REF} \frac{(R1 + R2)}{R2}$

μA767

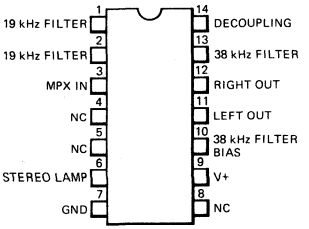
FM STEREO MULTIPLEX DECODER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA767 is a monolithic FM Stereo Multiplex Decoder System constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This integrated circuit demodulates a stereo multiplex signal into the right and left audio channels while inherently suppressing SCA frequency components. Internal provision is made for driving an external stereo mode indicator lamp. The excellent performance, wide supply range and low external parts requirement make the μA767 suitable for all line-operated and automotive FM stereo multiplex applications. For stereo decoding including interstation audio muting and stereo/mode switching, see the μA732 data sheet.

- **45 dB CHANNEL SEPARATION**
- **55 dB STORECAST REJECTION WITHOUT SCA FILTERS**
- **HIGH CURRENT STEREO INDICATOR LAMP DRIVER**
- **OPERATION WITH 8 V TO 14 V SUPPLIES**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9A
PACKAGE CODE P



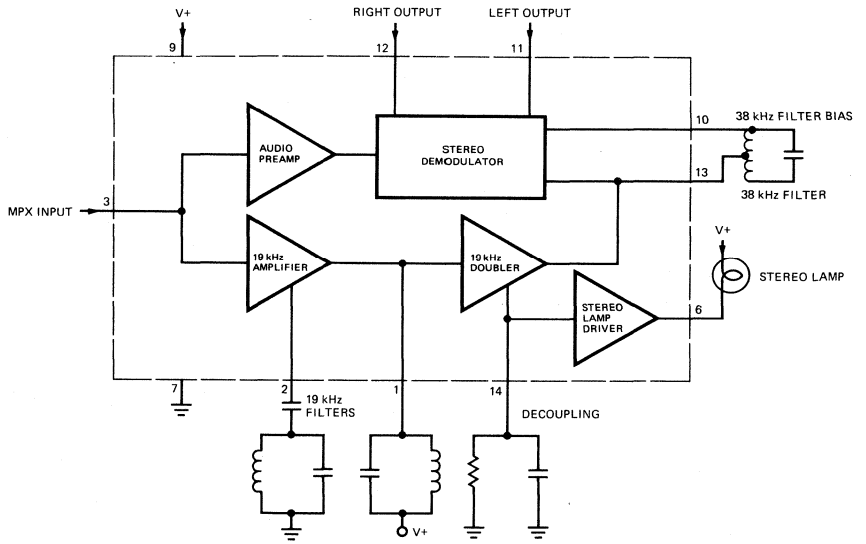
ORDER INFORMATION

TYPE	PART NO.
μA767C	μA767PC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	+15 V
Voltage at Stereo Lamp Driver Terminal	+22 V
Current into Stereo Lamp Driver Terminal (Note 2)	100 mA
Internal Power Dissipation	670 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature	
Hermetic DIP (Soldering, 60 s)	+300°C
Molded DIP (Soldering, 10 s)	+260°C

BLOCK DIAGRAM



Notes on following page.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, V+ = +12 V, 200 mV_{RMS} standard stereo multiplex signal applied to input, unless otherwise specified (Note 3). Refer to Test Circuit of Figure 1.

CHARACTERISTICS	MIN	TYP	MAX	UNITS
Supply Current		12	18	mA
Input Resistance	12	20		kΩ
Stereo Separation				
f = 100 Hz		40		dB
f = 1 kHz	30	45		dB
f = 10 kHz	20	40		dB
Channel Balance (Monaural Input)		0.2		dB
Total Harmonic Distortion		0.5	1.0	%
Voltage Gain		1.0		V/V
67 kHz Storecast Rejection (Note 4)		55		dB
19 kHz Pilot Level Required at Input for:				
Stereo Indicator Lamp on		12	22	mV RMS
Stereo Indicator Lamp off	4.0	8.0		mV RMS
High Frequency Audio Components in Left and Right Outputs (dB below 1 kHz output)				
19 kHz		30		dB
38 kHz		25		dB

NOTES:

(1) Power supply transients up to 22V are permissible for periods of 15 seconds. However, extended operation at voltages greater than 15V should be avoided as the maximum allowable internal power dissipation for this device may be exceeded.

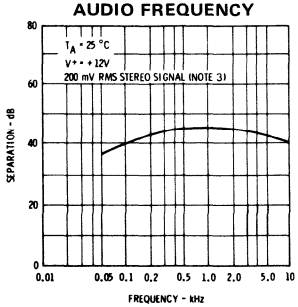
(2) Rating applies to steady state current. Maximum permissible surge current during turn-on of the Stereo Indicator Lamp is 500 mA.

(3) "Standard Stereo Multiplex Signal" here refers to a 200mV RMS (0.56V p-p) composite stereo signal including 10% pilot with L=1 and R = 1 as described in the FCC Rules on FM Broadcasting.

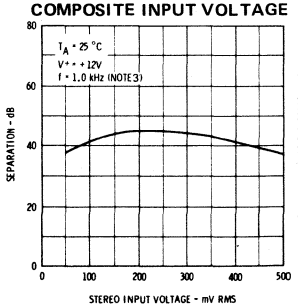
(4) Measured with a stereo composite signal consisting of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on FM Broadcasting.

TYPICAL PERFORMANCE CURVES

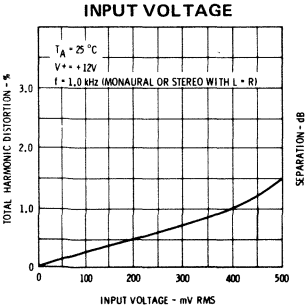
SEPARATION AS A FUNCTION OF AUDIO FREQUENCY



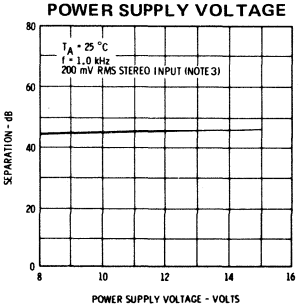
1 kHz SEPARATION AS A FUNCTION OF COMPOSITE INPUT VOLTAGE



1 kHz DISTORTION AS A FUNCTION OF INPUT VOLTAGE



1 kHz SEPARATION AS A FUNCTION OF POWER SUPPLY VOLTAGE



μA767 FM STEREO MULTIPLEX DECODER TEST CIRCUIT AND TYPICAL APPLICATION

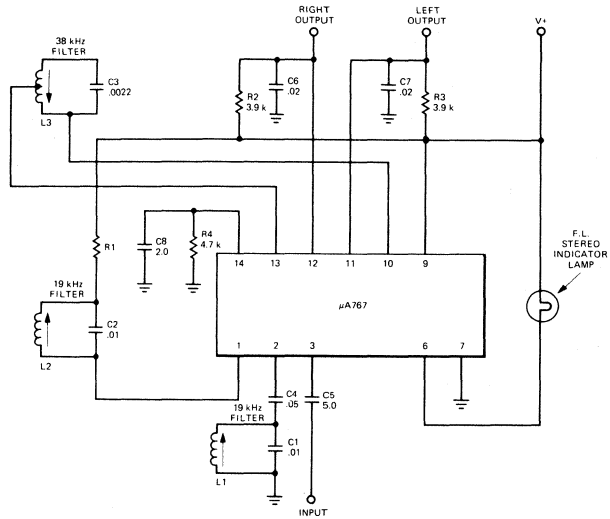
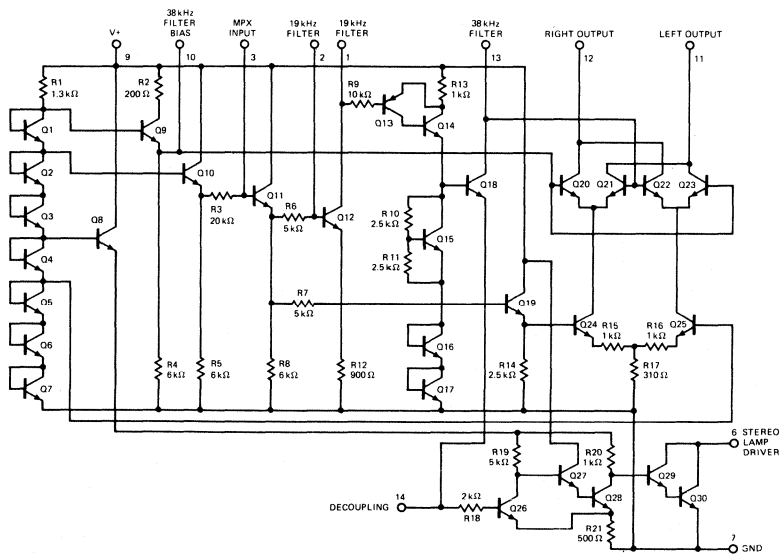


Fig. 1

NOTES:
(1) Capacitors C_1, C_2, and C_3 should be polystyrene or mylar.
(2) Coils L_1 and L_2 are 7.0 mH nominal with Q_{UL} = 60 (Miller #1361 or equivalent).
(3) Coil L_3 is 8.0 mH nominal with Q_{UL} = 80, tapped at 10:1 turns ratio. (Miller #1362 or equivalent).
(4) Resistor R_1 can be increased (or decreased) in value to increase (or decrease) the 19kHz sensitivity.

μA767 FM STEREO MULTIPLEX DECODER EQUIVALENT CIRCUIT



μA780

CHROMA SUBCARRIER REGENERATOR (PHASE LOCKED LOOP)

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA780 is a monolithic Phase Locked Loop designed for use as a color TV subcarrier regenerator and is constructed using the Fairchild Planar* epitaxial process. This integrated circuit, which uses an automatic phase control (APC) loop, accepts the composite NTSC color video signal, extracts the color subcarrier reference and generates a CW signal suitable for use as a chroma demodulation reference. Other features include control of the CW phase (tint) by a dc voltage, blanking of the CW output during burst time and synchronous generation of an automatic color control (ACC) voltage.

The μA780 in combination with the μA781 Chroma IF Amplifier and the μA746 Chroma Demodulator forms a complete low cost, high quality chroma processing system for color TV receivers.

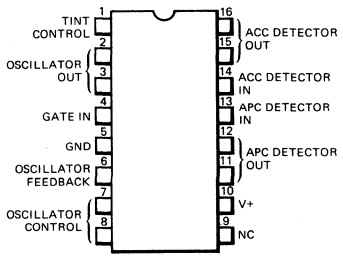
The μA780 is also useful as a communications phase locked loop system to select, amplify and demodulate AM, FM, FSK and SSB signals.

- **COMPLETE COLOR TV SUBCARRIER REGENERATOR**
- **AUTOMATIC PHASE CONTROL LOOP**
- **DC TINT CONTROL**
- **SYNCHRONOUS ACC/KILLER DETECTOR**
- **COLOR BURST GATING AND BLANKING**
- **INTERNALLY REGULATED SUPPLY**

ABSOLUTE MAXIMUM RATINGS

Supply Current	40 mA
Current into Gate Input Terminal	5 mA
Peak-to-Peak Voltage at either APC or ACC Detector Input Terminals	5 V
Internal Power Dissipation	730 mW
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Pin Temperature	
Molded DIP (Soldering, 10 seconds)	260°C

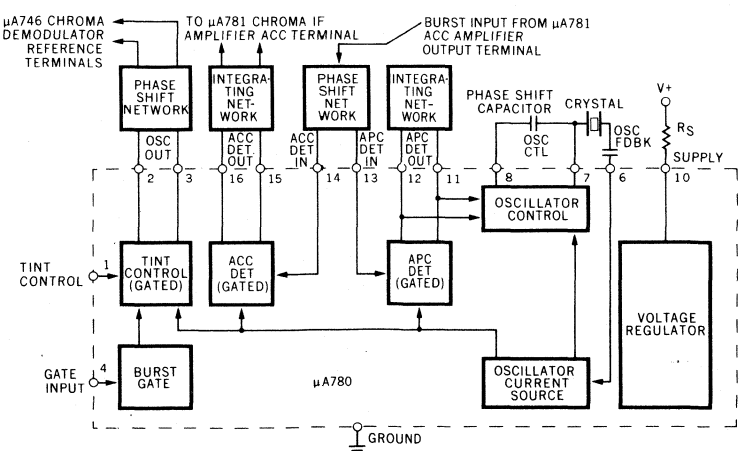
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B
PACKAGE CODE P



ORDER INFORMATION

TYPE	PART NO.
μA780C	μA780PC

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

μA780C

DC CHARACTERISTICS: $T_A = 25°C$, Gate "ON", Test Circuit 1 unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current			26		mA
Voltage at Supply Terminal		11.3	12.0	12.6	V
Supply Regulation (ΔV_{10})	$V_+ = 22$ V to $V_+ = 27$ V		40	200	mV
Total Current into Oscillator Output Terminals	Gate "OFF", 50 kΩ resistor connected between Pin 10 and Pin 6, Pin 2 shorted to Pin 3	4.2	5.8	7.6	mA
Current into Either APC Detector Output Terminal	12 kΩ resistor connected between Pin 6 and Ground		12	40	μA
Offset Voltage between ACC Detector Output Terminals ($V_{15} - V_{16}$)	50 kΩ resistor connected between Pin 10 and Pin 6	−330	−70	+330	mV
Offset Voltage between APC Detector Output Terminals ($V_{11} - V_{12}$)	50 kΩ resistor connected between Pin 10 and Pin 6	−375	−50	+375	mV
Offset Voltage between Oscillator Control Terminals ($V_7 - V_8$)	12 kΩ resistor connected between Pin 6 and Ground, $V_{11} = V_{12} = 9.5$ V	−330	−20	+330	mV
Offset Voltage between Oscillator Output Terminals ($V_2 - V_3$)	Gate "OFF"	−200	+300	+800	mV
Voltage at Oscillator Feedback Terminal			2.8		V
Voltage at ACC Detector Input Terminal		6.0	6.5	7.0	V
Voltage at APC Detector Input Terminal		6.0	6.5	7.0	V
Voltage at Tint Control Terminal			200	300	mV
Voltage at Tint Control Terminal	Gate "OFF"	7.3	7.6	8.2	V
Internal Power Dissipation			310	400	mW

μA780C

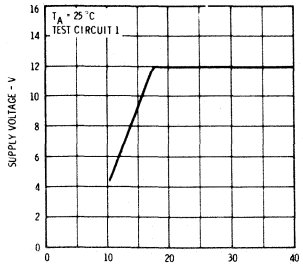
AC CHARACTERISTICS: $T_A = 25°C$, peak-to-peak burst level at APC Detector Input Terminal = 200 mV, Standard, NTSC Signal $f_o = 3.579545$ MHz, Test Circuit 2 unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Pull-in Range	$f_{\text{free run}} > f_o$		400		Hz
	$f_{\text{free run}} < f_o$		−400		Hz
Oscillator Static Phase Error	$f_{\text{free run}} = f_o + 120$ Hz		+2.2		Degree
	$f_{\text{free run}} = f_o - 120$ Hz		−2.2		Degree
Oscillator Control Sensitivity			12		Hz/mV
Input Resistance at Oscillator Feedback Terminal			2.2		kΩ
Input Capacitance at Oscillator Feedback Terminal			4.5		pF
Peak-to-Peak Current at Oscillator Output Terminal (Pin 3)	Tint Control Wiper at Ground		6.8		mA
ACC Detector Input Resistance			2.2		kΩ
ACC Detector Input Capacitance			4.5		pF
ACC Detector Sensitivity	100 mV_{p-p} burst level at ACC Detector Input Terminal, Oscillator Locked		+2.2		$mVdc/mV_{p-p}$
APC Detector Input Resistance			2.2		kΩ
APC Detector Input Capacitance			4.5		pF
APC Detector Sensitivity			5.0		mV/Degree

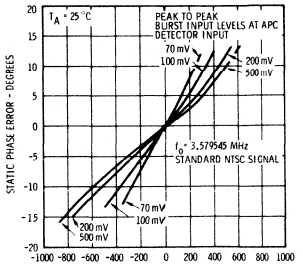
TYPICAL PERFORMANCE CURVES FOR μA780C

(Test Circuit 2 unless otherwise specified)

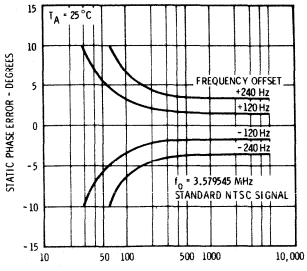
SUPPLY VOLTAGE AS A FUNCTION OF SUPPLY CURRENT



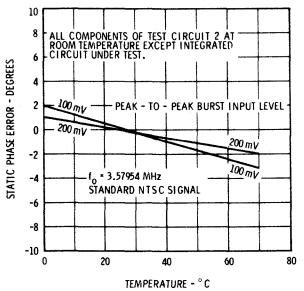
STATIC PHASE ERROR AS A FUNCTION OF FREQUENCY OFFSET



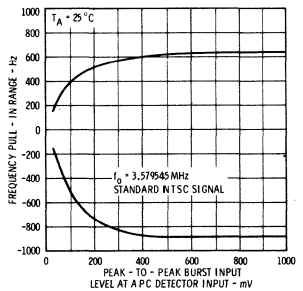
STATIC PHASE ERROR AS A FUNCTION OF BURST INPUT LEVEL



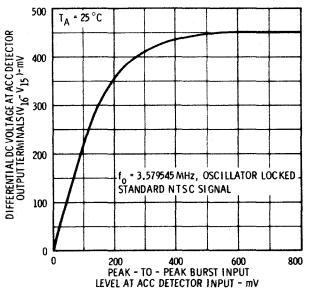
STATIC PHASE ERROR AS A FUNCTION OF TEMPERATURE



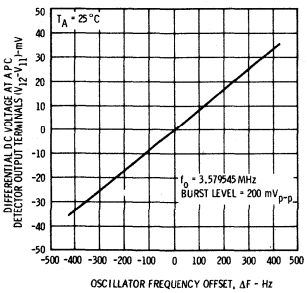
FREQUENCY PULL-IN RANGE AS A FUNCTION OF BURST INPUT LEVEL



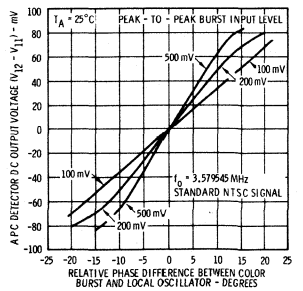
DIFFERENTIAL DC VOLTAGE AT ACC DETECTOR OUTPUT AS A FUNCTION OF BURST INPUT LEVEL



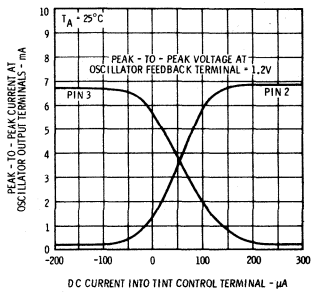
DIFFERENTIAL DC VOLTAGE AT APC DETECTOR OUTPUT TERMINALS AS A FUNCTION OF OSCILLATOR FREQUENCY OFFSET



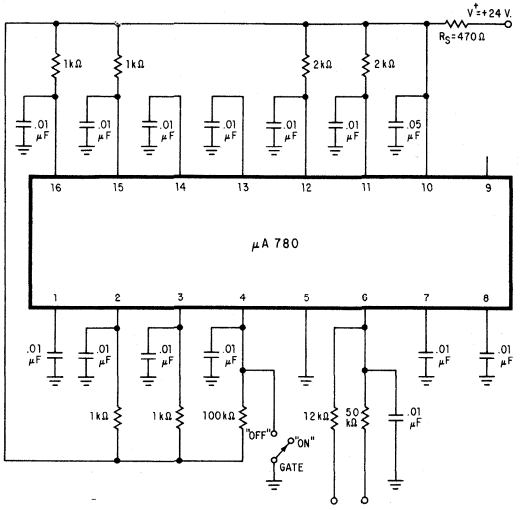
APC DETECTOR OUTPUT AS A FUNCTION OF RELATIVE PHASE DIFFERENCE



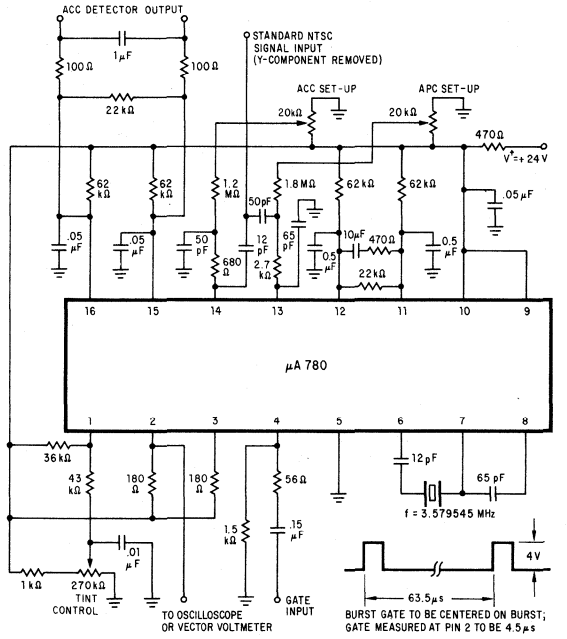
OSCILLATOR OUTPUT AS A FUNCTION OF TINT CONTROL CURRENT



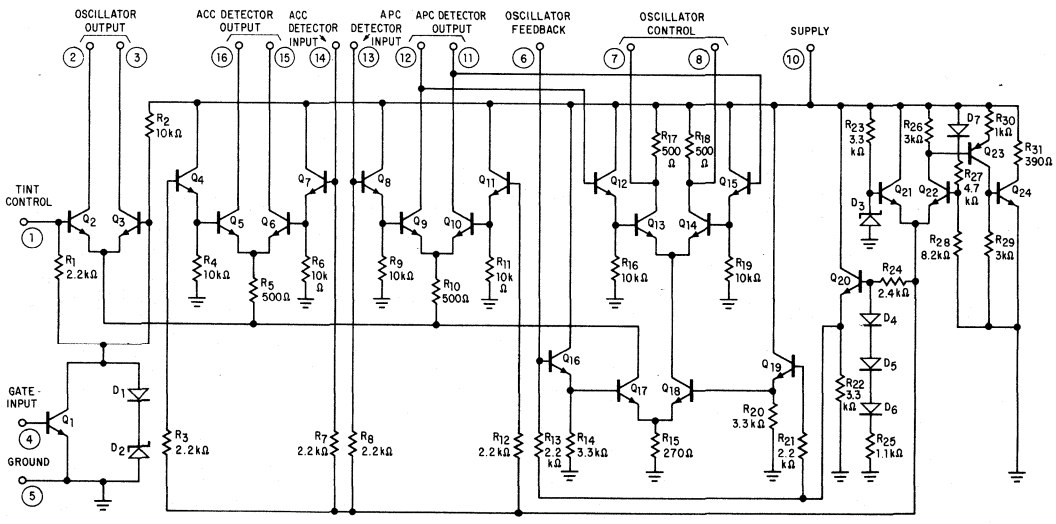
TEST CIRCUIT 1



TEST CIRCUIT 2

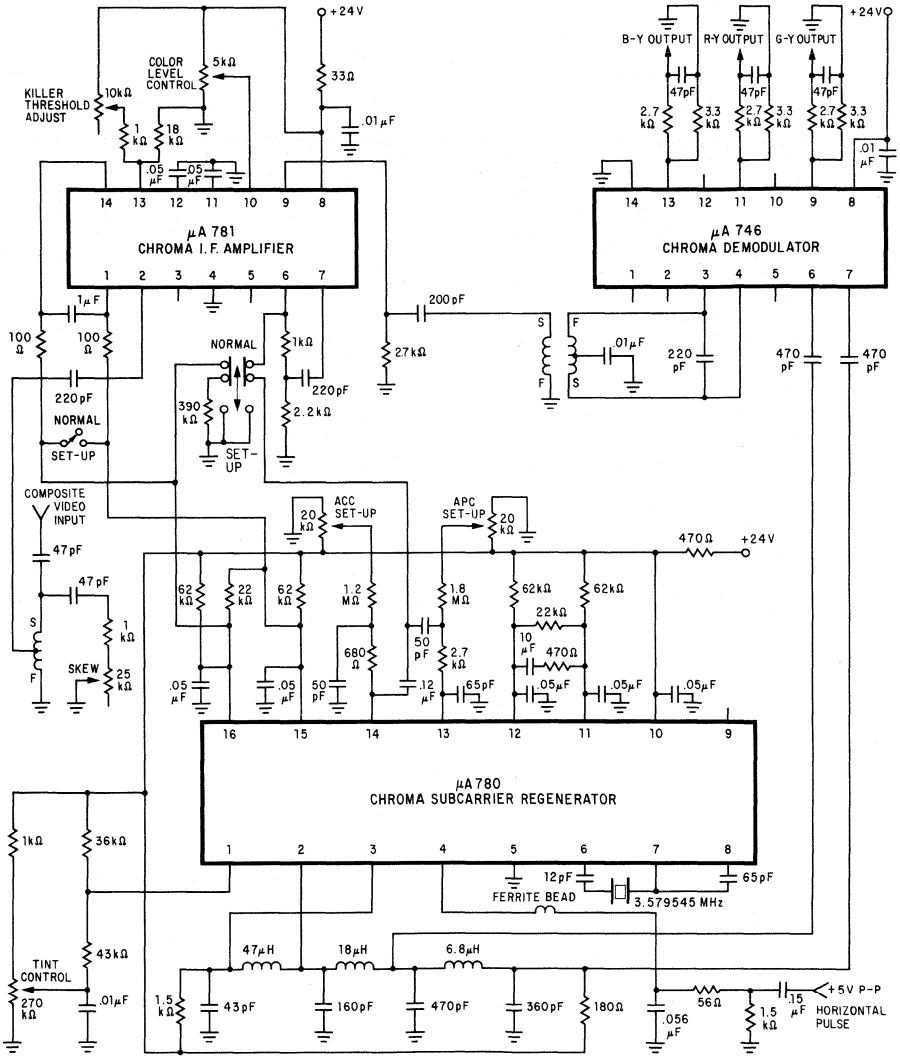


EQUIVALENT CIRCUIT

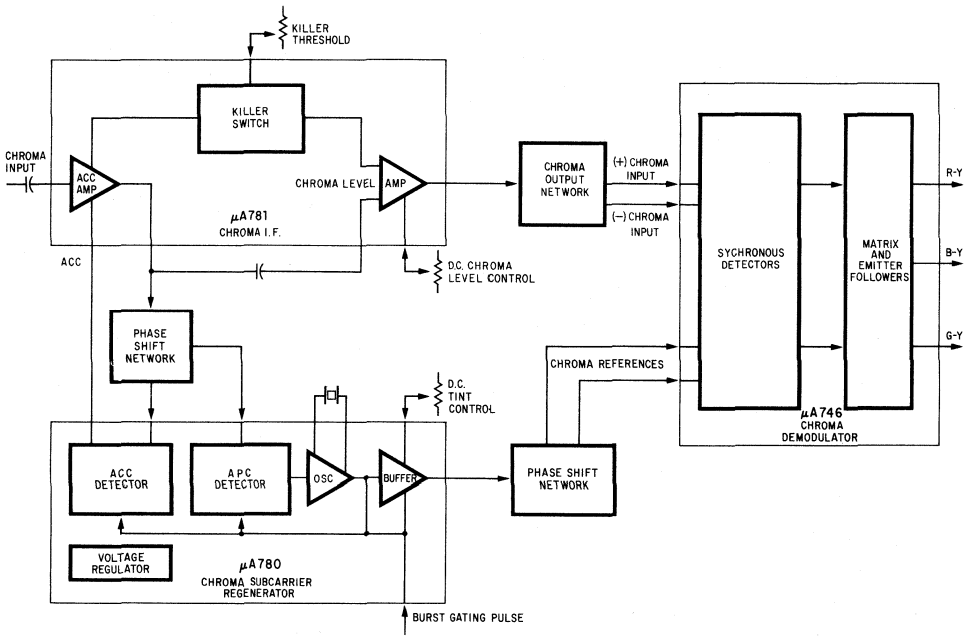


○ = Pin Numbers

INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM (COMPLETE SCHEMATIC)



INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM (BLOCK DIAGRAM)



μA781

GAIN CONTROLLED CHROMA AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA781 is a monolithic Gain Controlled IF Amplifier for color TV constructed using the Fairchild Planar* epitaxial process. The first section is a gain controlled chroma signal amplifier whose output is used to drive a subcarrier regenerator circuit. The gain of the second section is controlled by means of an external dc voltage to set chroma level. In addition, the second stage may be gated off to provide "color killing" action in the absence of a color signal with the trip point of the gate adjusted externally.

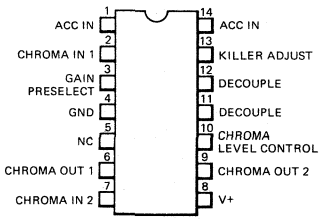
The μA781 in combination with the μA780 Phase Locked Loop Subcarrier Regenerator and the μA746 Chroma Demodulator forms a complete low cost, high quality chroma processing system for color TV receivers.

- **COMPLETE COLOR TV CHROMA IF AMPLIFIER**
- **10 MHz BANDWIDTH**
- **AUTOMATIC COLOR CONTROL (ACC) AMPLIFIER**
- **DC CHROMA LEVEL CONTROL**
- **ADJUSTABLE COLOR KILLER**
- **OUTPUT SHORT CIRCUIT PROTECTION**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	30 V
Internal Power Dissipation	670 mW
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Pin Temperature	
Molded DIP (Soldering, 10 s)	260°C
Output Short Circuit Duration	30 s

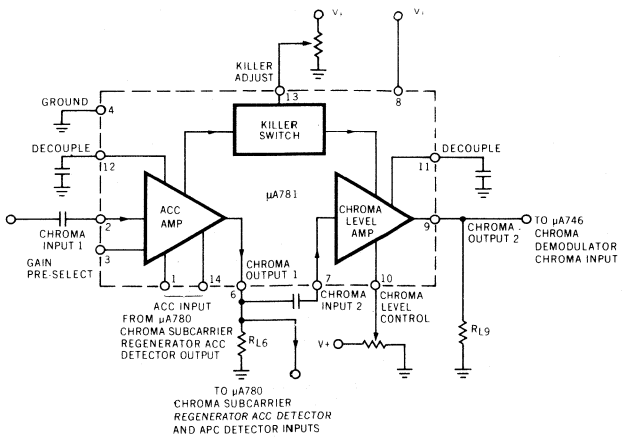
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9A
PACKAGE CODES P



ORDER INFORMATION

TYPE	PART NO.
μA781C	μA781PC

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

μA781C

ELECTRICAL CHARACTERISTICS (Note 1)

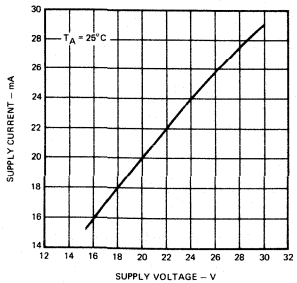
CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Supply Current	$R_{L6} = R_{L9} = 1\ M\Omega$ (Note 1)	8.0 17	13 24	18 31	mA mA
Internal Power Dissipation			400	550	mW
Short Circuit Load Current, Chroma Output 1	$R_{L6} = 0\ \Omega$	20	42		mA
Short Circuit Load Current, Chroma Output 2	$R_{L9} = 0\ \Omega$	20	36		mA
DC Voltage at Chroma Output 1 Terminal		15.5	17.5	20	V
DC Voltage at Chroma Output 2 Terminal		17.5	18	18.5	V
Gain, ACC Amplifier Stage		14	17	19	dB
Output Voltage Sensitivity of ACC Amplifier to ACC Control Voltage	$V_{ACC} = V_1 - V_{14} = 0$ mV to $V_1 - V_{14} = -75$ mV	11	14	16	$mV_{p-p}/mVdc$
Maximum Gain, Chroma Level Amplifier Stage		12	15.8	17	dB
DC Voltage at Chroma Level Control Terminal for 90% Maximum Output Level, Chroma Level Amplifier Stage	Chroma Level Control Set for 90% Maximum Output	3.0	5.0	5.5	V
DC Voltage at Chroma Level Control Terminal for 10% Maximum Output Level, Chroma Level Amplifier Stage	Chroma Level Control Wiper set for 10% of Maximum Output	17	19.5	22	V
Killer "ON" Threshold (Pin 13)			16.6	17	V
Killer "OFF" Threshold (Pin 13)		16	16.3		V
DC Voltage at Decouple Terminal, Pin 11		15	15.5	16	V
DC Voltage at Decouple Terminal, Pin 12		14.5	15.3	16	V
DC Voltage at Gain Preselect Terminal		0.7	1.0	1.2	V
DC Voltage at Chroma Input 1 Terminal			1.7		V
DC Voltage at Chroma Input 2 Terminal			1.4		V
Gain Change with Temperature, Chroma Level Amplifier Stage	$T_A = 25°C$ to $T_A = 70°C$ Adjust Input Level at Chroma Input 2 for Output Level = 1.0 V RMS at Maximum Gain. Set Chroma Level Control Wiper for Output Level = 100 mV RMS		0.7		dB
Chroma Input 1 Resistance			2.4		kΩ
Chroma Input 1 Capacitance			6.2		pF
Chroma Input 2 Resistance			2.4		kΩ
Chroma Input 2 Capacitance			4.2		pF

NOTE (1)

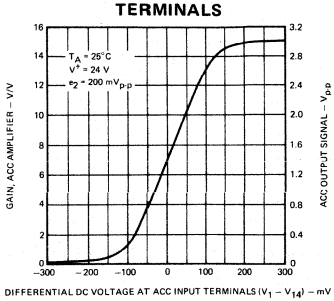
$T_A = 25°C$, $V^+ = 24$ V, $R_{L6} = 3.3$ kΩ, $R_{L9} = 2.7$ kΩ, Chroma Level Control Wiper at Ground, Voltage at ACC Input Terminals = 10 V, zero Differential Voltage between ACC Input Terminals, f = 3.58 MHz, Peak-to-Peak Input at Chroma Input 1 = 200 mV, Peak-to-Peak Input at Chroma Input 2 = 400 mV, unless otherwise specified. Refer to Test Circuit 1.

TYPICAL PERFORMANCE CURVES FOR μA781C

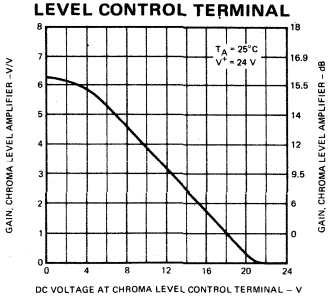
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



ACC AMPLIFIER GAIN AS A FUNCTION OF DIFFERENTIAL DC VOLTAGE AT ACC INPUT TERMINALS

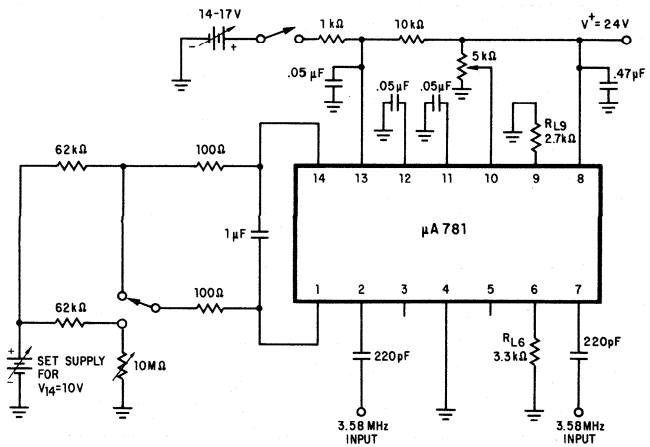


CHROMA LEVEL AMPLIFIER GAIN AS A FUNCTION OF DC VOLTAGE AT CHROMA LEVEL CONTROL TERMINAL

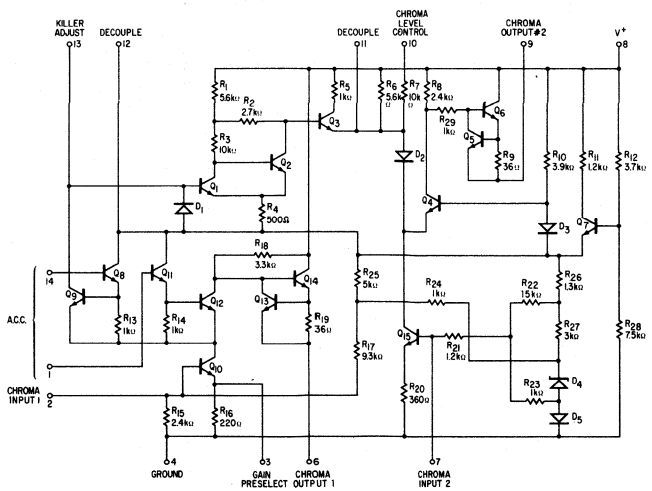


4

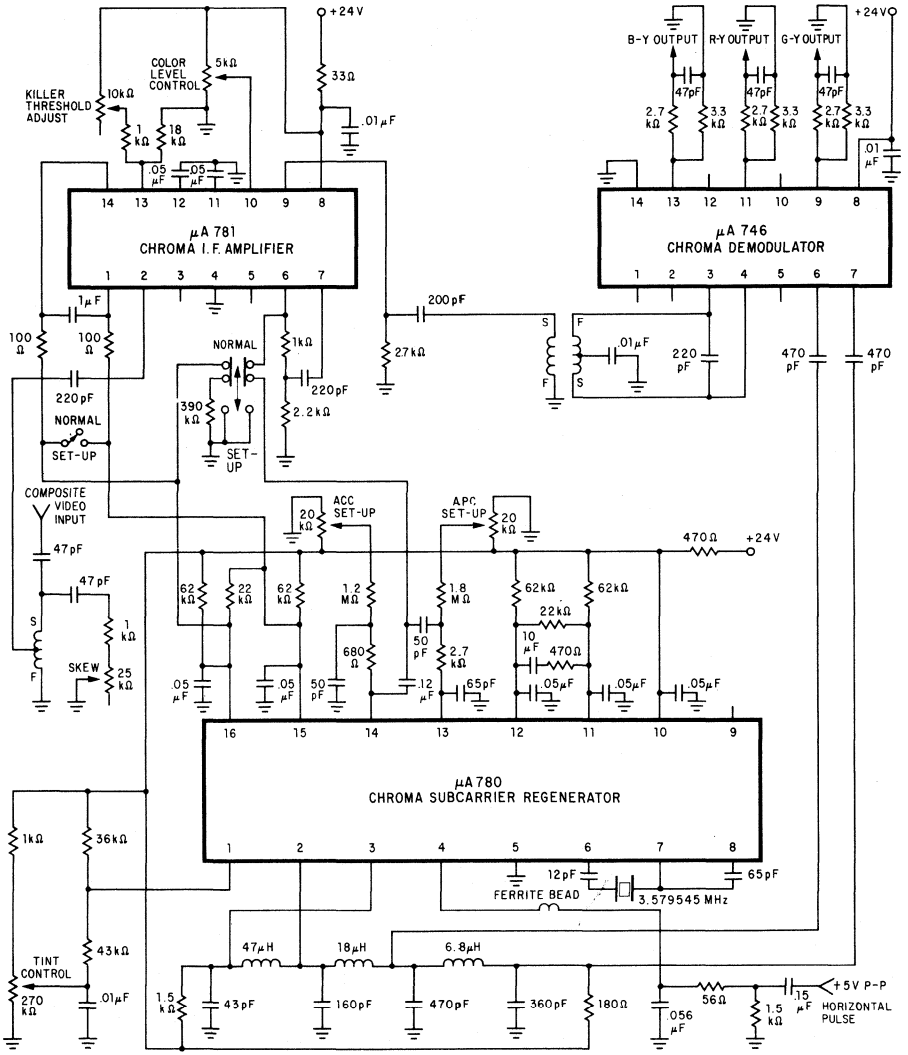
TEST CIRCUIT



EQUIVALENT CIRCUIT

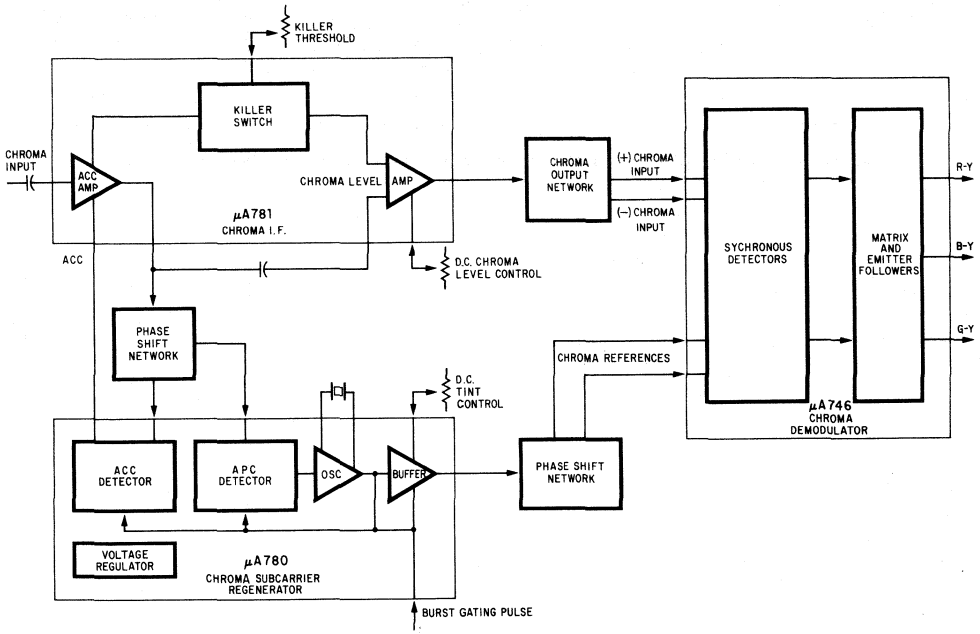


INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM



INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM

BLOCK DIAGRAM



μA783

9 WATT AUDIO POWER AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

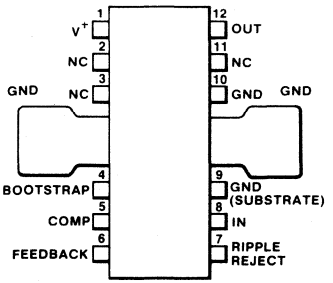
GENERAL DESCRIPTION — The μA783 is high-voltage monolithic integrated circuit in a 12-pin power package. It is constructed using the Fairchild Planar* epitaxial process. It is designed for use as a low frequency Class B power amplifier and is intended primarily for 8 Ω and 16 Ω applications. It typically provides 9 W into 8 ohms and 5 W into 16 ohms from a 24 V supply.

The μA783 is provided with two pin configurations (P3 and P4). Both devices are identical electrically.

The μA783 is pin for pin compatible with the TBA810S and TCA940.

- **THERMAL SHUTDOWN**
- **WIDE SUPPLY VOLTAGE RANGE (4 V to 30 V)**
- **HIGH CURRENT CAPABILITY (2.5 A)**
- **12-PIN POWER PACKAGE**

CONNECTION DIAGRAM
12-PIN POWER PACKAGE
(TOP VIEW)
PACKAGE OUTLINE 9W
PACKAGE CODES P3, P4



ABSOLUTE MAXIMUM RATINGS

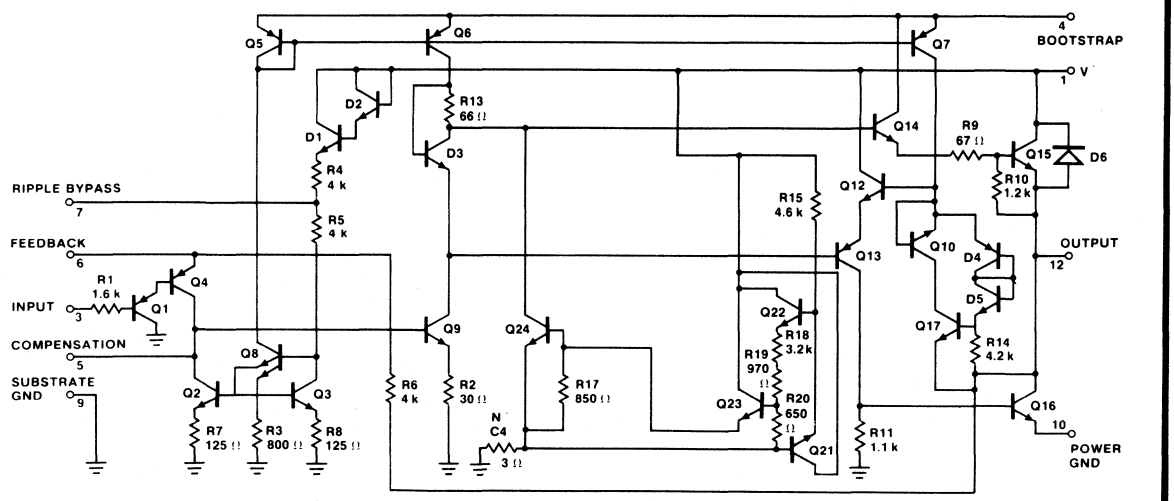
Supply Voltage	30 V
Output Peak Current (Non-Repetitive)	3.5 A
Output Current (Repetitive)	2.5 A
Input Voltage	220 mVrms
Power Dissipation: at T_A = 70°C	1.0 W
at T_C = 90°C	6.0 W
Storage and Junction Temperature	-40 to 150°C
Pin Temperature (Soldering, 10 s	260C

*Planar is a patented Fairchild process.

ORDER INFORMATION

TYPE	PART NO.
μA783C	μA783P3C
μA783C	μA783P4C

EQUIVALENT CIRCUIT



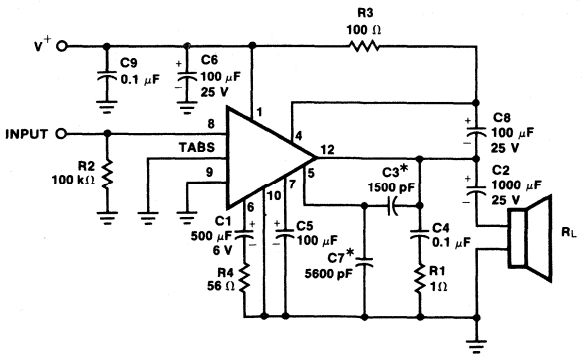
ELECTRICAL CHARACTERISTICS: Refer to the test circuit: $T_A = 25°C$

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Output Voltage (Pin 12)	V+ = 24.0 V	11.2	12.0	12.8	V
Quiescent Drain Current (Pin 1)			20.0	30.0	mA
Bias Current (Pin 8)			0.4		μA
Power Output	THD = 10% f = 1.0 kHz V+ = 24.0 V, R_L = 16 Ω V+ = 24.0 V, R_L = 8 Ω V+ = 14.4 V, R_L = 4 Ω V+ = 6.0 V, R_L = 4 Ω	8.0	 5.0 9.0 5.2 0.9		 W W W W
Input Sensitivity	P_{OUT} = 9 W, V+ = 24.0 V R_L = 8.0 Ω, f = 1.0 kHz R_f = 56 Ω R_f = 22 Ω		 147.0 60.0	 200.0	 mV mV
Input Resistance (Pin 8)			5.0		MΩ
Frequency Response (-3.0 dB)	V+ = 24.0 V, R_L = 8.0 Ω C3 = 820 pF C3 = 1500 pF		 20-30000 20-20000		 Hz Hz
Total Harmonic Distortion	P_{OUT} = 50 mW to 5 W, V+ = 24.0 V R_L = 8.0 Ω, f = 1.0 kHz		0.3		%
Voltage Gain (Open Loop)	V+ = 24.0 V, R_L = 8.0 Ω, f = 1.0 kHz		70.0		dB
Voltage Gain (Closed Loop)	V+ = 24.0 V, R_L = 8.0 Ω, f = 1.0 kHz	34.0	36.0	40.0	dB
Input Noise Voltage	V+ = 24.0 V, R_g = 0, BW (-3.0 dB) = 20 Hz to 20,000 Hz		3.0		μV
Input Noise Current	V+ = 24.0 V, BW (-3.0 dB) = 20 Hz to 20,000 Hz		0.15		nA
Efficiency	P_{OUT} = 9 W, V+ = 24.0 V, R_L = 8.0 Ω, f = 1.0 kHz		70.0		%
Supply Voltage Rejection	V+ = 24.0 V, R_L = 8.0 Ω f_{ripple} = 100 Hz		45.0		dB

THERMAL DATA			μA783P3	μA783P4
θ_{JC}	Thermal Resistance Junction to Case (tab)	MAX	12° C/W	10° C/W
θ_{JA}	Thermal Resistance Junction to Ambient	MAX	70° C/W**	80° C/W

**Obtained with tabs soldered to print circuit with minimized copper area.

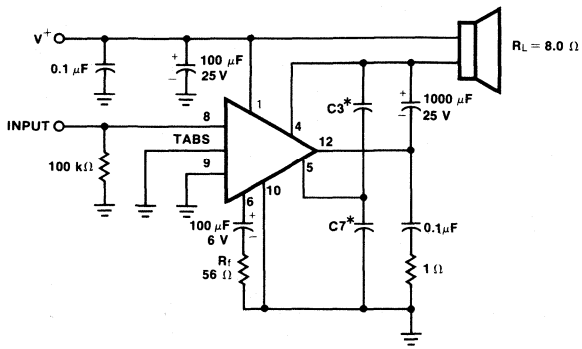
TEST AND APPLICATION CIRCUIT



*C3 and C7 See Figure 3

Figure 1

TYPICAL CIRCUIT WITH LOAD CONNECTED TO THE SUPPLY VOLTAGE



*C3 and C7 See Figure 3

Figure 2

TYPICAL VALUE OF C3 AS A FUNCTION OF R_f FOR VARIOUS VALUES OF BANDWIDTH

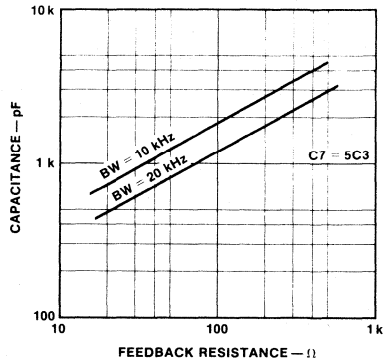


Figure 3

POWER OUTPUT AS A FUNCTION OF SUPPLY VOLTAGE

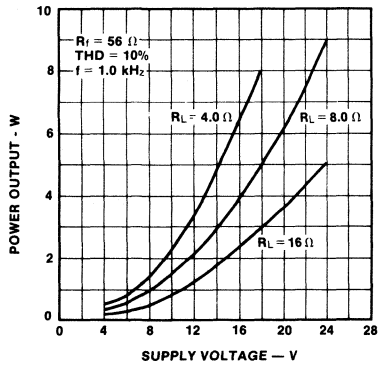


Figure 4

MAXIMUM POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE (SINE WAVE OPERATION)

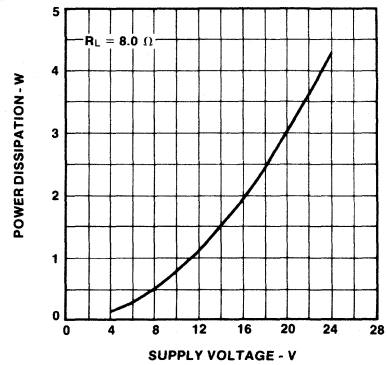


Figure 5

TOTAL HARMONIC DISTORTION AS A FUNCTION OF POWER OUTPUT

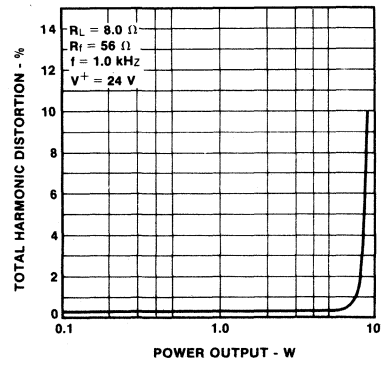


Figure 6

TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY

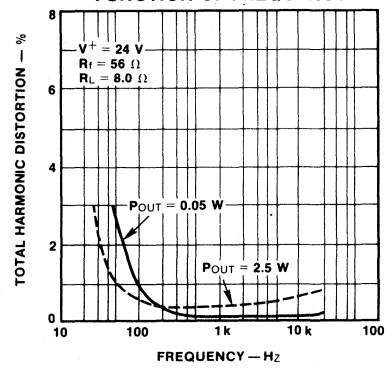


Figure 7

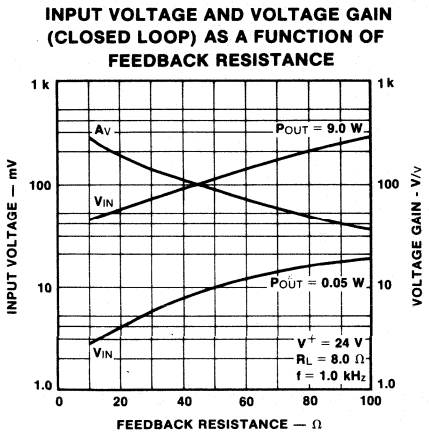


Figure 8

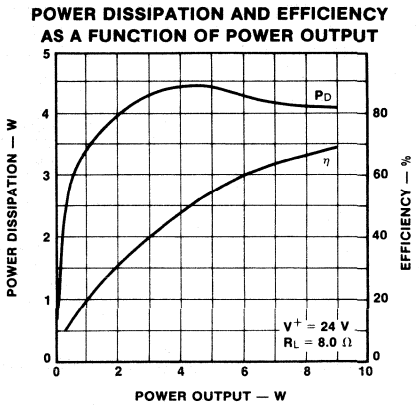


Figure 9

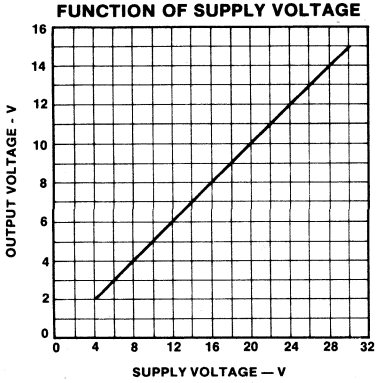


Figure 10

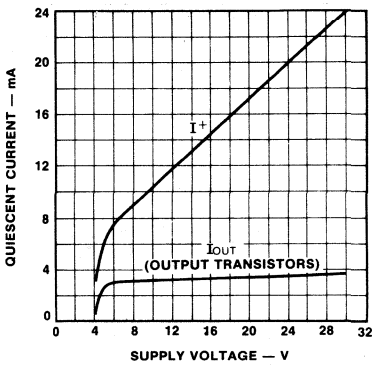


Figure 11

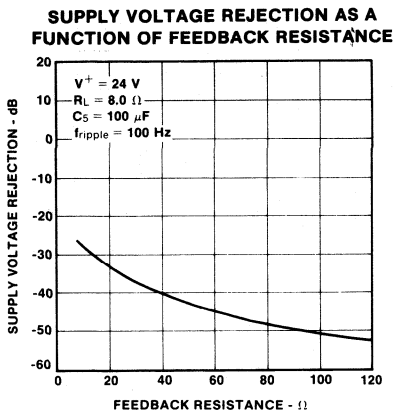


Figure 12

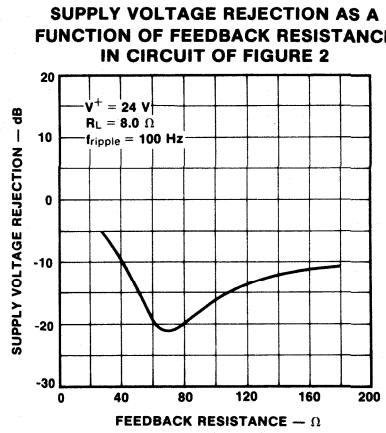


Figure 13

MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by connecting the tabs to an external heat sink (μA783P4C, Figure 14) or by soldering them to an area of copper on the printed circuit. (μA783P3C, Figure 15). During soldering, the tabs temperature must not exceed 230°C and the soldering time must not be longer than 12 seconds. Figures 16a and 16b show two ways that can be used for mounting the device.

MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (μA783P4C)

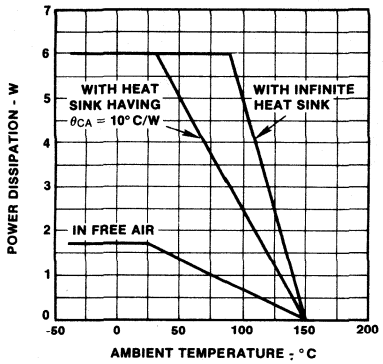
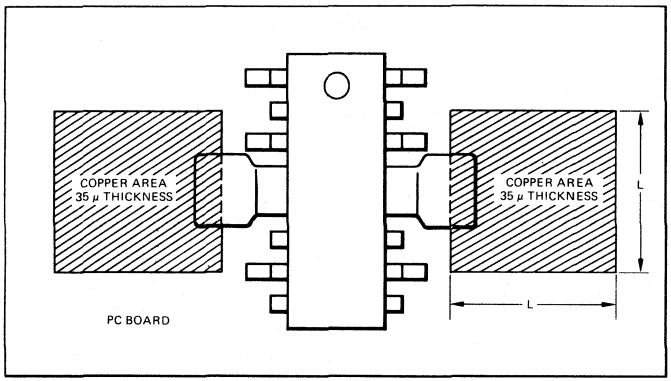


Figure 14

MAXIMUM POWER DISSIPATION AND TOTAL THERMAL RESISTANCE AS A FUNCTION OF COPPER AREA OF PC BOARD (μA783P3C)



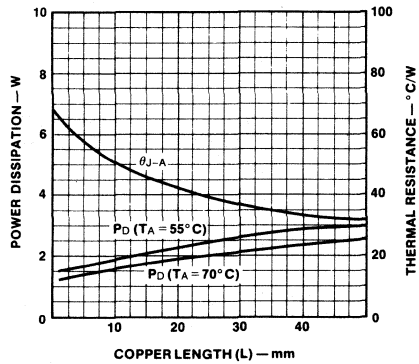


Figure 15

Figure 16a shows a method of mounting the μA783P3C that is satisfactory both from the point of view of heat dissipation and from mechanical considerations. For the μA783P4C, the desired thermal resistance is obtained attaching the hardware shown in Figure 16b, to a bracket with proper dimensions. This bracket can also act as a support for the whole printed circuit board.

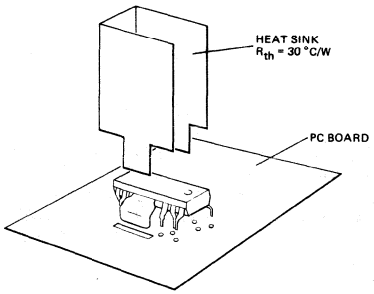


FIGURE 16a

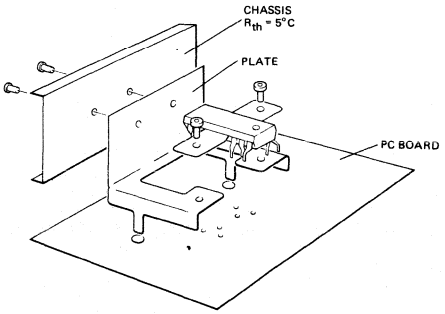


Figure 16b

4

THERMAL SHUTDOWN

The on chip design of the thermal limiting circuit offers the following advantages:

1. An overload on the output (even if permanent) or an above-limit ambient temperature can be easily handled.
2. The heat sink can have a smaller factor of safety compared with that of a conventional circuit. In case of too high a junction temperature, power output, power dissipation and the supply current decrease (Figure 17) thus protecting the device.

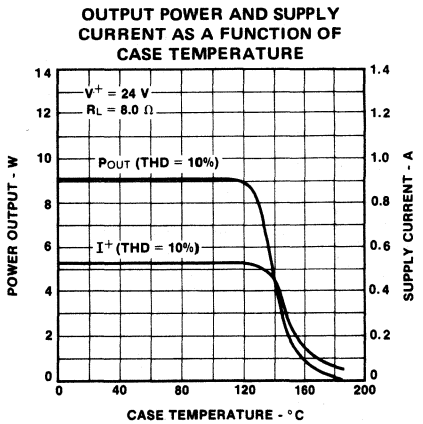


Figure 17

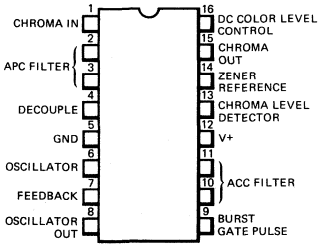
μA787
CHROMA PROCESSOR
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA787 is a monolithic color TV Chroma Processor circuit. It is constructed using the Fairchild Planar* epitaxial process. The device performs the entire chroma processing function in a color TV receiver. The μA787 interfaces with a variety of chroma demodulator circuits, e.g., μA746, 3067, and μA788. However, when teamed with the μA788 (chroma demodulator and dc tint control), it offers the most complete 2-chip chroma system, featuring reduced component count and minimum adjustments.

Automatic color level control, an additional feature of the μA787 controls the gain of the chroma bandpass amplifier by detection of the chroma level. ACC and ACL work in conjunction to give superior chroma performance under varying signal conditions.

- **GAIN CONTROLLED CHROMA BANDPASS AMPLIFICATION**
- **DC COLOR LEVEL CONTROL**
- **SYNCHRONOUS BURST LEVEL DETECTION (ACC)**
- **COLOR KILLER**
- **PHASE LOCKED CHROMA SUBCARRIER REGENERATION (APC)**
- **PEAK CHROMA LEVEL DETECTION (ACL)**
- **ACC AND COLOR KILLER ADJUSTMENTS NOT REQUIRED**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B
PACAKGE CODE P



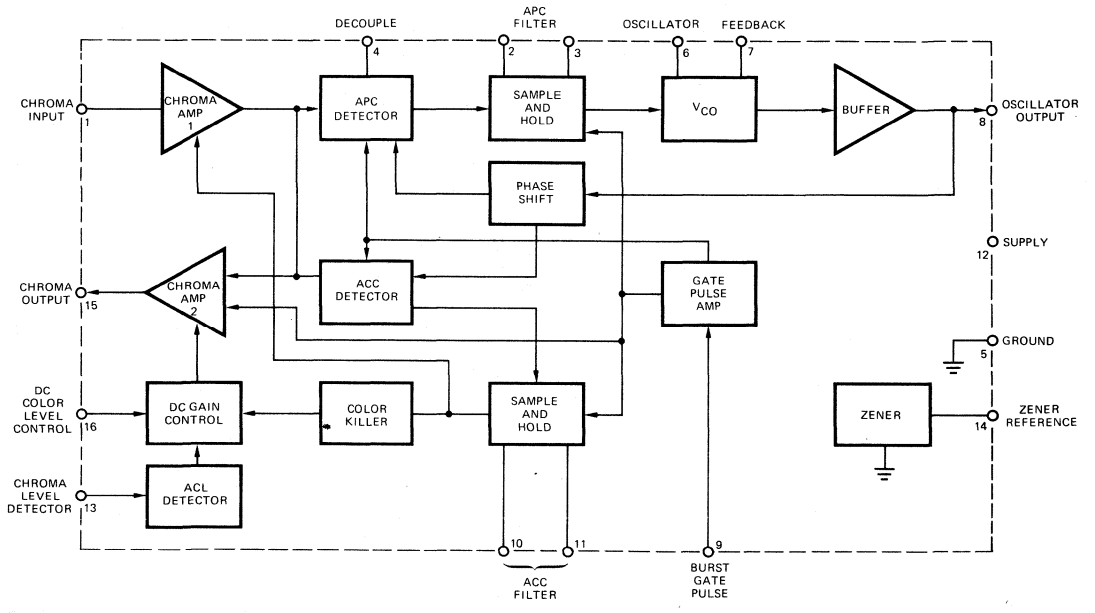
ORDER INFORMATION

TYPE	PART NO.
μA787	μA787PC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	14 V
Power Dissipation	730 mW
Current into Zener Reference Terminal	20 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature (soldering, 10 s)	260°C

BLOCK DIAGRAM

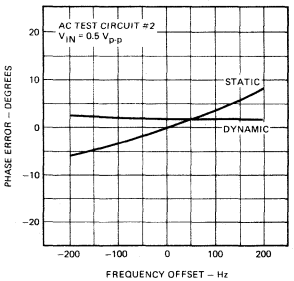


*Planar is a patented Fairchild process.

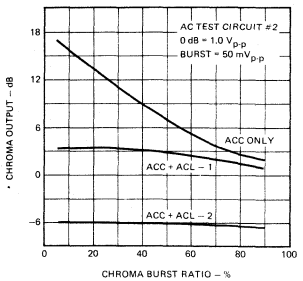
DC ELECTRICAL CHARACTERISTICS: T_A = 25°C, S1 and S2 normally open, Test Circuit 1, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current			26	36	mA
Zener Reference		11.1	11.9	12.7	V
Chroma Input			2.1		V
APC Filter			8.0		V
Decouple Bypass			7.5		V
Oscillator			8.0		V
Oscillator Feedback			2.0		V
Oscillator Output			7.6		V
Burst Gate Input	S2 Closed		1.7		V
ACC Filter			8.0		V
Chroma Level Detector			0.54		V
Chroma Output	S1, S2 Closed		6.2		V
AC CHARACTERISTICS: V_{12} = 11.2 V, S3 normally open, Test Circuit 2, unless otherwise specified.					
Oscillator Output	V_{IN} = 0	0.6	1.1	1.8	V_{p-p}
Chroma Output	V_{IN} = 0.5 V_{p-p}	1.5	2.5	4.0	V_{p-p}
Oscillator Pull In Range	V_{IN} = 0.5 V_{p-p}	200	400		Hz
Chroma Output	S3 Closed		450		mV_{p-p}
Chroma Input Level for Color Killer Threshold		5.0	20	50	mV_{p-p}

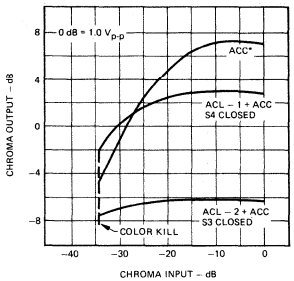
DYNAMIC AND STATIC PHASE ERROR AS A FUNCTION OF FREQUENCY OFFSET



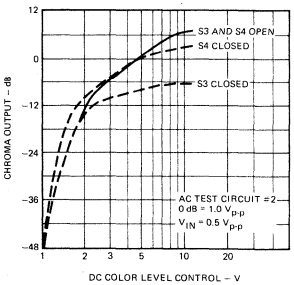
CHROMA OUTPUT AS A FUNCTION OF CHROMA BURST MODULATION RATIO



CHROMA OUTPUT AS A FUNCTION OF CHROMA INPUT

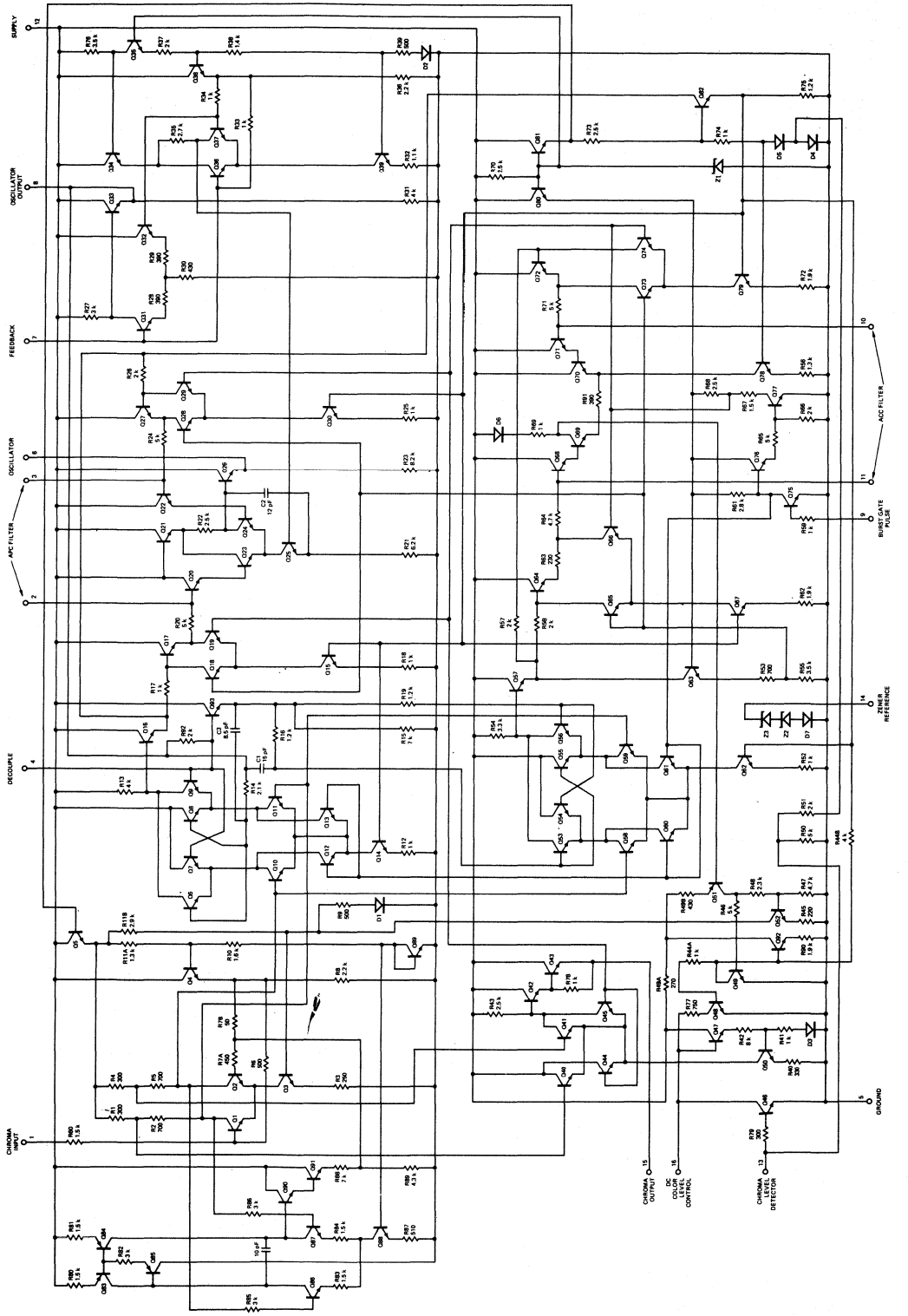


CHROMA OUTPUT AS A FUNCTION OF DC COLOR LEVEL CONTROL VOLTAGE

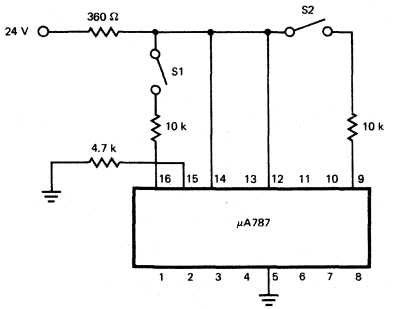


ACC — Output controlled by ACC only
ACL – 1 — Output partially controlled by ACL
ACL – 2 — Output fully controlled by ACL

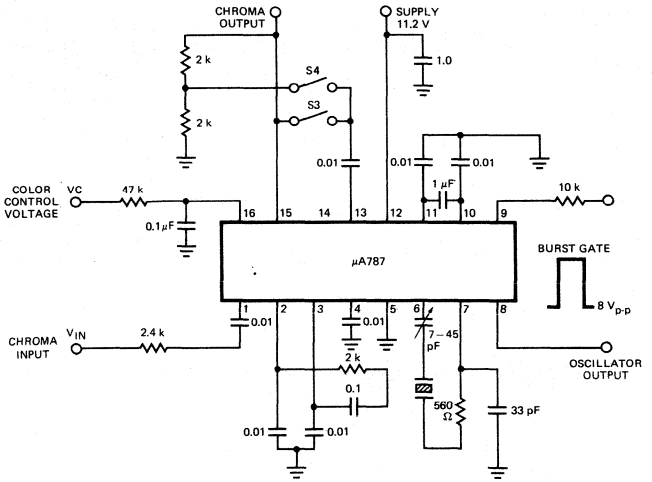
EQUIVALENT CIRCUIT



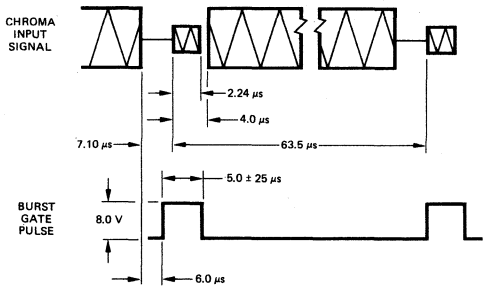
DC TEST CIRCUIT 1



AC TEST CIRCUIT 2



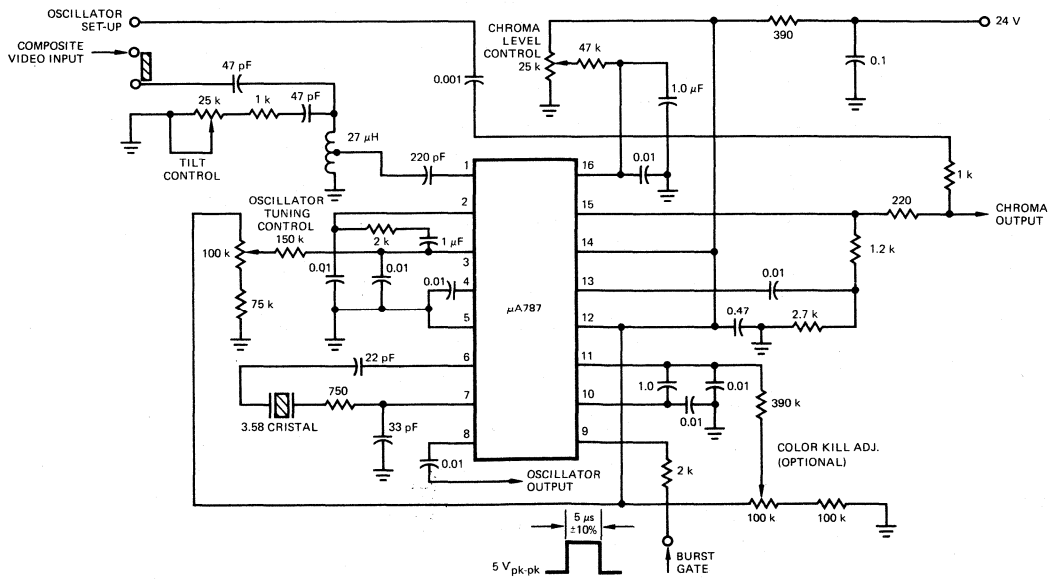
AC TEST SIGNAL (V_{IN})



Burst: 8 Cycles –3.58 MHz amplitude is 46.5% of chrominance with first and last cycle being at least 85% full amplitude. Amplitude of remaining cycles shall be within 5% of specification value. Chroma amplitude is 0.5 V Peak-to-Peak.

NOTES
1. Burst position during blanking interval may be altered if necessary.
2. Chrominance duration is 52 μs.
3. Burst gate pulse applied to test circuit is timed to coincide with burst.

TYPICAL APPLICATION



μA788

TV CHROMA DEMODULATOR AND DC TINT CONTROL

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA788 is a monolithic chroma demodulator with a dc tint control. It is constructed using the Fairchild Planar* epitaxial process. The device adds the luminance and color difference signals and provides direct coupled color signals to the video output drivers. The tint control section of the IC has a constant amplitude output with dc phase control.

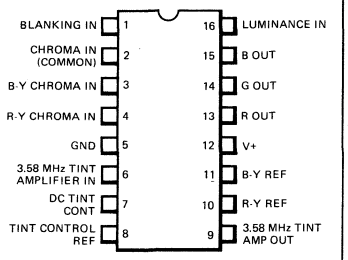
The μA788 will interface with several chroma processing systems, e.g., 3066 or μA780/μA781, but is intended to complement the μA787 chroma processing IC to form a 2-chip chroma system with optimum performance.

- **10 V PEAK-TO-PEAK BLUE OUTPUT**
- **INTERNAL SUBCARRIER FILTERING**
- **COLOR DIFFERENCE OR RGB SIGNALS AT THE OUTPUT**
- **LUMINANCE SIGNAL INPUT**
- **HORIZONTAL RETRACE BLANKING PULSE INPUT**
- **DC TINT CONTROL**
- **TINT RANGE ADJUSTABLE TO 150°**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+)	28 V
Power Dissipation	730 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature Molded DIP (soldering, 10 s)	260°C
Luminance Input Voltage	Supply Voltage (V+)
Minimum Tint Control Reference Load Resistance (Pin 8)	8.0 kΩ
Minimum Output Load Resistance (Pins 9, 13, 14, 15)	3.0 kΩ
Peak-to-Peak Reference Voltage (Pins 10, 11)	5.0 V
Peak-to-Peak Chroma Voltage (Pins 2, 3, 4)	5.0 V
Blanking Input Voltage	−3.0 V to +7.0 V

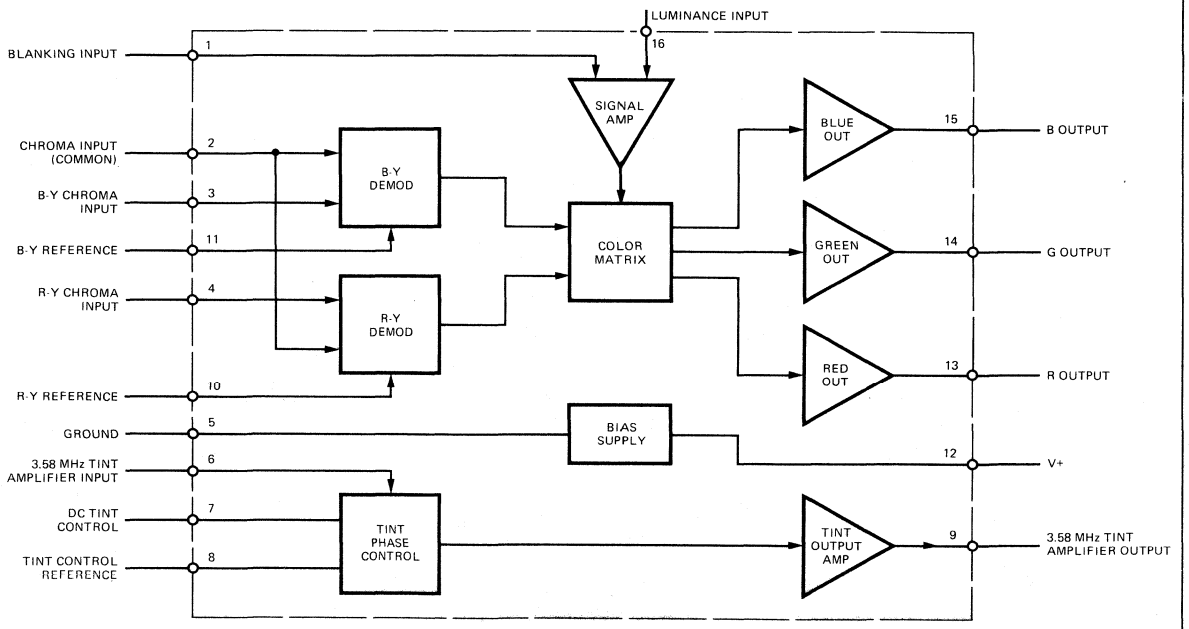
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B
PACKAGE CODE P



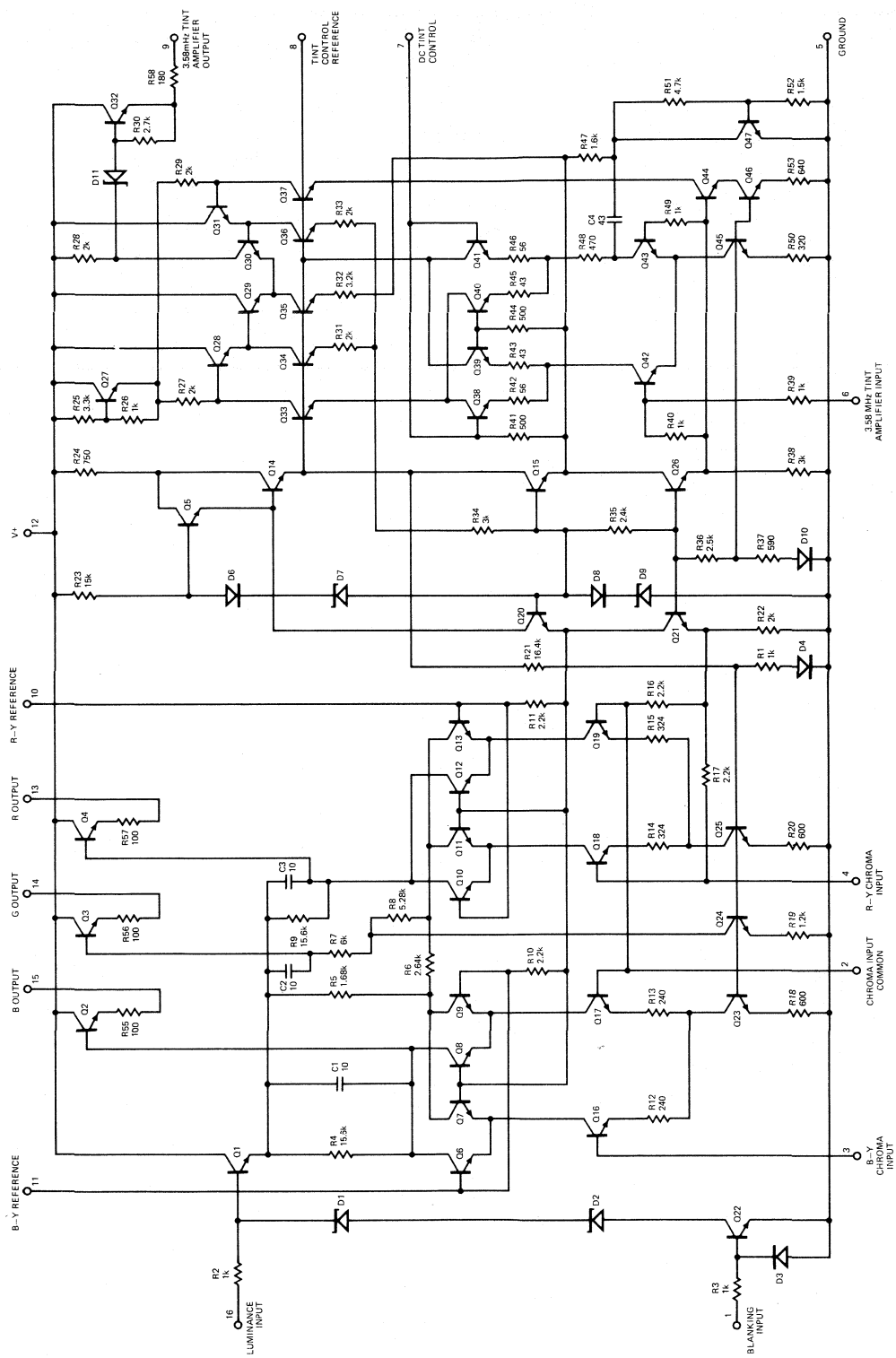
ORDER INFORMATION

TYPE	PART NO.
788	μA788PC

BLOCK DIAGRAM



EQUIVALENT CIRCUIT



ALL RESISTOR VALUES ARE IN OHMS AND ALL CAPACITOR VALUES ARE IN PICO FARADS.

DC CHARACTERISTICS: $T_A = 25°C$, V+ = 24 V, Test Circuit 1, unless otherwise specified.

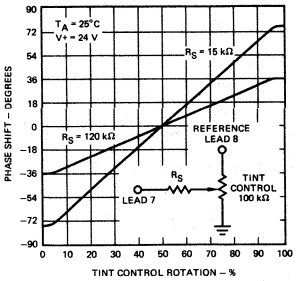
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
DC Bias Voltages					
Blanking Input (V1)	S1 Closed		1.2		V
Common Chroma Input (V2)			3.0		V
B-Y, R-Y Chroma Input (V3, V4)			3.0		V
3.58 MHz Tint Input (V6)			3.0		V
DC Tint Phase Control Input (V7)			5.6		V
Tint Phase Control Reference (V8)			11.2		V
3.58 MHz Tint Output (V9)			16		V
R-Y, B-Y Reference Input (V10, V11)			5.6		V
Demodulator Output (V13, V14, V15)		13	14.5	16	V
Luminance Input (V16)			23.8		V
Supply Current			25	33	mA
Blanking Input Current (I1)	V1 = 5.0 V		4.5		mA
Luminance Input Resistance (Pin 16)			100		kΩ
Chroma Input Resistance (Pins 2, 3, 4)			2.0		kΩ
Chroma Input Capacitance (Pins 2, 3, 4)			5.0		pF
Reference Input Resistance (Pins 10, 11)			2.0		kΩ
Reference Input Capacitance (Pins 10, 11)			6.0		pF
3.58 MHz Tint Amp Input Resistance (Pin 6)			2.0		kΩ
3.58 MHz Tint Amp Input Capacitance (Pin 6)			3.0		pF
3.58 MHz Tint Amp Output Resistance (Pin 9)			200		Ω
Demodulator Output Temperature Coefficient (V13, V14, V15)			−3.0		mV/°C

AC CHARACTERISTICS: $T_A = 25°C$, V+ = 24 V, Test Circuit 2, unless otherwise specified.

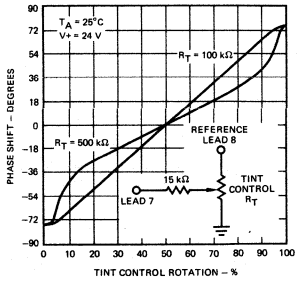
Tint Amp Output Voltage (V9)		1.0	2.0		V_{p-p}
Maximum Available Tint Range			150		Degrees
Blue Output Voltage	Chroma Input V3 = V4 = 0.7 V_{p-p}	6.0	8.0		V_{p-p}
B-Y Demodulator Conversion Gain	Blue Output V15 = 5.0 V_{p-p}	10	16		V/V
Demodulator Output Gain Relative to B-Y Output (V15)	B-Y Output (V15) Normalized to 1.0				
R-Y Output (V13)		0.65	0.76	0.84	
G-Y Output (V14)		0.15	0.20	0.25	
Demodulator Output Phase Angle Relative to B-Y Output	B-Y Output Phase Normalized to 0°				
R-Y Output (V13)		101	106	111	Degrees
G-Y Output (V14)		248	256	264	Degrees
Differential Voltage Between Any Two Demodulator Outputs (V13, V14, V15)	Chroma Input = 0		0.3		V
Demodulator ac Unbalance Voltage (V13, V14, V15)	Chroma Input = 0		0.2		V_{p-p}
Gain From Luminance Input	S2 Closed				
(Lead 16) to Demodulator Outputs	f = 1.0 kHz		0.95		V/V
	f = 5.0 MHz		0.5		V/V

TYPICAL PERFORMANCE CURVES

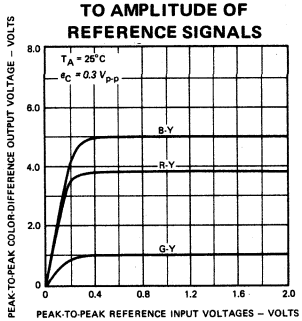
TINT CONTROL – RANGE



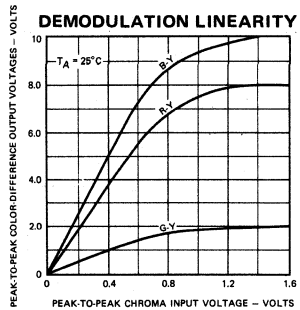
TINT CONTROL – LINEARITY



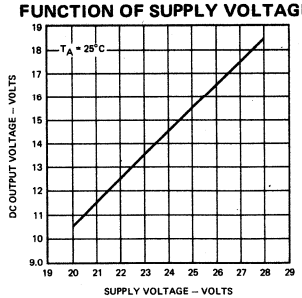
DEMODULATION SENSITIVITY TO AMPLITUDE OF REFERENCE SIGNALS



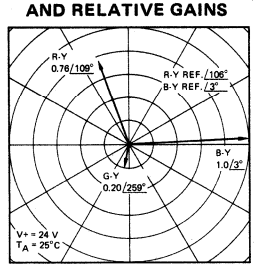
DEMODULATION LINEARITY



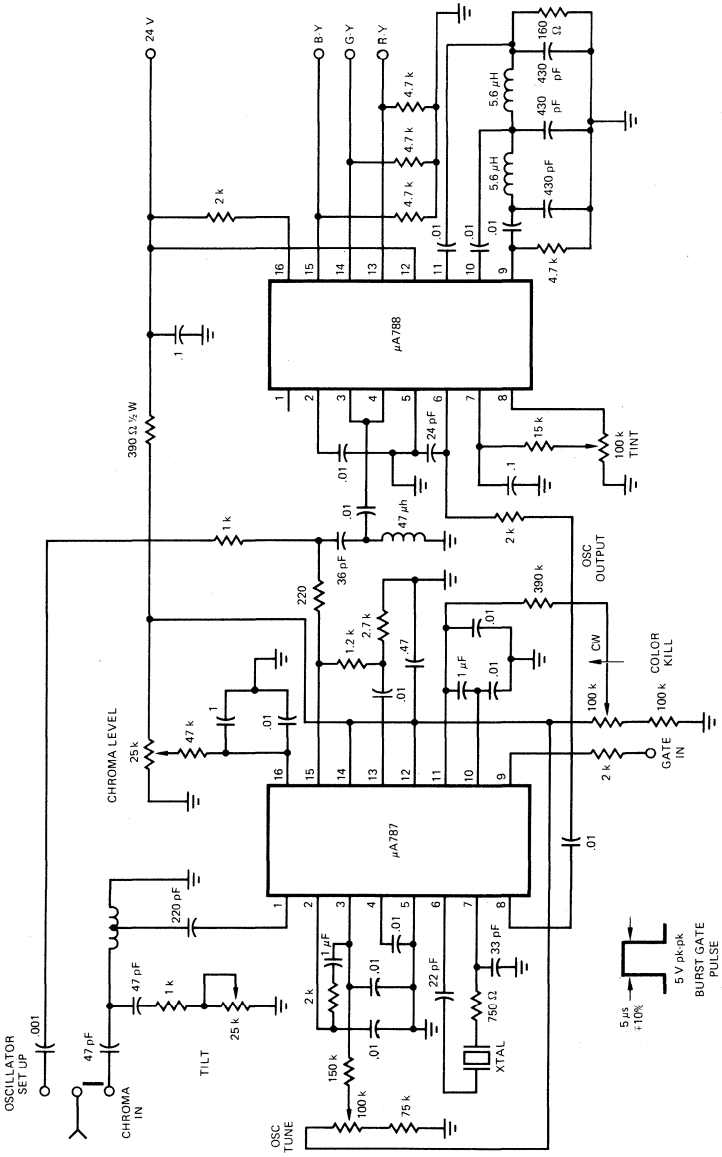
DC VOLTAGE AT ANY DEMODULATOR OUTPUT AS A FUNCTION OF SUPPLY VOLTAGE



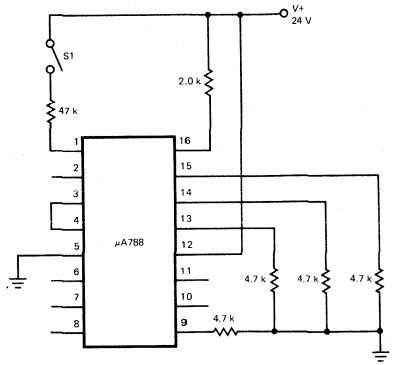
DEMODULATION ANGLES AND RELATIVE GAINS



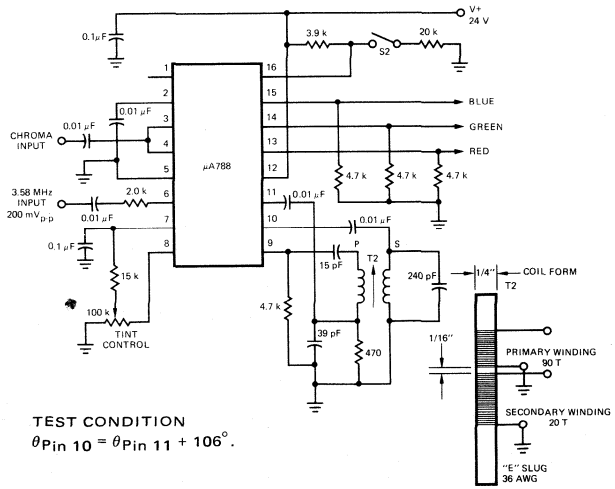
TYPICAL APPLICATION



TEST CIRCUIT 1



TEST CIRCUIT 2



TEST CONDITION

$\theta_{Pin\ 10} = \theta_{Pin\ 11} + 106^{\circ}$.

μA796

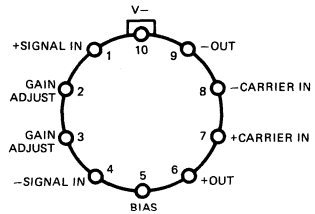
DOUBLE-BALANCED MODULATOR/DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA796 is a monolithic Double-Balanced Modulator/Demodulator using the Fairchild Planar* epitaxial process. This circuit produces an output voltage which is the product of an input voltage (signal) and a switching function (carrier). Communications applications include modulation and demodulation of AM, SSB, DSB, FSK, FM and phase encoded signals. Signal conditioning techniques possible include frequency doubling and halving, linear mixing and chopping, with additional uses as phase detectors in phase locked loops and as differentiators in NRZ and phase encoded digital tape and disk memories.

- **EXCELLENT CARRIER SUPPRESSION**
- **LOW OFFSETS AND DRIFT**
- **FULLY BALANCED INPUTS AND OUTPUT**
- **USEFUL TO 100 MHz**
- **WIDE RANGE OF APPLICATION**

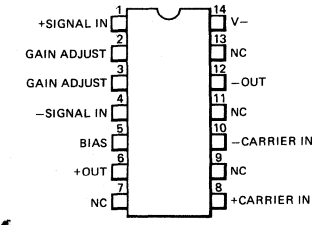
CONNECTION DIAGRAMS
10-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5Q
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA796	μA796HM
μA796C	μA796HC

14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9A
PACKAGE CODE P



ORDER INFORMATION

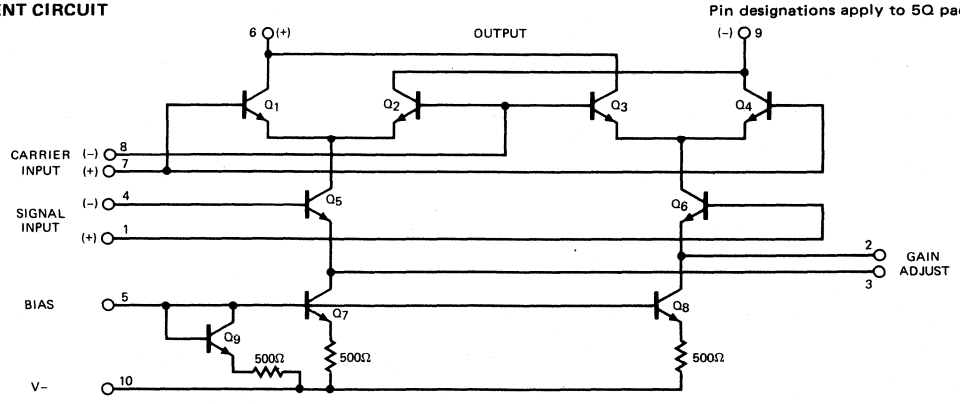
TYPE	PART NO.
μA796C	μA796PC

ABSOLUT MAXIMUM RATINGS

Internal Power Dissipation (Note 1)	500 mW
Applied Voltage (Note 2)	30 V
Differential Input Signal ($V_7 - V_8$)	±5.0 V
Differential Input Signal ($V_4 - V_1$)	$\pm(5 + I_5R_e)$ V
Input Signal ($V_2 - V_1$, $V_3 - V_4$)	5.0 V
Bias Current (I_5)	12 mA
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range (μA796)	–55°C to +125°C
Operating Temperature Range (μA796C)	0°C to +70°C
Pin Temperature (Soldering, 10 s)	300°C

EQUIVALENT CIRCUIT

Pin designations apply to 5Q package only



Notes on following pages.

*Planar is a patented Fairchild process.

μA796

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, Figure 1 unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Carrier Feedthrough	V_C = 60 mV (rms) sine wave f_C = 1.0 kHz, offset adjusted		40		μV (rms)
	V_C = 60 mV (rms) sine wave f_C = 10 MHz, offset adjusted		140		μV (rms)
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset adjusted		0.04	0.2	mV (rms)
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset not adjusted		20	100	mV (rms)
Carrier Suppression	f_S = 10 kHz, 300 mV (rms) f_C = 500 kHz, 60 mV (rms) sine wave offset adjusted	50	65		dB
	f_S = 10 kHz, 300 mV (rms) f_C = 10 MHz, 60 mV (rms) sine wave offset adjusted		50		dB
Transadmittance Bandwdith	R_L = 50Ω Carrier Input Port, V_C = 60 mV (rms) sine wave f_S = 1.0 kHz, 300 mV (rms) sine wave		300		MHz
	Signal Input Port, V_S = 300 mV (rms) sine wave $V_7 - V_8$ = 0.5 V dc		80		MHz
Voltage Gain, Signal Channel	V_S = 100 mV (rms), f = 1.0 kHz $V_7 - V_8$ = 0.5 V dc	2.5	3.5		V/V
Input Resistance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 V dc		200		kΩ
Input Capacitance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 V dc		2.0		pF
Single Ended Output Resistance	f = 10 MHz		40		kΩ
Single Ended Output Capacitance	f = 10 MHz		5.0		pF
Input Bias Current	$(I_1 + I_4)/2$		12	25	μA
Input Bias Current	$(I_7 + I_8)/2$		12	25	μA
Input Offset Current	$(I_1 - I_4)$		0.7	5.0	μA
Input Offset Current	$(I_7 - I_8)$		0.7	5.0	μA
Average Temperature Coefficient of Input Offset Current	$(-55°C < T_A < +125°C)$		2.0		nA/°C
Output Offset Current	$(I_6 - I_9)$		14	50	μA
Average Temperature Coefficient of Output Offset Current	$(-55°C < T_A < +125°C)$		90		nA/°C
Signal Port Common Mode Input Voltage Range	f_S = 1.0 kHz		5.0		V_{p-p}
Signal Port Common Mode Rejection Ratio	$V_7 - V_8$ = 0.5 V dc		-85		dB
Common Mode Quiescent Output Voltage			8.0		Vdc
Differential Output Swing Capability			8.0		V_{p-p}
Positive Supply Current	$(I_6 + I_9)$		2.0	3.0	mA
Negative Supply Current	(I_{10})		3.0	4.0	mA
Power Dissipation			33		mW

NOTES:
1. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C.
2. Voltage applied between 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.

μA796C

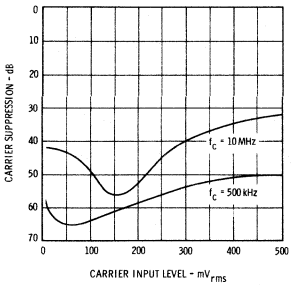
ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, Figure 1 unless otherwise specified

CHARACTERISTICS	CONDITIONS (Pin designations apply to metal can package only)	MIN	TYP	MAX	UNITS
Carrier Feedthrough	V_C = 60 mV (rms) sine wave f_C = 1.0 kHz, offset adjusted		40		μV rms
	V_C = 60 mV (rms) sine wave f_C = 10 MHz, offset adjusted		140		μV rms
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset adjusted		0.04	0.2	mV rms
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset not adjusted		20	150	mV rms
Carrier Suppression	f_S = 10 kHz, 300 mV (rms) f_C = 500 kHz, 60 mV (rms) sine wave offset adjusted	50	65		dB
	f_S = 10 kHz, 300 mV (rms) f_C = 10 MHz, 60 mV (rms) sine wave offset adjusted		50		dB
Transadmittance Bandwidth	R_L = 50Ω Carrier Input Port, V_C = 60 mV (rms) sine wave f_S = 1.0 kHz, 300 mV (rms) sine wave		300		MHz
	Signal Input Port, V_S = 300 mV (rms) sine wave $V_7 - V_8$ = 0.5 V dc		80		MHz
Voltage Gain, Signal Channel	V_S = 100 mV (rms), f = 1.0 kHz $V_7 - V_8$ = 0.5 V dc	2.5	3.5		V/V
Input Resistance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 V dc		200		kΩ
Input Capacitance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 V dc		2.0		pF
Single Ended Output Resistance	f = 10 MHz		40		kΩ
Single Ended Output Capacitance	f = 10 MHz		5.0		pF
Input Bias Current	$(I_1 + I_4)/2$		12	30	μA
	$(I_7 + I_8)/2$		12	30	μA
Input Offset Current	$(I_1 - I_4)$		0.7	5.0	μA
	$(I_7 - I_8)$		0.7	5.0	μA
Average Temperature Coefficient of Input Offset Current	$0°C \leq T_A \leq +70°C$		2.0		nA/°C
Output Offset Current	$(I_6 - I_9)$		14	60	μA
Average Temperature Coefficient of Output Offset Current	$0°C < T_A < +70°C$		90		nA/°C
Signal Port Common Mode Input Voltage Range	f_S = 1.0 kHz		5.0		V_{p-p}
Signal Port Common Mode Rejection Ratio	$V_7 - V_8$ = 0.5 V dc		–85		dB
Common Mode Quiescent Output Voltage			8.0		Vdc
Differential Output Swing Capability			8.0		V_{p-p}
Positive Supply Current	$(I_6 + I_9)$		2.0	3.0	mA
Negative Supply Current	(I_{10})		3.0	4.0	mA
Power Dissipation			33		mW

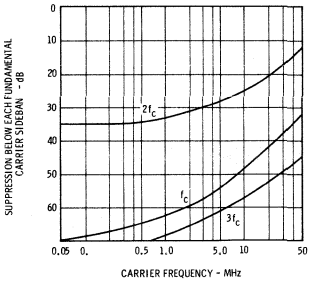
NOTES
1. Rating applies to ambient temperatures up to 70°C.
2. Voltage applied between pins 6-7, 8-1, 9-7, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.

TYPICAL PERFORMANCE CURVES FOR μA796

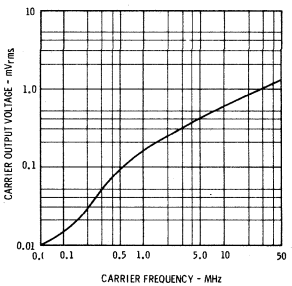
CARRIER SUPPRESSION AS A FUNCTION OF CARRIER INPUT LEVEL



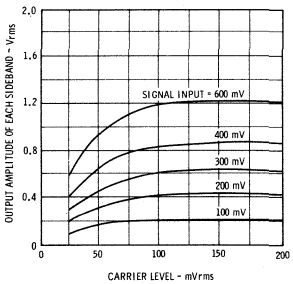
CARRIER SUPPRESSION AS A FUNCTION OF FREQUENCY



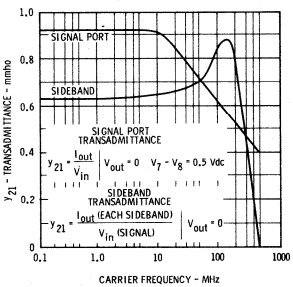
CARRIER FEEDTHROUGH AS A FUNCTION OF FREQUENCY



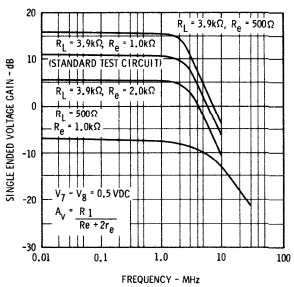
SIGNAL-PORT FREQUENCY RESPONSE



SIDEBAND OUTPUT AS A FUNCTION OF CARRIER LEVELS

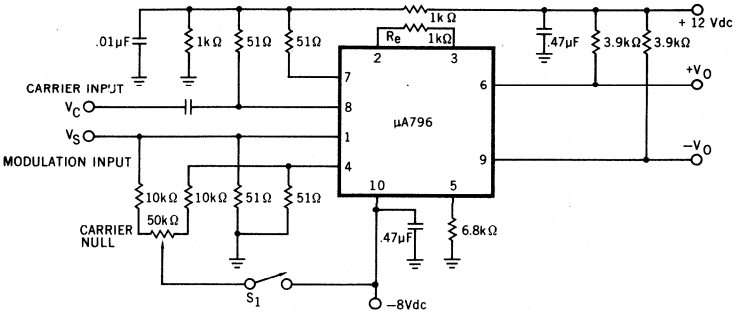


SIDEBAND AND SIGNAL PORT TRANSADMITTANCES AS A FUNCTION OF FREQUENCY



TYPICAL APPLICATIONS

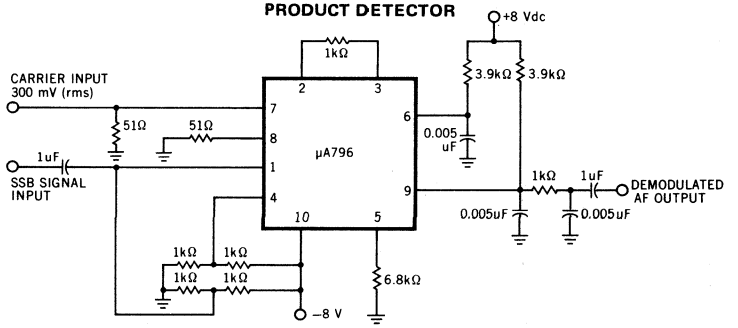
TYPICAL MODULATOR CIRCUIT



Note: S_1 is closed for "adjusted" measurements.

Fig. 1

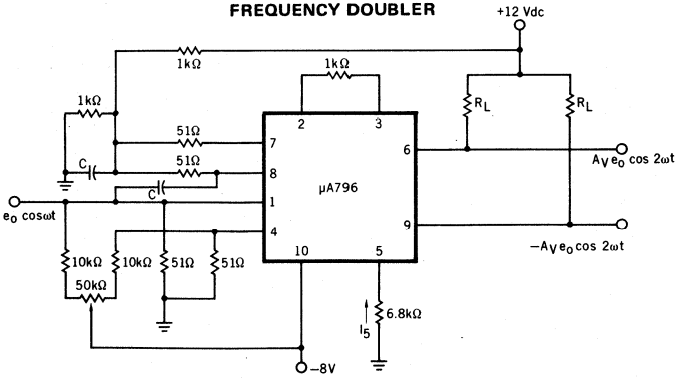
PRODUCT DETECTOR



This figure shows the μA796 used as a single sideband (SSB) suppressed carrier demodulator (product detector). The carrier signal is applied to the carrier input port with sufficient amplitude for switching operation. A carrier input level of 300 mV(rms) is optimum. The composite SSB signal is applied to the signal input port with an amplitude of 5.0 to 500 mV(rms). All output signal components except the desired demodulated audio are filtered out, so that an offset adjustment is not required. This circuit may also be used as an AM detector by applying composite and carrier signals in the same manner as described for product detector operation.

Fig. 2

FREQUENCY DOUBLER



The frequency doubler circuit shown will double low-level signals with low distortion. The value of C should be chosen for low reactance at the operating frequency.

Signal level at the carrier input must be less than 25 mV peak to maintain operation in the linear region of the switching differential amplifier. Levels to 50 mV peak may be used with some distortion of the output waveform. If a larger input signal is available a resistive divider may be used at the carrier input, with full signal applied to the signal input.

Fig. 3

μA1310

PHASE LOCKED LOOP FM STEREO MULTIPLEX DECODER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA1310 is a monolithic FM Stereo Multiplex Decoder System constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This integrated circuit decodes an FM stereo multiplex signal into right and left audio channels, while inherently suppressing SCA information when it is contained in the composite input signal.

The μA1310 operates over a wide supply voltage range and uses a low number of external components. It has only one control to adjust: a potentiometer to set oscillator frequency. No external coils are required.

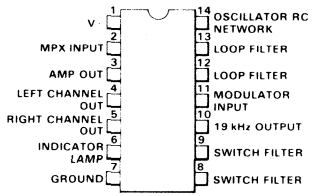
- **LOW DISTORTION (THD) – 0.3% TYP**
- **EXCELLENT SCA REJECTION – 75 dB TYP**
- **HIGH CHANNEL SEPARATION – 40 dB**
- **WIDE SUPPLY VOLTAGE RANGE – 8 TO 14 V DC**
- **SINGLE ADJUSTMENT FOR COMPLETE ALIGNMENT**
- **LOW EXTERNAL COMPONENT COUNT – NO COILS**
- **AUTOMATIC STEREO/MONAURAL SWITCHING**
- **STEREO INDICATOR LAMP DRIVER WITH CURRENT LIMITING**

ABSOLUTE MAXIMUM RATINGS: T_A = 25°C unless otherwise noted

Power Supply Voltage	14 V
Lamp Current	75 mA
Power Dissipation (Package Limitation)	625 mW
Derate above T_A = 25°C	5.0 mW/°C
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Pin Temperature (Soldering, 10 s)	260°C

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

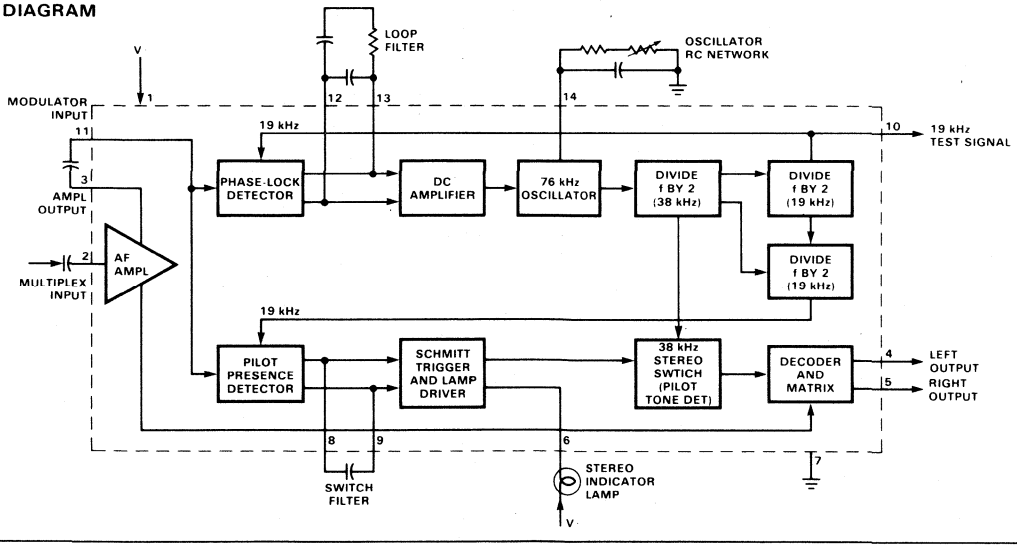
PACKAGE OUTLINE 9A
PACKAGE CODE P



ORDER INFORMATION

TYPE	PART NO.
μA1310	μA1310PC

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: V+ = 12 V, T_A = 25°C, 560 mV(RMS) (28 V_{p-p}) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) pilot level (10%) using circuit of Figure 1, unless otherwise noted.

CHARACTERISTICS	MIN	TYP	MAX	UNITS
Maximum Standard Composite Input Signal (0.5% THD)	2.8			$V_{(p-p)}$
Maximum Monaural Input Signal (1.0% THD)	2.8			$V_{(p-p)}$
Input Impedance	20	50		kΩ
Stereo Channel Separation	30	40		dB
Audio Output Voltage (desired channel)		485		mV(RMS)
Monaural Channel Balance (pilot tone OFF)			1.5	dB
Total Harmonic Distortion		0.3		%
Ultrasonic Frequency Rejection (19 kHz) (38 kHz)		34.4 45		dB dB
Inherent SCA Rejection (f = 67 kHz; 9.0 kHz beat note measured with 1.0 kHz modulation OFF)		75		dB
Stereo Switch Level (19 kHz input level for lamp ON) (19 kHz input level for lamp OFF)	 5.0		20	mV(RMS)
Capture Range (permissible tuning error of internal oscillator, reference circuit values of Fig. 1)		±3.5		%
Current Drain (lamp OFF)		13		mA

TYPICAL APPLICATION

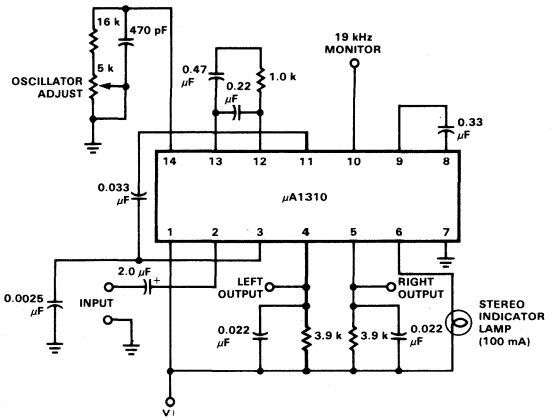


Fig. 1

μA1391•μA1394

TV HORIZONTAL PROCESSOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA1391 is an integrated circuit which performs the low level horizontal processing functions in a television receiver. It includes a phase detector, an oscillator and a predriver. The μA1394 is electrically similar to the μA1391, except that it accepts a negative flyback input.

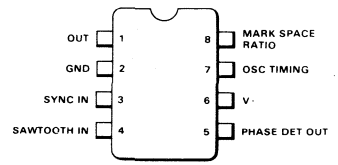
The device is constructed on a single silicon chip using the Fairchild Planar* epitaxial process.

- **INTERNAL SHUNT REGULATOR**
- **PRESET HOLD CONTROL CAPABILITY**
- **±300 Hz TYPICAL PULL-IN**
- **LINEAR BALANCED PHASE DETECTOR**
- **VARIABLE OUTPUT DUTY CYCLE FOR DRIVING A TUBE OR TRANSISTOR OUTPUT STAGE**
- ***LOW THERMAL FREQUENCY DRIFT***
- **SMALL STATIC PHASE ERROR**
- **ADJUSTABLE DC LOOP GAIN**

ABSOLUTE MAXIMUM RATINGS: T_A = 25°C unless otherwise noted.

Supply Current	40 mA
Output Voltage	40 V
Output Current	30 mA
Sync Input Voltage (Pin 3)	5.0 V_{p-p}
Flyback Input Voltage (Pin 4)	5.0 V_{p-p}
Power Dissipation (Package Limitation)	
Plastic Package	625 mW
Derate above T_A = 25°C	5.0 mW/°C
Operating Temperature Range (Ambient)	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

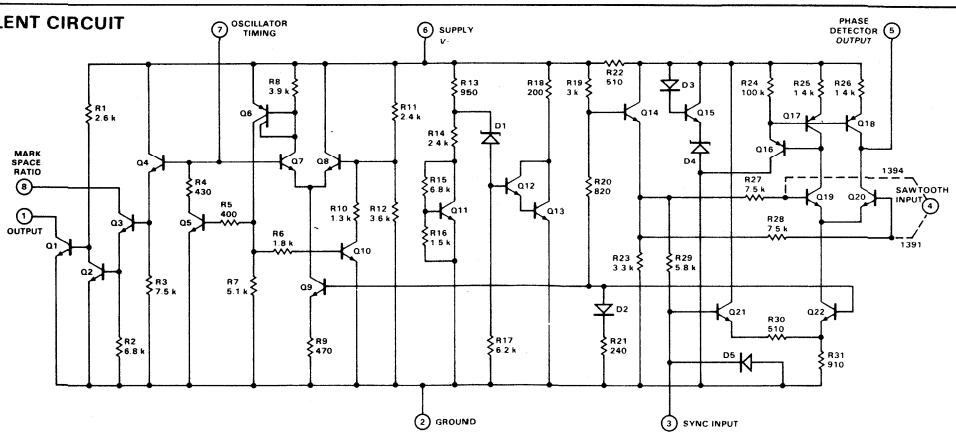
CONNECTION DIAGRAM
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
μA1391	μA1391TC
μA1394	μA1394TC

EQUIVALENT CIRCUIT



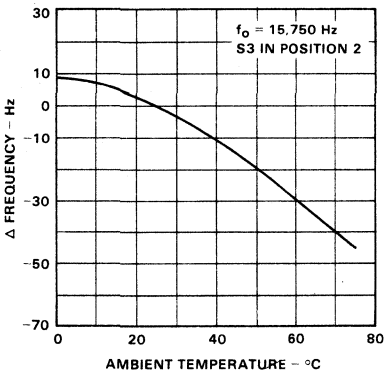
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: T_A = 25°C, unless otherwise noted (See Test Circuit, all switches in Position 1)

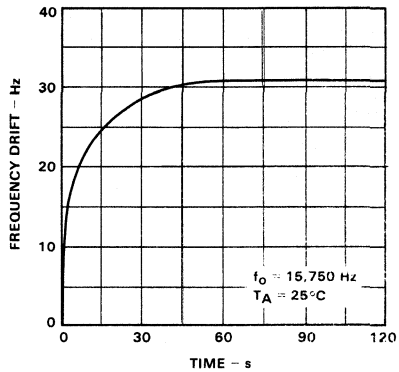
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Regulated Voltage (Pin 6)		8.0	8.6	9.0	V
Supply Current (Pin 6)			20		mA
Collector-Emitter Saturation Voltage (Output Transistor Q1 in Equivalent Circuit)	I_C = 20 mA, Pin 1		0.15	0.25	V
Voltage (Pin 4)			2.0		V
Oscillator Pull-in Range Adjust R_H in Figure 2			±300		Hz
Oscillator Hold-in Range Adjust R_H in Figure 2			±900		μs
Static Phase Error	Δf = 300 Hz		0.5		μs
Free-running Frequency Supply Dependance (S1 in Position 2)			±3.0		Hz/V
Phase Detector Leakage (Pin 5) (All switches in Position 2)				+1.0	μA
Sync Input Voltage (Pin 3)		2.0		5.0	V_{p-p}
Sawtooth Input Voltage (Pin 4)		1.0		3.0	V_{p-p}

TYPICAL ELECTRICAL CHARACTERISTICS

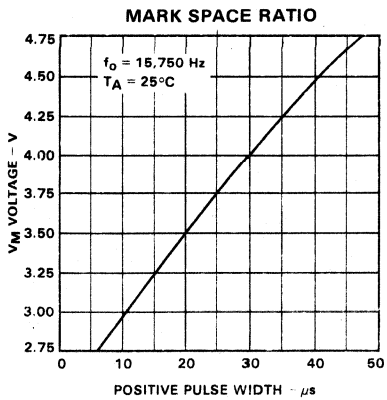
FREQUENCY AS A FUNCTION OF AMBIENT TEMPERATURE

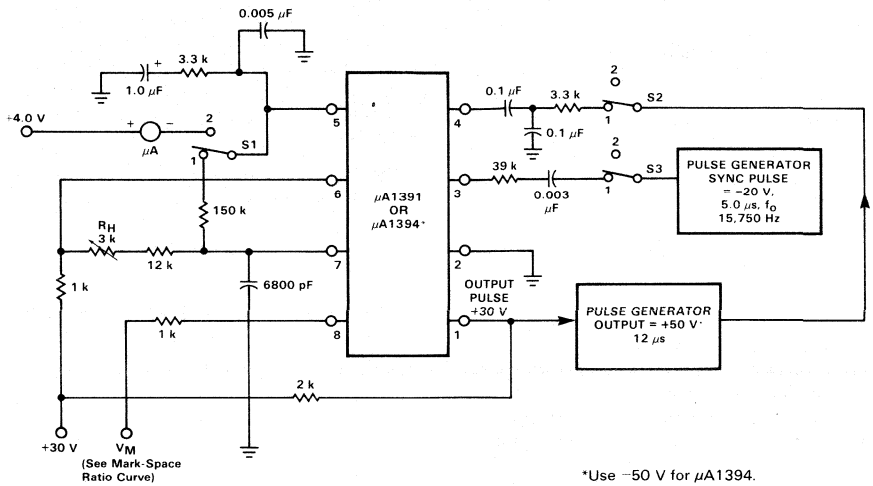


FREQUENCY DRIFT AS A FUNCTION OF WARM-UP TIME



MARK SPACE RATIO





TEST CIRCUIT

μA1391/μA1394 APPLICATIONS INFORMATION

The μA1391 and μA1394 integrated circuits are identical except for the polarity of the sawtooth input signal accepted at Pin 4. The μA1391 requires a positive ramp sawtooth signal during the horizontal retrace period; the μA1394 requires a negative ramp.

The following discussion makes no distinction between the μA1391 and the μA1394. Reference should be made to the "Typical Application Circuit."

This circuit contains a temperature-compensated shunt regulator which operates over a wide current range to accommodate normal fluctuations from an unregulated power supply. A minimum current of 18 mA into Pin 6 is recommended for good regulation. Allowing for 2 mA of shunt current external to the device, a minimum of 20 mA should be supplied through dropping resistors R_A and R_B:

$$R_A + R_B = \frac{\text{Unregulated Supply (Min)} - 9.0\ \text{V}}{20\ \text{mA}}$$

Resistors R_A and R_B may be combined and capacitor C_A eliminated when operating from a supply having less than 3% ripple.

The duty cycle of the output is controlled by the voltage (V_M) applied to Pin 8. The OFF time (output HIGH) is variable from 6 μs to 48 μs by changing V_M from 2.75 V to 4.75 V. (See Mark-Space Ratio Typical Performance Curve.) The source impedance to Pin 8 (parallel resistance of R_D and R_E) should be 1 kΩ for stable operation.

The oscillator free-running fequency is primarily determined by the RC network connected to Pin 7 and is given by the approximate expression:

$$f_o \simeq \frac{1}{0.6\ R_C\ C_B}$$

The desired free-running oscillator fequency is 15,734 Hz in conventional receivers or 31,468 Hz for systems which derive vertical sync by counting down from twice horizontal frequency. Either frequency may be obtained by a wide combination of values for R_C and C_B.

Oscillator sensitivity, however, is a direct function of R_C which therefore provides an independent means for adjusting the dc loop gain and thus the static phase accuracy. The expression for dc loop gain is

$$f_c = \mu\beta$$

where f_c is loop gain with units of Hz/radian, μ is phase detector sensitivity which, for the μA1391/94, has units of A/radian and β is oscillator sensitivity with units, correspondingly, of Hz/A.

The phase detector sensitivity of the μA1391/94 is:

$$\mu = \frac{I_{5(\text{positive})} - I_{5(\text{negative})}}{6.28\ \text{radians}}$$

Typically, $I_{5(\text{positive})} - I_{5(\text{negative})} = 0.5$ mA,

$$\therefore\ \mu_{\text{typical}} = 0.16\ \text{mA/radian}$$

Neglecting the effects of R_Y and R_4, oscillator sensitivity of the device is given by:

$$\beta = \frac{f_o R_C}{0.6\ V_6}$$

Typically, $V_6 = 8.5$ V and $f_o = 15{,}734$ Hz,

$$\beta_{\text{typical}} = R_C \times 3.1\ \text{Hz/mA}$$

Combining the above expressions for μ and β:

$$f_{c\ \text{typical}} = 0.5\ R_C\ \text{Hz/radian}$$

where R_C is in ohms.

The static phase error is inversely proportional to dc loop gain and is given by:

$$\theta = \frac{\Delta f}{f_c} \text{ radians}$$

where θ is static phase error in radians and Δf is oscillator tuning error in Hz.

For convenience, static phase error may also be expressed in μs. At f_o = 15,734 Hz:

$$t_s = 10.1 \frac{\Delta f}{f_c} \mu s$$

Static phase error, for a given oscillator tuning error, can therefore be chosen by the selection of R_C. Static phase error should only be made small enough to ensure clean burst gating (about ±0.5 μs for color receivers), since unnecessarily high dc loop gain would have the undesirable effect of making the loop overly sensitive to thermal noise induced horizontal jitter.

Static phasing can be adjusted by adding a small resistor in a series or a large resistor in parallel with the flyback pulse integrating capacitor.

The design of the dynamic characteristics of the loop is less straightforward and involves certain compromises. A loop filter designed for high immunity to impulse noise disturbances will tend to have a response which is too slow for tracking phase changes caused by airplane flutter. Pull-in time and pull-in range will also be adversely affected. A fast responding loop, however, may suffer from excessive ringing following an impulse noise disturbance.

The dynamic characteristics of the loop can be directly affected by the selection of values for R_X, R_Y and C_C once R_C is selected for satisfactory static phase error performance. The values of R_X, R_Y and C_C shown in the Typical Application Circuit represent a reasonable compromise although factors ranging from horizontal APC interaction with the AGC system to designer preferences could modify these values. It should be noted that an increase in the value of R_Y will reduce the hold-in range.

The following simplified equations may be found helpful for optimizing the loop characteristics:

$$f_{\eta\eta} \text{ (noise bandwidth)} = \frac{1 + X^2\, \omega_c}{4 \times 1}$$

$$\omega_\eta \text{ (natural undamped loop resonant feequency)} = \frac{\omega_c}{(1 + X)\, T}$$

and

$$K \text{ (Damping coefficient)} = \frac{X^2 T\, \omega_c}{4}$$

where

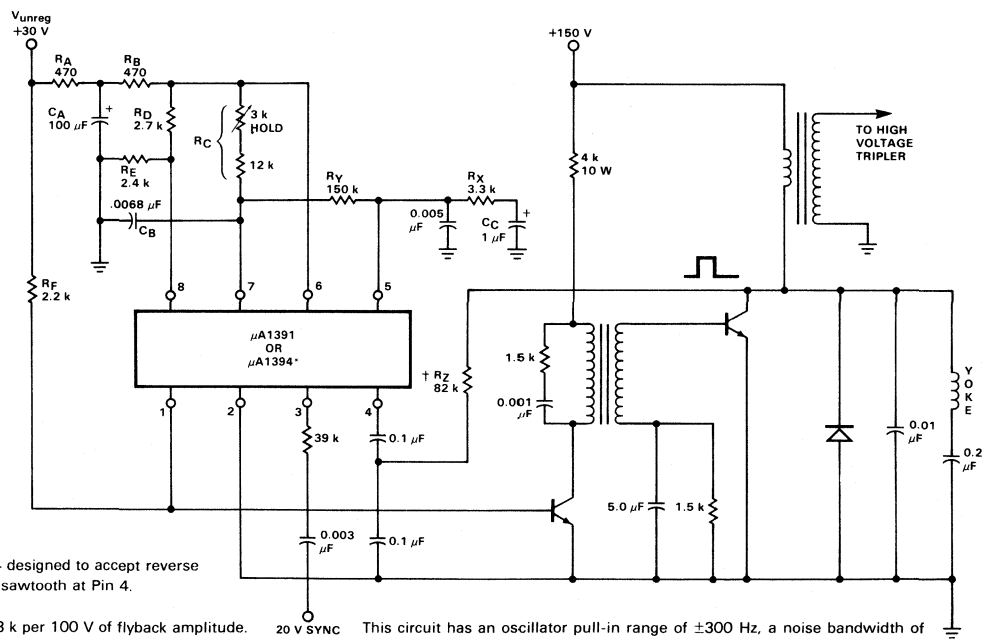
$$X = \frac{R_Y}{R_X}$$

$$\omega_c = 2\, \pi\, f_c,$$

and

$$T = R_Y\, C_C$$

Although the μA1391/94 operates at a relatively low frequency, care should nevertheless be exercised in the layout of associated components to prevent ringing and undesired coupling of signals.



*μA1394 designed to accept reverse polarity sawtooth at Pin 4.

†R_Z = 6.8 k per 100 V of flyback amplitude.

This circuit has an oscillator pull-in range of ±300 Hz, a noise bandwidth of 320 Hz, and a damping factor of 0.8.

Fig. 1 TYPICAL APPLICATION CIRCUIT

μA2136

FM IF AMPLIFIER/LIMITER/DETECTOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

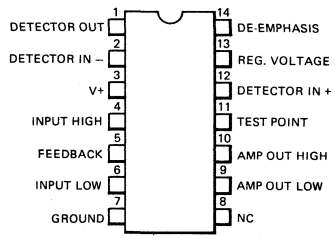
GENERAL DESCRIPTION – The 2136 is a monolithic three-stage limiting amplifier and FM detector circuit constructed using the patented Fairchild Planar* epitaxial process. The chip also contains a regulator which reduces parameter variations with temperature and applied supply voltage. The stabilized dc outputs of the regulator and the detector make the device especially suited for AFC applications using varactor diodes. The device is designed as a pin-to-pin substitute for the ULN2136. With minor changes in external components, it also serves as a replacement for the ULN2111 and similar products. In these applications the regulated output terminal (pin 13) is used as the supply terminal.

- **EXCELLENT AM REJECTION – 40 dB TYPICAL AT 10.7 MHz**
- **QUADRATURE DETECTOR EMPLOYING SINGLE TUNED CIRCUIT**
- **ACTIVE CIRCUITRY PERFORMANCE INSENSITIVE TO SUPPLY VARIATIONS**
- **TEMPERATURE STABILIZED VOLTAGE REGULATOR IS SHORT CIRCUIT PROTECTED**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage:	
(Used as μA2136) Supply on Pin 3	+20 V
(Used as μA2111) Supply on Pin 13	+15 V
Input Voltage (Pin 4)	+3.5 V
Power Dissipation (Note 1)	670 mW
Regulator Output Current (Pin 13)	30 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature	
Hermetic DIP (Soldering, 60 seconds)	300°C
Molded DIP (Soldering, 10 seconds)	260°C

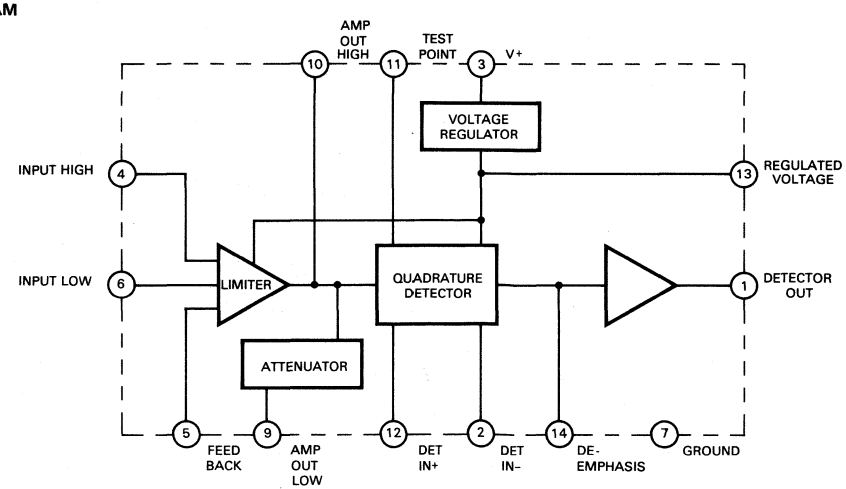
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9A
PACKAGE CODES P



ORDER INFORMATION

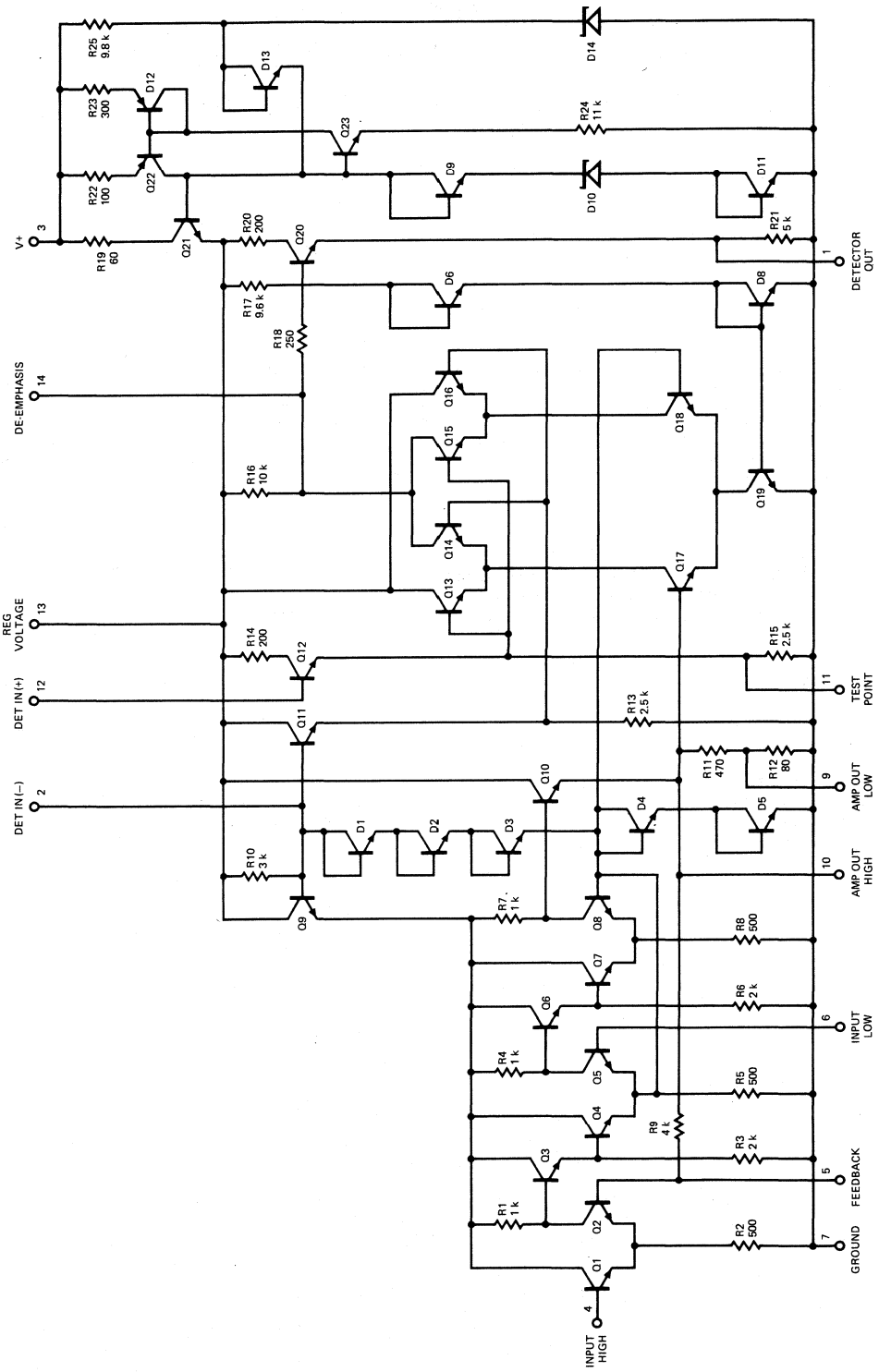
TYPE	PART NO.
μA2136	μA2136PC

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS: T_A = 25°C, Supply Voltage −12 V, See Test Circuit, Note 2, unless otherwise specified

DC CHARACTERISTICS (V_{IN} = 0 V)

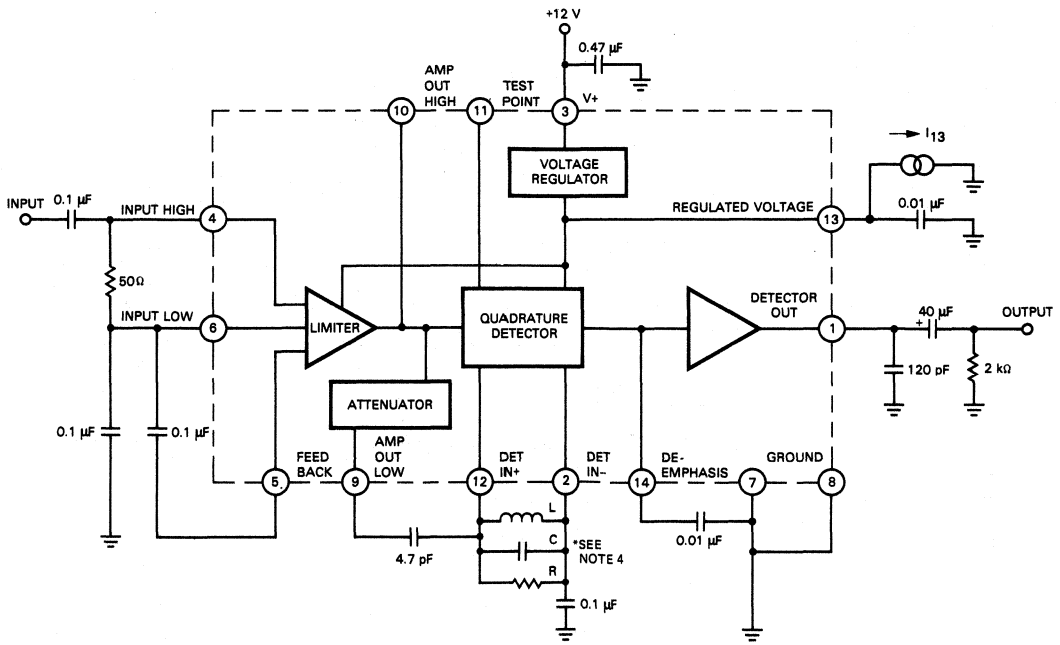
CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_3	Pin 13 open	12	17	22	mA
Detector Output Level	V_1		3.0	3.8	4.6	V
Temperature Sensitivity of V_1		I_{13} = 20 mA		+1.5		mV/°C
Temperature Sensitivity of V_{13}		I_{13} = 20 mA		+1.5		mV/°C
De-Emphasis Resistance	R_{14}		7.0	10	13	kΩ
Amplifier Input Resistance	R_{IN4}			5.0		kΩ
Amplifier Input Capacitance	C_{IN4}			11		pF
Detector Input Resistance	R_{IN12}			70		kΩ
Detector Input Capacitance	C_{IN12}			2.7		pF
Amplifier HIGH Output Resistance	R_{OUT10}			60		Ω
Detector Output Resistance	R_{OUT1}			200		Ω

AC CHARACTERISTICS (f_o = 10.7 MHz, Deviation = ±75 kHz, Modulation Frequency = 400 Hz)

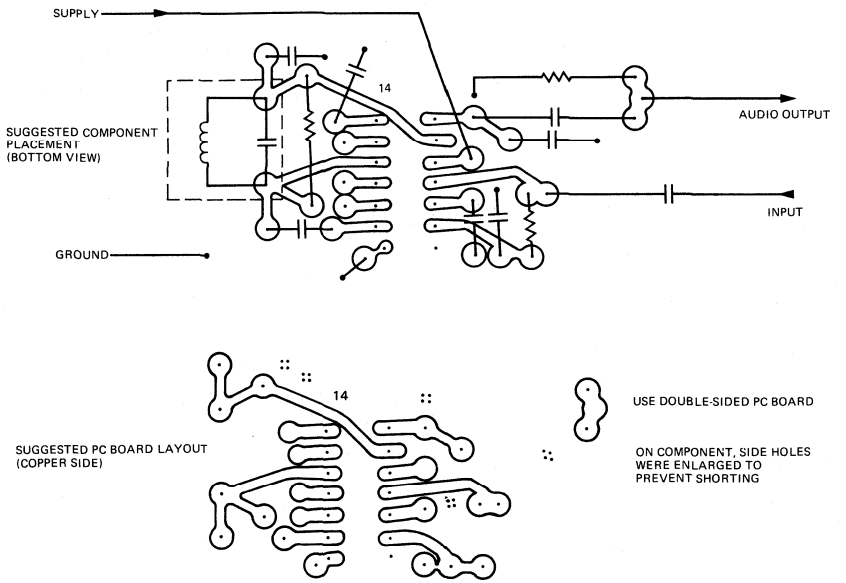
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Amplifier Voltage Gain	$V_G = V_{10}/V_4$	V_{IN} < 0.3 mV_{RMS}		56		dB
Input Limiting Threshold	V_{TH}	Recovered Audio = V_{OUT}−3.0 dB		450	800	μV_{RMS}
Recovered Audio Output	V_{OUT}	V_{IN} = 10 mV_{RMS}		400		mV_{RMS}
Output Distortion	THD	V_{IN} = 10 mV_{RMS}		1.0	3.0	%
AM Rejection	AMR	(Note 3)		40		dB
Line Regulation	$\Delta V_{13}/\Delta V_8$	I_{13} = 20 mA		5.0	25	mV/V

NOTES:
1. Rating applies up to 70°C operating temperature. Derate 8.3 mW/°C between 70°C and 85°C.
2. The tank circuit parameters apply to the finished test jig. They are measured between pins 12 and 2 without IC inserted.
3. $AMR = 20 \log \frac{V_{OUT} \text{ at 10 mV FM, 100\% modulated with } f_m = 400 \text{ Hz}}{V_{OUT} \text{ at 10 mV AM, 10.7 MHz, 30\% modulated with } f_m = 400 \text{ Hz}}$
4. Tank circuit values: L = 1.5 – 3 μH, C = 120 pF, R = 3.9 kΩ, Q_L = 20 ± 5%.

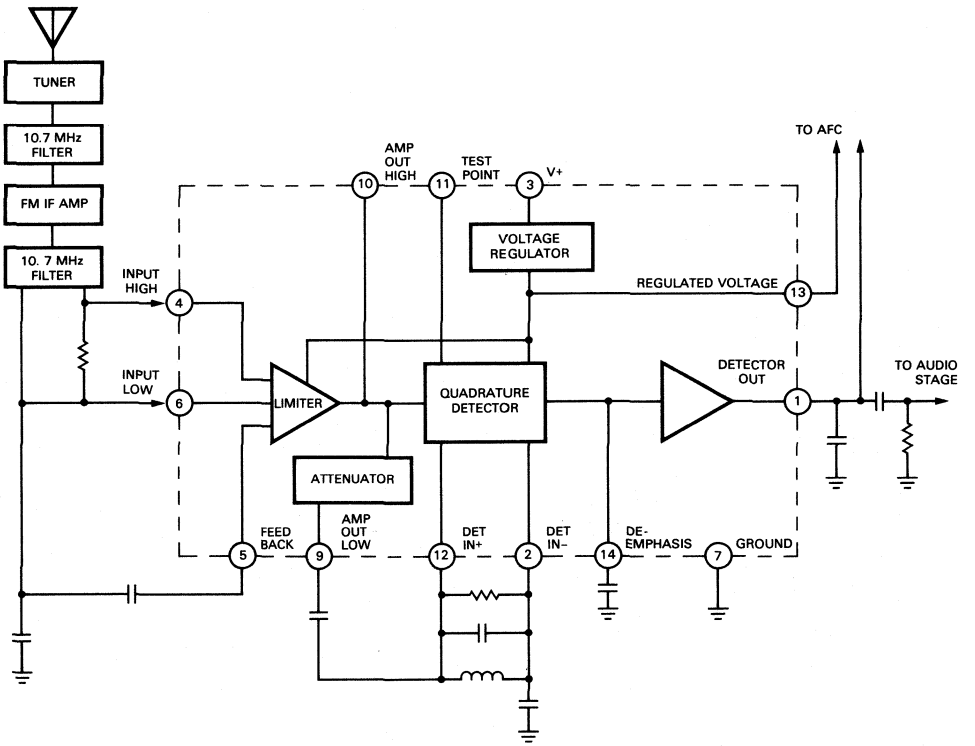
TEST CIRCUIT



PC BOARD LAYOUT



TYPICAL APPLICATIONS



μA3064

TV AUTOMATIC FINE-TUNING CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3064 is a monolithic TV Automatic Fine-Tuning Circuit constructed using the Fairchild Planar* epitaxial process. The 3064 combines all of the automatic fine-tuning circuitry, except transformers, in one integrated circuit. Systems with low level IF amplifiers can now achieve tuning accuracies of ±25 kHz due to the 3064's high sensitivity. Internal voltage regulation improves overall performance and reduces system cost.

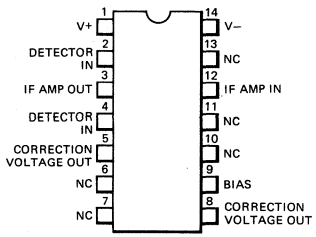
- **HIGH SENSITIVITY**
- **25 kHz MAX. FREQUENCY DEVIATION**
- **INTERNAL VOLTAGE REGULATOR**
- **INTERNAL AGC**

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	(Note 2)
Internal Power Dissipation (Note 3)	700 mW
Detector Differential Voltage (V_{2-4})	±10V
Detector Input Voltage Range (V_2, V_4)	+5V, -6V
I.F. Amp Output (V_3)	+20V, 0V
Bias Voltage (Vg)	+2V, 0V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Pin Temperature (Soldering, 10 s)	260°C

NOTES:
(1) All voltages referenced to V_ except as noted.
(2) V_+ terminal may be connected to any positive voltage source through a suitable dropping resistor, provided the dissipation rating is not exceeded.
(3) Derate linearly at 5.6 mW/°C for ambient temperatures above +25°C.

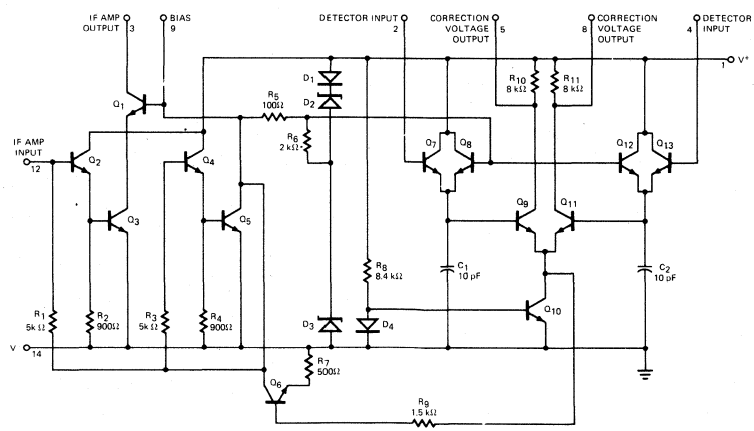
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9A
PACKAGE CODE P



ORDER INFORMATION

TYPE	PART NO.
μA3064	μA3064PC

EQUIVALENT CIRCUIT



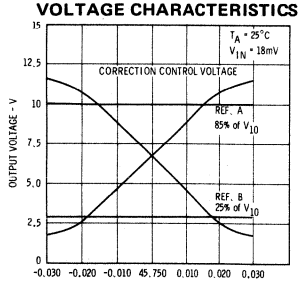
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $V_+ = +30V$, $R_S = 1.5\ k\Omega$, $T_A = 25°C$, Test Circuit 1, unless otherwise specified

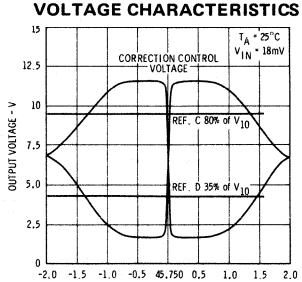
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Power Consumption	$T_A = +25°C$	130	140	150	mW
	$T_A = -25°C$		135	150	mW
	$T_A = +85°C$		145	150	mW
Supply Current – I+	$V_1 = +10.5V$ Test Ckt 2	4.0	6.5	9.5	mA
Regulated Supply Voltage – V_+	Test Ckt 2	10.9	11.8	12.8	V
Quiescent Operating Current – I_3		1.0	2.0	4.0	mA
Quiescent Operating Voltages – (V_5, V_8)		5.0	6.9	8.0	V
Output Offset Voltage – (V_5, V_8)		–1.0	0	1.0	V
Input Admittance – Y_{11}	f = 45.75 MHz		0.41 + j 1.0		mmho
Reverse Transfer Admittance – Y_{12}	f = 45.75 MHz		0 + j 3.4		μmho
Forward Transfer Admittance – Y_{21}	f = 45.75 MHz		24.5 – j 29		mmho
Output Admittance – Y_{22}	f = 45.75 MHz		0.04 + j 0.9		mmho
Correction Control Voltage - V_5 (Test Circuit 1)	V_{IN} = 18 mV RMS f_o = 45.750 MHz Δf as listed (MHz)				
	–0.030	85			% V_+
	+0.030			25	% V_+
	–0.900	80			% V_+
	+0.900			35	% V_+
	–1.500			80	% V_+
	+1.500	35			% V_+
Correction Control Voltage - V_8 (Test Circuit 1)	V_{IN} = 18 mV RMS f_o = 45.750 MHz Δf as listed (MHz)				
	–0.030			25	% V_+
	+0.030	85			% V_+
	–0.900			35	% V_+
	+0.900	80			% V_+
	–1.500	35			% V_+
	+1.500			80	% V_+

TYPICAL PERFORMANCE CURVES

NARROW-BAND DYNAMIC CONTROL VOLTAGE CHARACTERISTICS

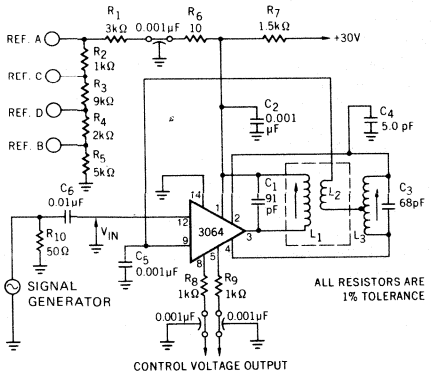


WIDE-BAND DYNAMIC CONTROL VOLTAGE CHARACTERISTICS



NOTE: See test circuit 1.

TEST CIRCUIT 1
CORRECTION VOLTAGES



L_1 is aligned for symmetrical bandwidth on either side of 45.750 MHz.

L_2 tertiary winding wound on L_1 coil form.

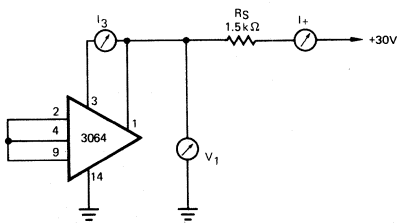
L_3 is aligned for zero differential output between terminals 5 and 8 at f_o = 45.750 MHz.

REFERENCE VOLTAGE PERCENTAGES

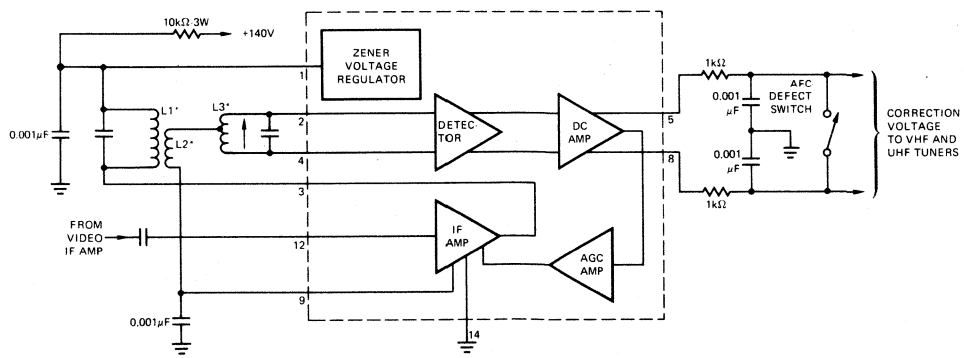
Ref. A	**85% of V_1**
Ref B	**25% of V_1**
Ref. C	**80% of V_1**
Ref. D	**35% of V_1**

NOTE: Parts placement is critical.

TEST CIRCUIT 2
Regulated Voltage, Total Supply Current and Quiescent Current at Terminal 3



BLOCK DIAGRAM



COIL DATA FOR DISCRIMINATOR WINDINGS

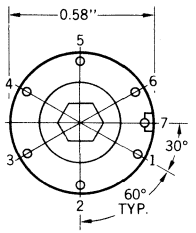
L_1 – Discriminator Primary: 3 1/16 turns; #20, Enamel-covered wire–close-wound, at bottom of coil form. Inductance of L_1 = 0.165 μH; Q_o = 120 at f_o = 45.75 MHz. Start winding at Terminal #6; finish at Terminal #1. See Notes below.

L_2 – Tertiary Windings: 2 1/16 turns; #20 Enamel-covered wire–close wound over botton end of L_1. Start winding at Terminal #3; finish at Terminal #4. See Notes below.

L_3 – Discriminator Secondary: 3 1/2 turns; center-tapped, space wound at bottom of coil form. Inductance of L_3 = 0.180 μH; Q_o = 150 at f_o = 45.75 MHz. Start winding at Terminal #2; finish at Terminal #5, connect center tap to Terminal #7. See Notes below.

NOTES:
1. Coil Forms; Cylindrical; 0.30" Dia. max.
2. Tuning Core: 0.250" Dia. x 0.37" Length.
   : Material: Carbinal J or equivalent.
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.

COIL FORM BASE TERMINAL DIAGRAM



Coil	RCA Distributor Part No.
(L_1, L_2)	122 213
L_3	122 203

μA3065

TV SOUND SYSTEM

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3065 is a monolithic TV Sound System constructed using the Fairchild Planar* epitaxial process. It contains a multi-stage limiting IF amplifier, dc gain (volume) control, FM detector and an audio driver. Excellent sensitivity, high AM rejection and an internally regulated supply, coupled with low external component requirements make the 3065 ideally suited for TV sound channels.

- **DC VOLUME CONTROL ELIMINATES NEED FOR SHIELDED CABLES**
- **EXCELLENT AM REJECTION – 50 dB TYPICAL AT 4.5 MHz**
- **DIFFERENTIAL PEAK DETECTOR REQUIRES ONLY ONE SINGLE-TUNED COIL**
- **INTERNAL ZENER DIODE REGULATED SUPPLY**
- **LOW HARMONIC DISTORTION**

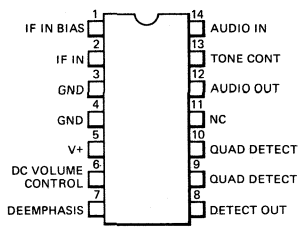
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	Note 1
Internal Power Dissipation (Note 2)	670 mW
Power Supply Current	50 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature	
Molded DIP (Soldering, 10 s) μA3065PC	260°C

NOTES
1. V_+ terminal may be connected to any positive voltage through a suitable dropping resistor, provided the dissipation rating is not exceeded.
2. Rating applies to ambient temperature up to 70°C. Derate linearly at 8.3 mW/°C above 70°C.

CONNECTION DIAGRAM

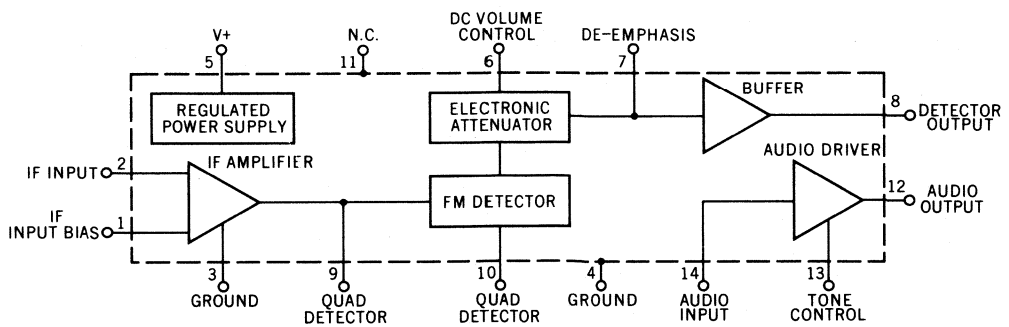
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9A
PACKAGE CODE P



ORDER INFORMATION

TYPE	PART NO.
μA3065	μA3065PC

BLOCK DIAGRAM



*Planar is a patented Fairchild process

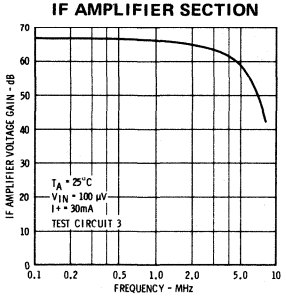
ELECTRICAL CHARACTERISTICS: T_A = 25°C, I+ = 30 mA unless otherwise specified

CHARACTERISTICS	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Zener Regulating Voltage (V_5)			10.3	11.2	12.2	V
Supply Current (I_5)	V_+ = 9.0V		10	16	24	mA
Internal Power Dissipation	I_+ = 33 mA		343	370	400	mW
Voltage at IF Input Bias (V_1)				2.0		V
Voltage at DC Volume Control (V_6)				4.8		V
Voltage at De-emphasis (V_7)				6.1		V
Voltage at Quad Detector (V_9)				3.7		V
Voltage at Audio Output (V_{12})			4.0	5.1	5.8	V
AC CHARACTERISTICS						
IF AMPLIFIER						
Input Limiting Voltage at −3 dB point	f = 4.5 MHz			200	400	μV
AM Rejection	f_o = 4.5 MHz, FM ± 25 kHz at 400 Hz, V_{IN} = 100 mV AM = 30% at 1 kHz		40	50		dB
IF Transconductance	f = 4.5 MHz					
Magnitude				500		mmho
Phase Angle				45		degrees
Feedback Capacitance	f = 1.0 MHz, Pin 2 to Pin 9			<0.02		pF
Input Impedance Components	f = 4.5 MHz, Pin 1 to Pin 2					
Parallel Input Resistance				17		kΩ
Parallel Input Capacitance				4.0		pF
Output Impedance Components	f = 4.5 MHz, Pin 9 to Ground					
Parallel Output Resistance				3.25		kΩ
Parallel Output Capacitance				75		pF
DETECTOR	(f_o = 4.5 MHz, FM = ±25 kHz at 400 Hz, V_{IN} = 100 mV)					
Recovered AF Voltage			0.5	0.75		Vrms
Total Harmonic Distortion				0.9	2.0	%
Output Resistance						
De emphasis Output				7.5		kΩ
Detector Output				300		Ω
ATTENUATOR						
Max. Attenuation	R_x = ∞		60	80		dB
Max. Play-through Voltage*	R_x = ∞			0.075	1.0	mV
AUDIO AMPLIFIER						
Voltage Gain	V_{14} = 0.1 Vrms, f = 400 Hz	2	17.5	20		dB
Total Harmonic Distortion	V_{12} = 2 Vrms, f = 400 Hz	2		1.5		%
Undistorted Output Voltage	THD = 5%, f = 400 Hz	2	2.0	2.5		Vrms
Input Resistance	f = 400 Hz			70		kΩ
Output Resistance	f = 400 Hz			270		Ω

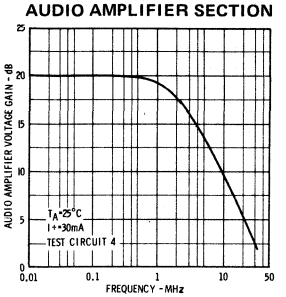
* Play-through voltage is the unwanted signal, measured at the detected output (Pin 8), when the volume control is set for minimum output.

TYPICAL PERFORMANCE CURVES FOR μA3065

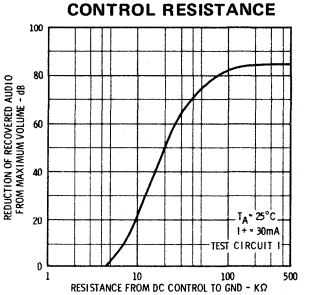
FREQUENCY RESPONSE OF IF AMPLIFIER SECTION



FREQUENCY RESPONSE OF AUDIO AMPLIFIER SECTION

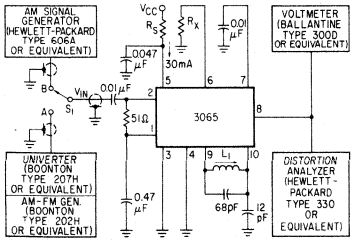


AUDIO GAIN REDUCTION VERSUS DC VOLUME CONTROL RESISTANCE



TEST CIRCUITS

INPUT LIMITING VOLTAGE, AM REJECTION, RECOVERED AUDIO, TOTAL HARMONIC DISTORTION, MAXIMUM ATTENUATION, MAXIMUM "PLAY-THROUGH" TEST CIRCUIT.



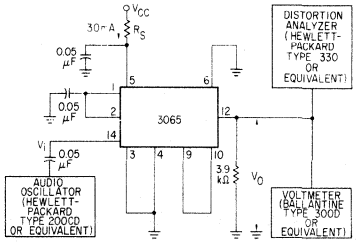
PINS 11, 12, 13, 14 NO CONNECTION

*L_1 = 16μH NOMINAL

$Q_{(UNLOADED)}$ = 50

TEST CIRCUIT 1

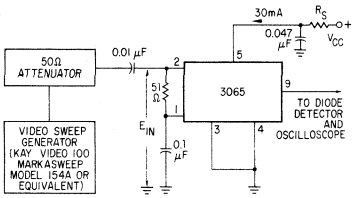
AUDIO VOLTAGE GAIN (UNDISTORTED OUTPUT)



PINS 7, 8, 11, 13 NO CONNECTION

TEST CIRCUIT 2

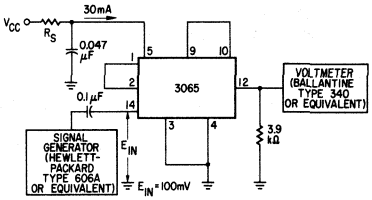
IF AMPLIFIER SECTION



E_{IN} = 100μVrms

TEST CIRCUIT 3

AUDIO AMPLIFIER SECTION

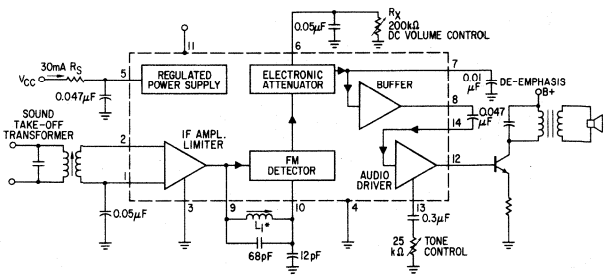


E_{IN} = 100 mV

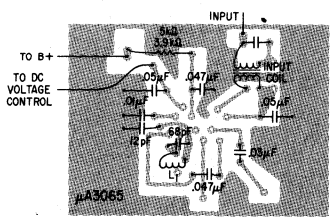
TEST CIRCUIT 4

TYPICAL APPLICATION

TV SOUND SYSTEM



SUGGESTED CIRCUIT LAYOUT COMPONENT SIDE



*L_1 = 16μH NOMINAL, $Q_{(UNLOADED)}$ = 50

μA3075

FM IF AMPLIFIER/LIMITER/DETECTOR/AUDIO PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3075 is a monolithic FM IF sub-system constructed using the Fairchild Planar* epitaxial process. The system consists of a three stage limiting amplifier with a zener diode regulated power supply, a differential peak detector stage and an internally biased audio preamplifier stage.

The IF amplifier stage provides typically 60 dB gain at 10.7 MHz and is followed by a differential limiting stage with constant current source to provide excellent limiting characteristics. The differential peak detector circuit requires only one coil and thus provides easy tuning and minimum external components.

Applications include automotive and home FM receivers, mobile communications equipment, and television sound channels.

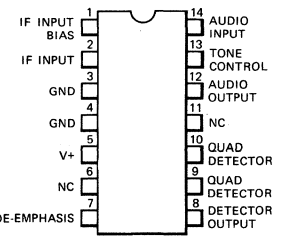
- **250μV TYPICAL LIMITING SENSITIVITY AT 10.7MHz**
- **125μV TYPICAL LIMITING SENSITIVITY AT 4.5MHz**
- **55dB TYPICAL AM REJECTION AT 4.5MHz**
- **SINGLE COIL TUNING**
- **DIFFERENTIAL PEAK DETECTION**
- **INTERNAL ZENER DIODE REGULATION FOR IF SECTION**

ABSOLUTE MAXIMUM RATINGS (Voltage at any terminal must not exceed V+)

Supply Voltage (Pin 5)	+18V
Input Voltage (between pins 1 and 2)	±3V
Power Dissipation (Note 1)	670mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature	
Hermetic DIP (Soldering 60 s) μA3075DC	300°C
Molded DIP (Soldering 10 s) μA3075PC	260°C

NOTE 1: Rating applies to T_A = 70°C. Above 70°C derate at 8.3mW/°C.

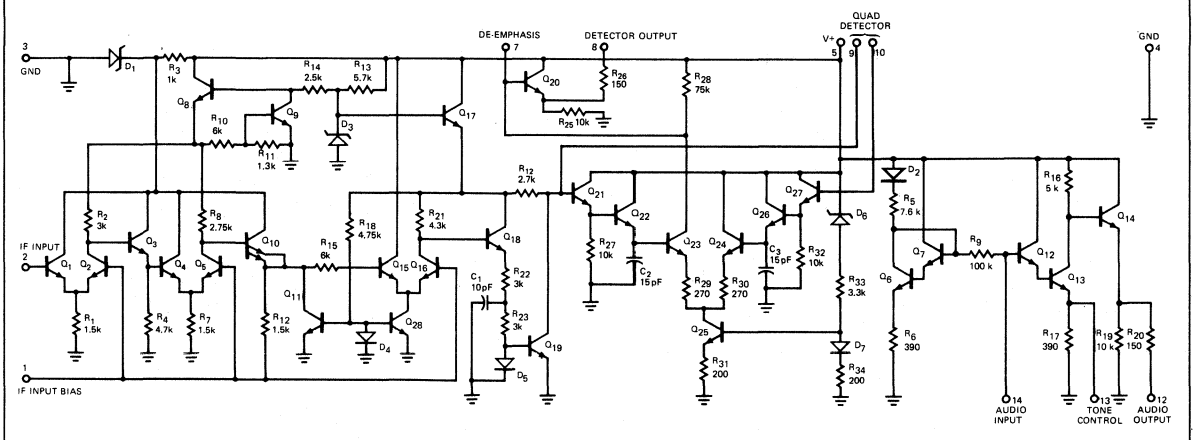
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9A
PACKAGE CODES P



ORDER INFORMATION

TYPE	PART NO.
μA3075	μA3075PC

EQUIVALENT CIRCUIT



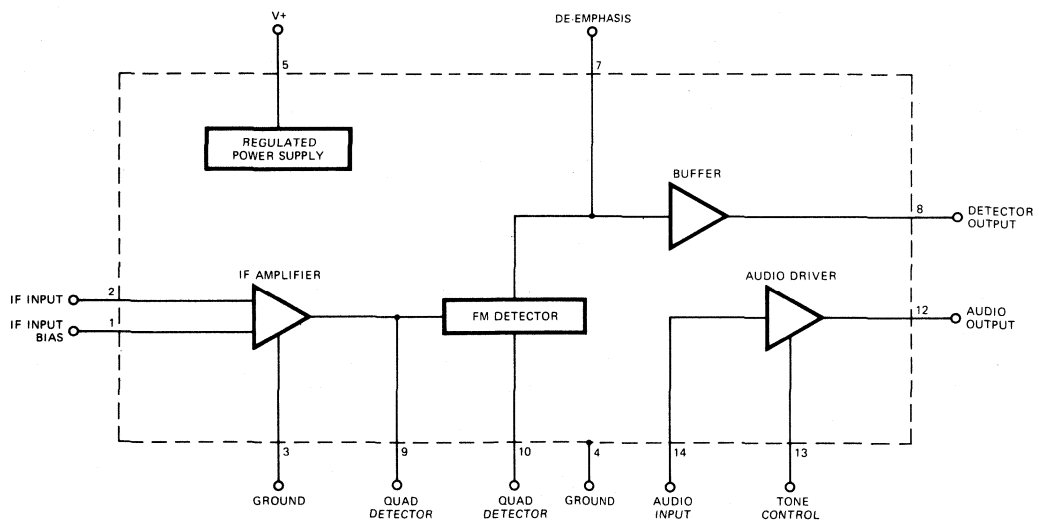
*Planar is a patented Fairchild process.

μA3075

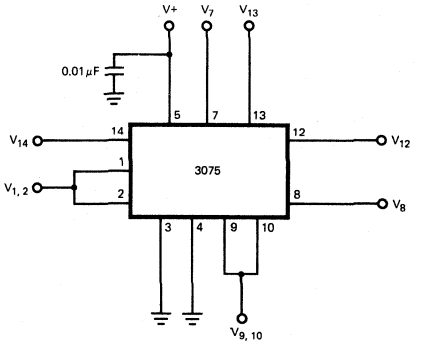
ELECTRICAL CHARACTERISTICS: T_A= 25°C, V+ = +12V, unless otherwise specified

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS (Test Circuit 1)						
Supply Current I_5		V+ = 8.5V	8.0	11		mA
		V+ = 12V	12	17	28	mA
		V+ = 16V		25	35	mA
Power Dissipation					340	mW
Terminal Voltages	Pin 7			6.0		V
	Pin 8			5.5		V
	Pin 12	R_L at Pin 12 = 3.9Ω		5.0		V
DC Shift Pin 8		Change V+ from 10V to 16V	−600		+600	mV
AC CHARACTERISTICS (IF Stage f = 10.7 MHz, Test Circuit 2)						
−3dB Limiting Sensitivity				250	600	μV
Recovered Audio at Detector Output			0.5	0.7		V_{RMS}
THD at Detector Output				1.0	2.0	%
AM Rejection			40	50		dB
AC CHARACTERISTICS (IF Stage f = 4.5 MHz, Test Circuit 2)						
−3dB Limiting Sensitivity				125	400	μV
Recovered Audio at Detector Output			1.0	1.4		V_{RMS}
THD at Detector Output				1.5	2.0	%
AM Rejection			40	56		dB
AC CHARACTERISTICS (Audio Amplifier f = 1 kHz, Test Circuit 3)						
Input Resistance			40			kΩ
Voltage Gain			10	12	17	V/V
THD at Detector Output		V_{OUT} = 2 V_{RMS}		2.0	4.0	%
Maximum Available Output Swing			8.4			Vp-p

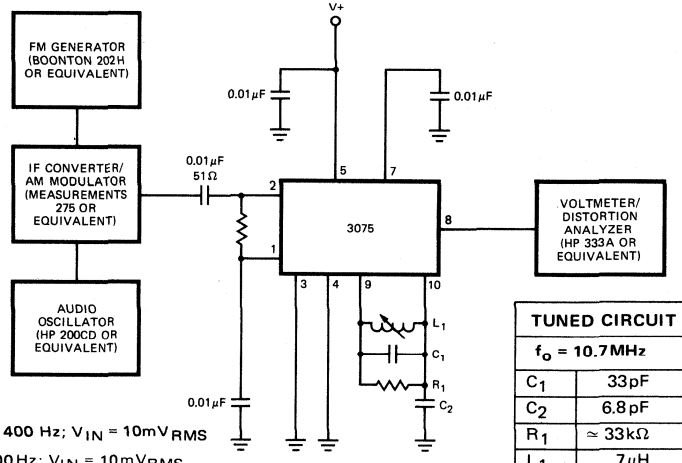
BLOCK DIAGRAM



TEST CIRCUITS



TEST CIRCUIT 1

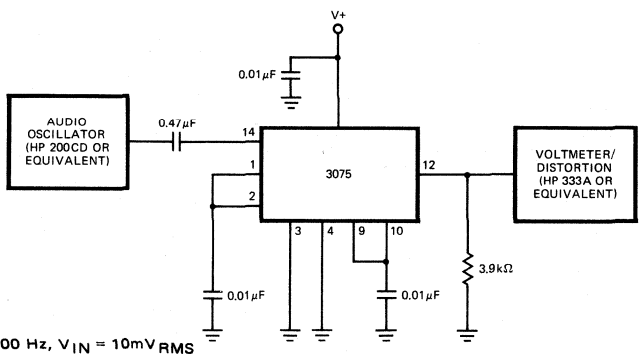


FM = 10.7 MHz ± 75 kHz @ 400 Hz; V_{IN} = 10mV$_{RMS}$

FM = 4.5MHz ± 25kHz @ 400Hz; V_{IN} = 10mV$_{RMS}$
NO CONNECTION TO PINS 6, 11, 12, 13, 14
AM modulation = 30% @ 400 Hz
Select R_1 for desired loaded Q (Q_L).

TEST CIRCUIT 2

TUNED CIRCUIT COMPONENTS		
	f_o = 10.7MHz	f_o = 4.5MHz
C_1	33pF	68pF
C_2	6.8pF	12pF
R_1	≃ 33kΩ	
L_1	7μH	16μH
Q_L	55	55



FM = 10.7 MHz ± 75 kHz @ 400 Hz, V_{IN} = 10mV$_{RMS}$
NO CONNECTION TO PINS 6, 7, 8, 11, 13

TEST CIRCUIT 3

μA3089

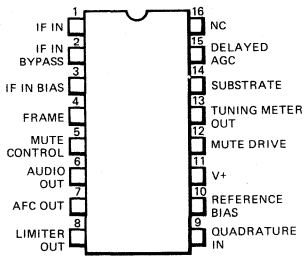
FM IF LIMITER DETECTOR AUDIO PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 3089 is a multifunction FM IF detector subsystem. It contains a three stage FM IF amplifier, a detector and an audio buffer amplifier. Auxiliary functions of the device include AGC and AFC for the tuner, a muting circuit and a tuning meter circuit. The circuit is fabricated using the Fairchild Planar† epitaxial process.

- **3-STAGE FM IF AMPLIFIER PROVIDING A 12 μV (TYP) LIMITING SENSITIVITY**
- **LEVEL DETECTORS ON EACH STAGE WITH A COMMON DRIVE FOR A TUNING METER OR A STEREO THRESHOLD LOGIC CIRCUIT**
- **DELAYED AGC OUTPUT FOR THE TUNER**
- **DOUBLY BALANCED QUADRATURE DETECTOR PROVIDING LOW DISTORTION – TYPICALLY 0.1 % WITH DOUBLE TUNED CIRCUIT**
- **FLEXIBLE AFC CIRCUIT**
- **AUDIO PREAMPLIFIER PROVIDING 400 mV (TYP) OF DRIVE**
- **AUDIO MUTE (SQUELCH) CONTROL CIRCUITS**
- **INTERNAL VOLTAGE REGULATOR**

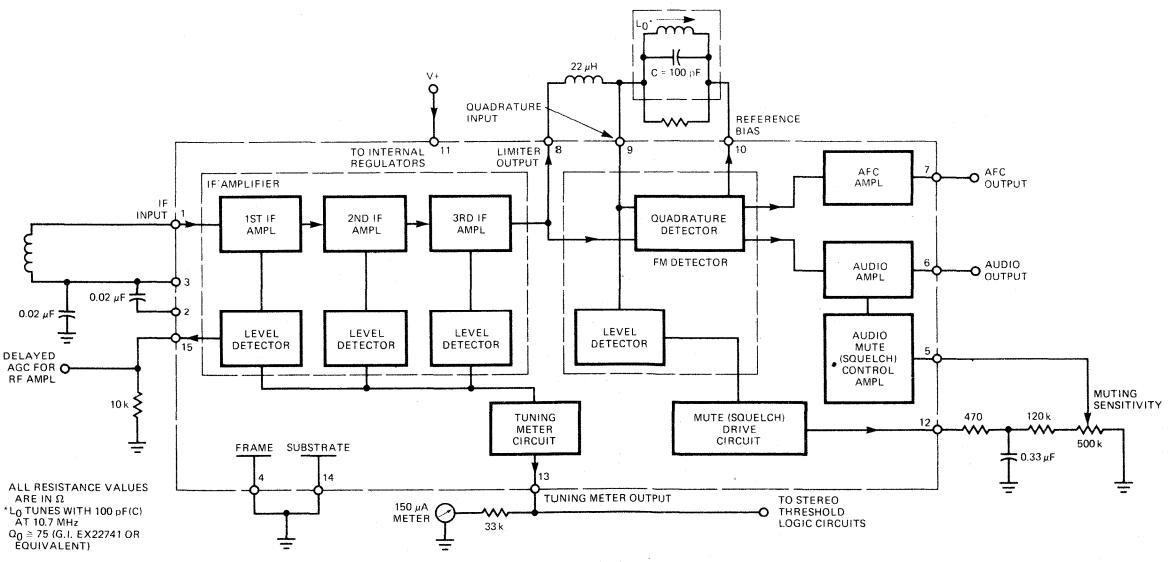
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6B 9B
PACKAGE CODE D P



ORDER INFORMATION

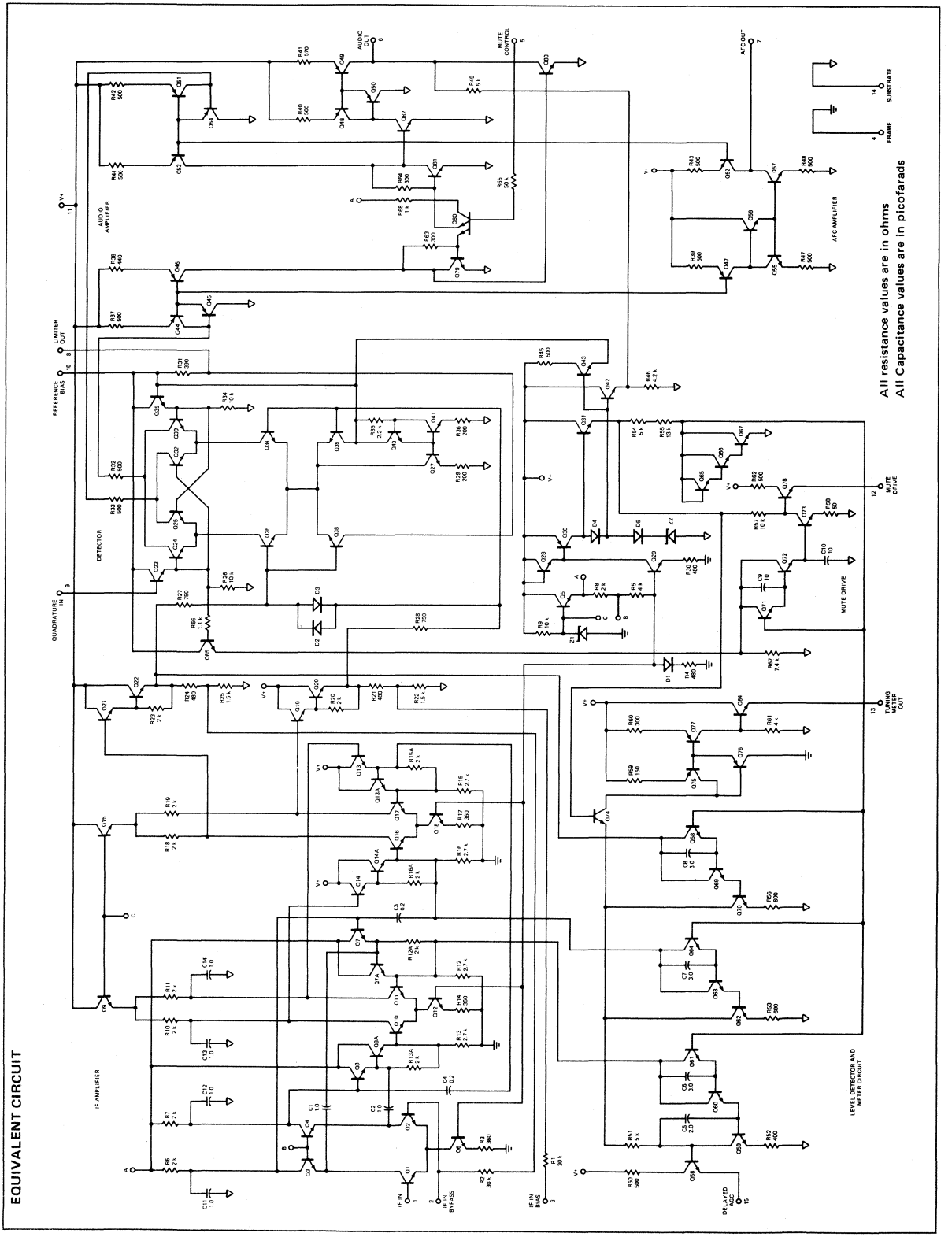
TYPE	PART NO.
μA3089	μA3089DM
μA3089C	μA3089DC
μA3089C	μA3089PC

BLOCK DIAGRAM



†Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Between Pins 11 and 4	+16V
Between Pins 11 and 14	+16V
DC Current Out of Terminal 15 for AGC	2.0 mA
DC Current Out of Terminals 12 and 13	5.0 mA
Power Dissipation	
$T_A \leq 85°C$	670 mW
$T_A > 85°C$	Derate at 10 mW/°C
Operating Temperature Range	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature (Soldering, 10 s)	260°C

μA3089

ELECTRICAL CHARACTERISTICS: V+ = 12 V, T_A = −55°C to 125°C (Note 2)

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS: V_{IN} = 0, Non-Muted, Test 1 or 2						
Quiescent Circuit Current	I_{11}				27	mA
DC Voltages at:						
IF Input	V_1		1.2		3.0	V
IF Input Bypass	V_2		1.2		3.0	V
IF Input Bias	V_3		1.2		3.0	V
Audio Output	V_6		5.0		6.5	V
Reference Bias	V_{10}		5.0		6.5	V
AC CHARACTERISTICS: f_o = 10.7 MHz, f_{MOD} = 400 Hz, Deviation = ± 75 kHz, V_{IN} = 0.1 V, Figure 1 or 2						
Input Limiting Voltage (−3 dB Point)					40	μV
AM Rejection (Pin 6)			35			dB
Recovered AF Voltage (Pin 6)			300		600	mV
*Total Harmonic Distortion (Pin 6)						
Single Tuned					5	%
Signal Plus Noise to Noise Ratio			60			dB

*THD Characteristics are mainly a function of the phase characteristics of the circuit connected between pins 8, 9 and 10.

NOTE 2: Full Temperature Range Performance Guaranteed by 25°C Testing.

μA3089C

ELECTRICAL CHARACTERISTICS: T_A = 25°C, V+ = 12 V

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS: V_{IN} = 0, Non-Muted, Test Circuit 1 or 2						
Quiescent Circuit Current	I_{11}			23	30	mA
DC Voltages at:						
IF Input	V_1		1.2	1.9	2.4	V
IF Input Bypass	V_2		1.2	1.9	2.4	V
IF Input Bias	V_3		1.2	1.9	2.4	V
Audio Output	V_6		5.0	5.6	6.0	V
Reference Bias	V_{10}		5.0	5.6	6.0	V
AC CHARACTERISTICS: f_o = 10.7 MHz, f_{MOD} = 400 Hz, Deviation = ± 75 kHz, V_{IN} = 0.1 V, Figure 1 or 2, unless otherwise stated						
Input Limiting Voltage (−3 dB Point)		V_{IN} = Parameter		12	25	μV
AM Rejection (Lead 6)		400 Hz, 30 % MOD	45	55		dB
Recovered AF Voltage (Lead 6)			300	400	500	mV
*Total Harmonic Distortion (Lead 6)						
Single Tuned		See Fig. 1		0.5	1.0	%
Double Tuned		See Fig. 2		0.1		%
Signal Plus Noise to Noise Ratio			60	67		dB

*THD Characteristics are mainly a function of the phase characteristics of the circuit connected between pins 8, 9 and 10.

μA3089
TEST CIRCUITS

TEST CIRCUIT USING A SINGLE TUNED DETECTOR COIL

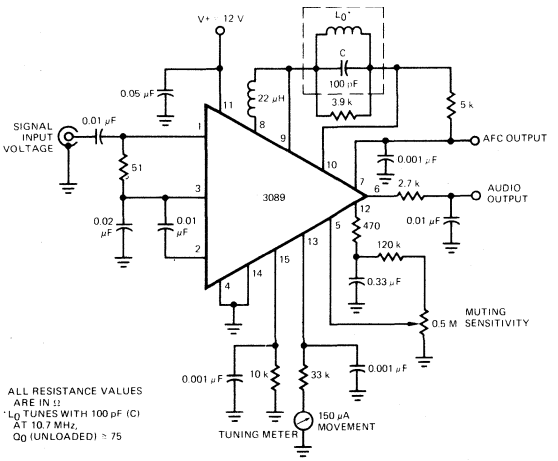


Fig. 1

TEST CIRCUIT USING A DOUBLE TUNED DETECTOR COIL

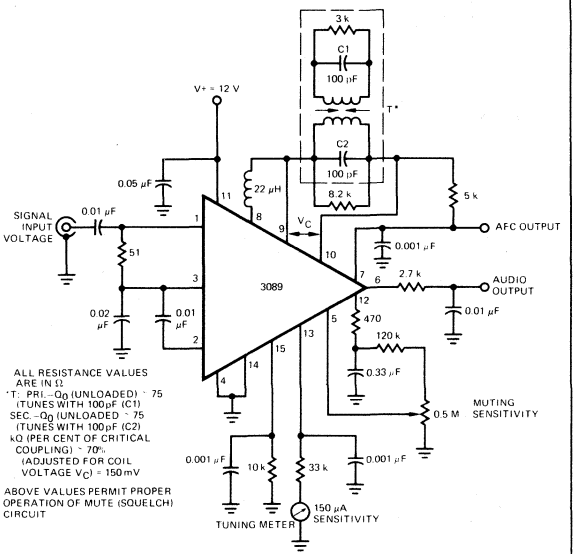
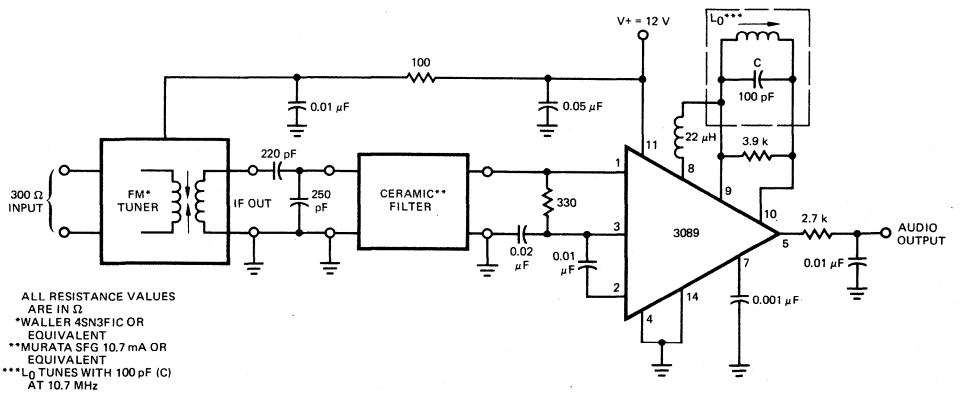


Fig. 2

TYPICAL FM SUBSYSTEM USING THE μA3089 WITH A SINGLE TUNED DETECTOR COIL



Performance data at f_o = 98 MHz, f_{MOD} = 400 Hz, Deviation = ± 75 kHz:

−3 dB Limiting Sensitivity	2 μV (Antenna Level)
20 dB Quieting Sensitivity	1 μV (Antenna Level)
30 dB Quieting Sensitivity	1.5 μV (Antenna Level)
Alternate channel rejection	60 dB

Fig. 3

TYPICAL PERFORMANCE CURVES FOR μA3089

MUTING ACTION, TUNER AGC, AND TUNING METER OUTPUT AS A FUNCTION OF INPUT SIGNAL VOLTAGE

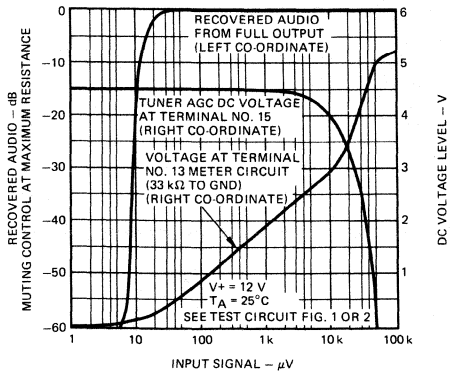


Fig. 4

AFC CHARACTERISTICS (CURRENT AT TERM. 7 AS A FUNCTION OF CHANGE IN FREQUENCY)

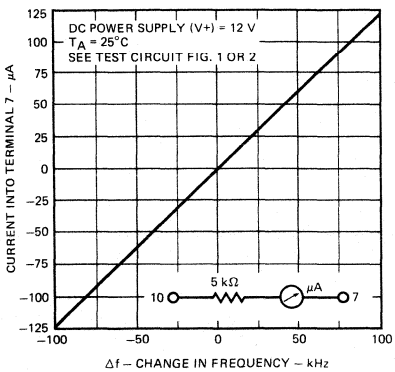


Fig. 5

μA4136

QUAD OPERATIONAL AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

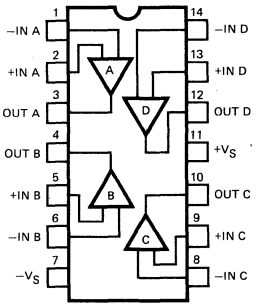
GENERAL DESCRIPTION – The μA4136 monolithic Quad Operational Amplifiers consists of four independent high gain, internally frequency compensated operational amplifiers. The specifically designed low noise input transistors allow the μA4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners. They are constructed using the Fairchild Planar* Epitaxial process. The simplified output stage completely eliminates crossover distortion under any load conditions, has large source and sink capacity, and is short-circuit protected. A novel current source stabilizes output parameters over a wide power supply voltage range.

- **UNITY GAIN BANDWIDTH 3 MHz**
- **CONTINUOUS SHORT CIRCUIT PROTECTION**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **NO LATCH-UP**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **μA741 OPERATIONAL AMPLIFIER TYPE PERFORMANCE**
- **PARAMETER TRACKING OVER TEMPERATURE RANGE**
- **GAIN AND PHASE MATCH BETWEEN AMPLIFIERS**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA4136	±22 V
μA4136C	±18 V
Differential Input Voltage (Note 1)	±30 V
Input Voltage (Note 1)	±15 V
Internal Power Dissipation (Note 2)	670 mW
Output Short Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
μA4136	−55°C to +125°C
μA4136C	0°C to +70°C
Storage Temperature Range	
Molded Package	−55°C to +125°C
Hermetic Package	−65°C to +150°C
Pin Temperature	
Molded Package (Soldering, 10 s)	260°C
Hermetic Package (Soldering, 60 s)	300°C

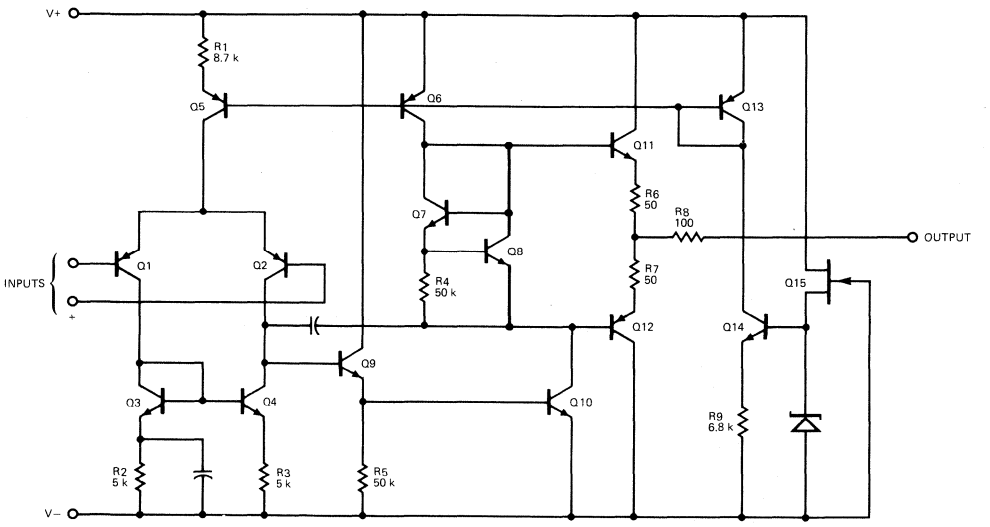
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
μA4136	μA4136DM
μA4136C	μA4136DC
μA4136C	μA4136PC

1/4 OF EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified

CHARACTERISTICS	CONDITIONS	μA4136			μA4136C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10$ kΩ		0.5	5.0		0.5	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	5.0		0.3	5.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	50,000	300,000		20,000	300,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Input Voltage Range		±12	±14		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Power Consumption			210	340		210	340	mW
Transient Response (Unity Gain) Risetime	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.13			0.13		μs
Transient Response (Unity Gain) Overshoot	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF		5.0			5.0		%
Unity Gain Bandwidth		2.0	3.0			3.0		MHz
Slew Rate (Unity Gain)	$R_L \geq 2$ kΩ		1.5			1.0		V/μs
Channel Separation (Open Loop)	f = 10 kHz, $R_S = 1$ kΩ		105			105		dB
(Gain = 100)	f = 10 kHz, $R_S = 1$ kΩ		105			105		dB
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for μA4136; $0°C \leq T_A \leq +70°C$ for μA4136C.								
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1500			800	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	25,000			15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ, $V_S = \pm 15$ V	±12			±10			V
Power Consumption	T_A = High		180	300		180	300	mW
	T_A = Low		240	400		240	400	

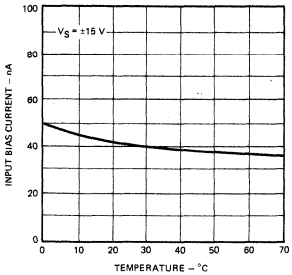
NOTES:

1. For supply voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C. Above $T_A = 70°C$, derate linearly at 8.3 mW/°C.
3. Short-circuit may be to ground, one amplifier only. $I_{SC} = 45$ mA (Typical).

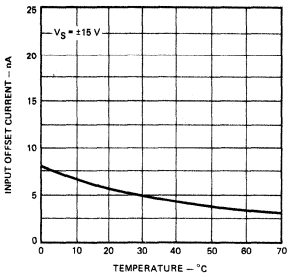
4

TYPICAL PERFORMANCE CURVES

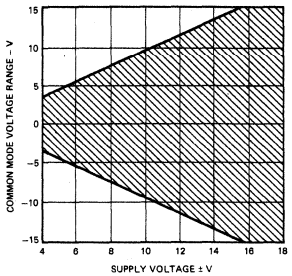
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



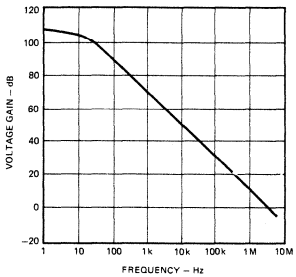
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



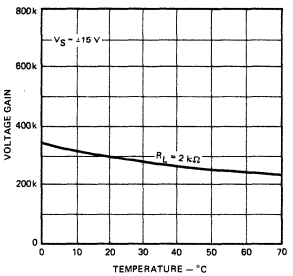
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



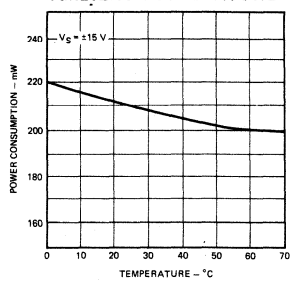
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



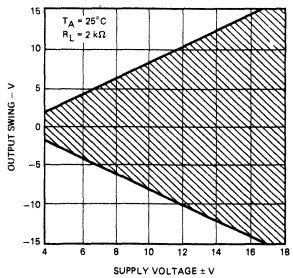
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



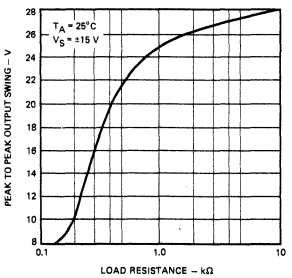
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



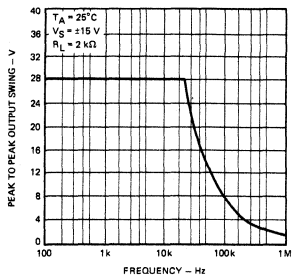
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



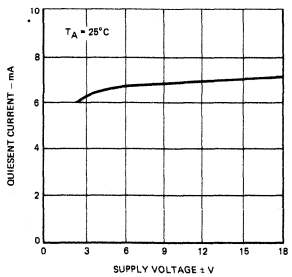
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



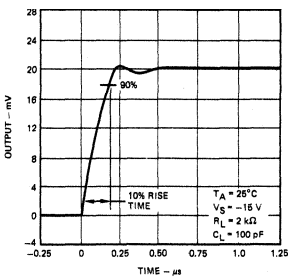
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



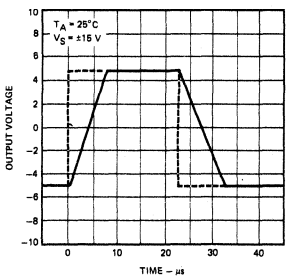
QUIESENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



TRANSIENT RESPONSE

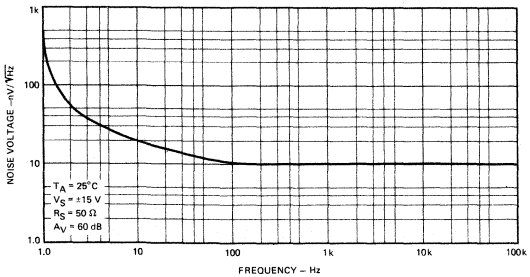


VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

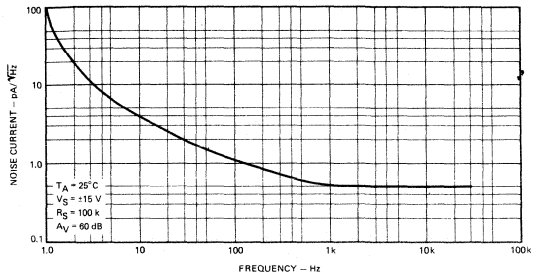


TYPICAL PERFORMANCE CURVES (Cont'd)

INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

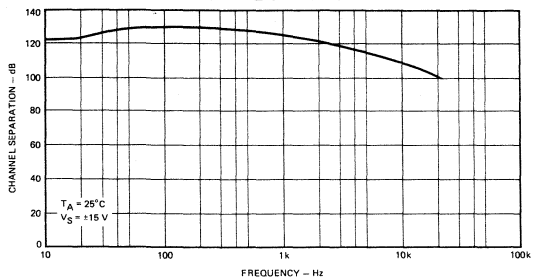


INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

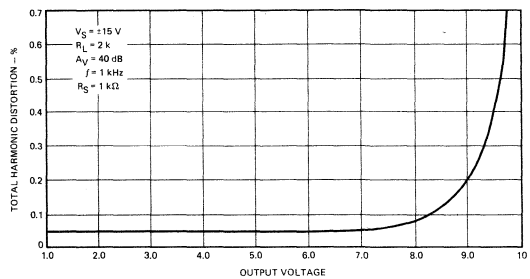


4

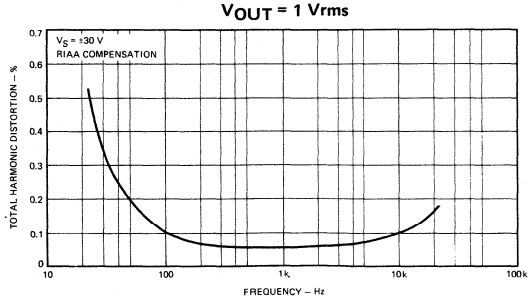
CHANNEL SEPARATION



TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT VOLTAGE f = 1 kHz

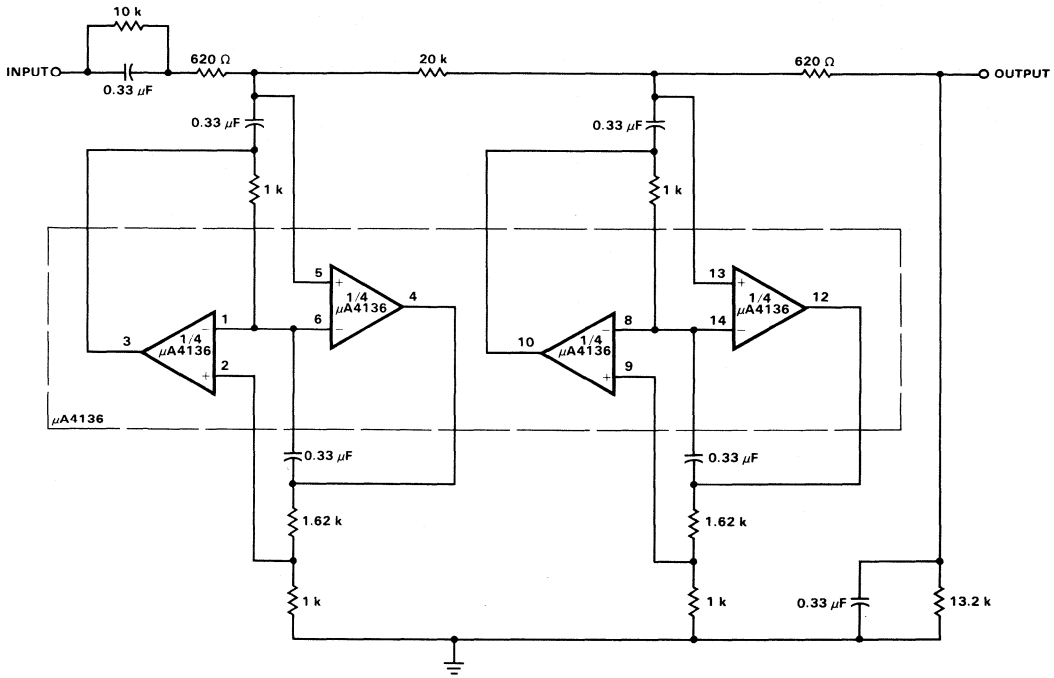


DISTORTION AS A FUNCTION OF FREQUENCY V_{OUT} = 1 Vrms

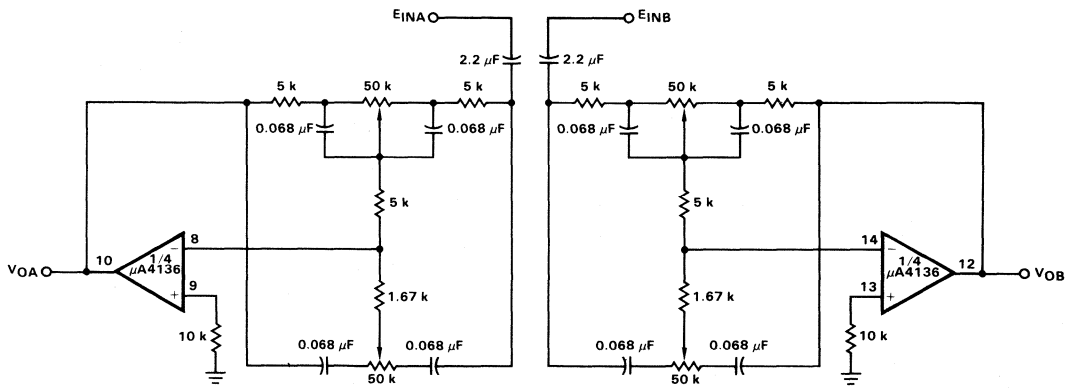


TYPICAL APPLICATIONS

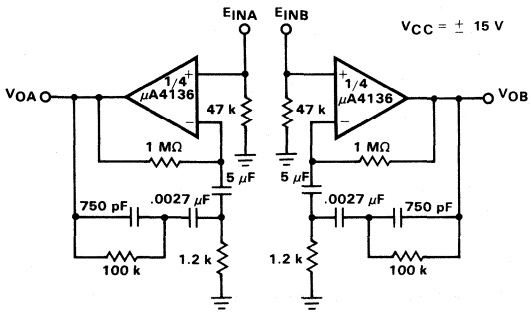
400 Hz LOWPASS BUTTERWORTH ACTIVE FILTER



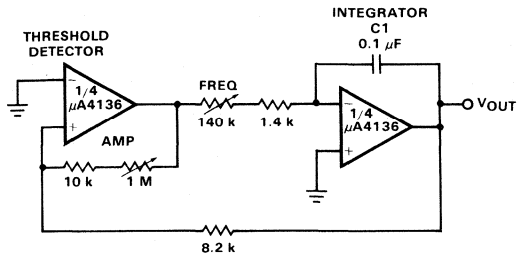
STEREO TONE CONTROL



RIAA PREAMPLIFIER

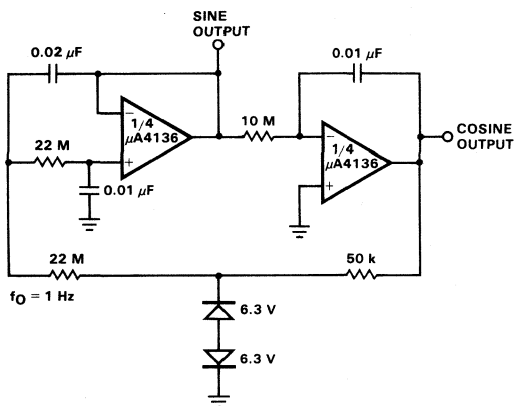


TRIANGULAR-WAVE GENERATOR

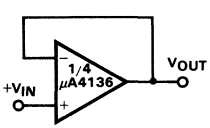


4

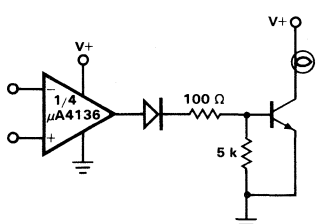
LOW FREQUENCY SINE WAVE GENERATOR WITH QUADRATURE OUTPUT



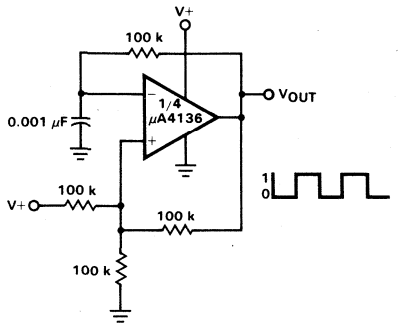
VOLTAGE FOLLOWER



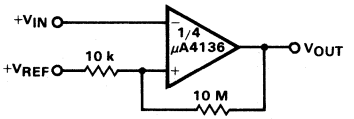
LAMP DRIVER



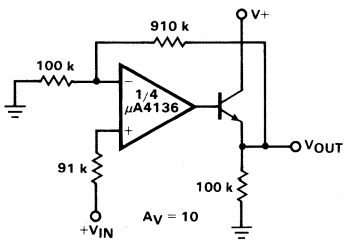
SQUAREWAVE OSCILLATOR



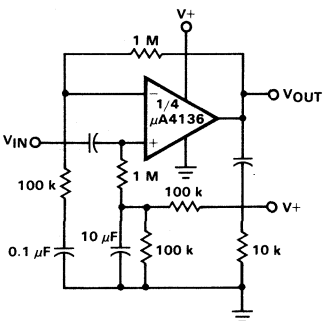
COMPARATOR WITH HYSTERESIS



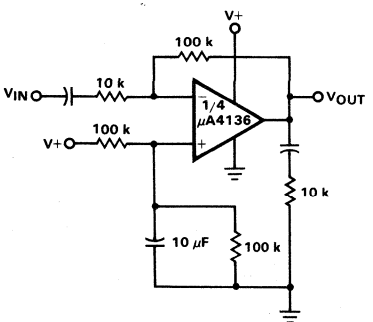
POWER AMPLIFIER



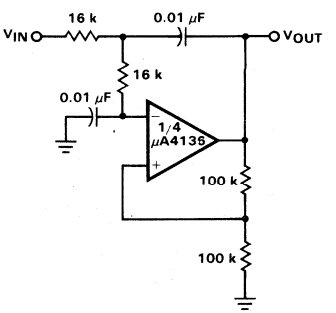
AC COUPLED NON-INVERTING AMPLIFIER



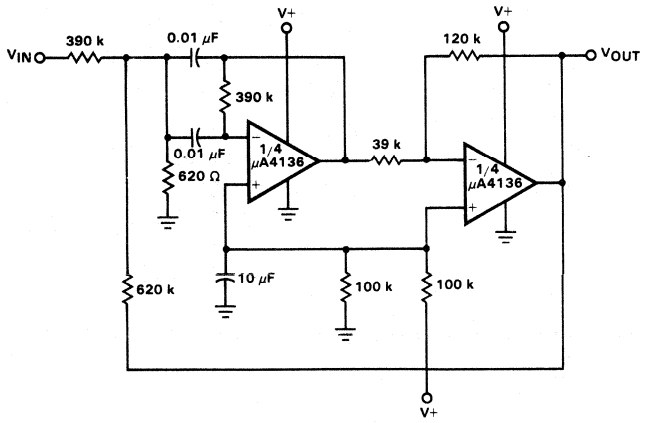
AC COUPLED INVERTING AMPLIFIER



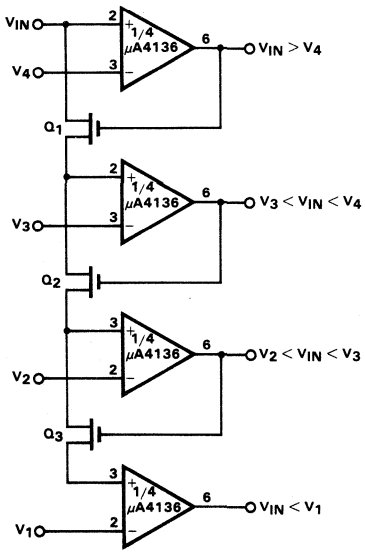
DC COUPLED 1 kHz LOW-PASS ACTIVE FILTER



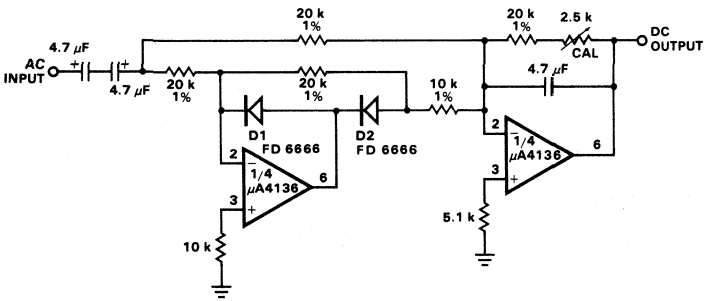
1 kHz BANDPASS ACTIVE FILTER



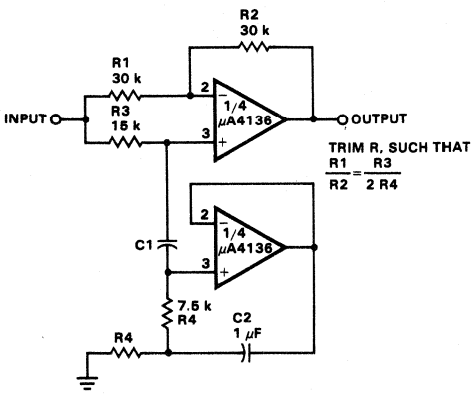
MULTIPLE APERTURE WINDOW DISCRIMINATOR



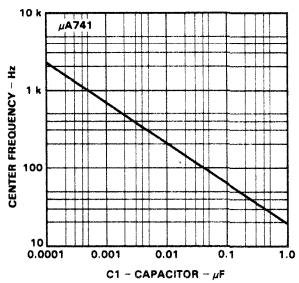
FULL-WAVE RECTIFIER AND AVERAGING FILTER



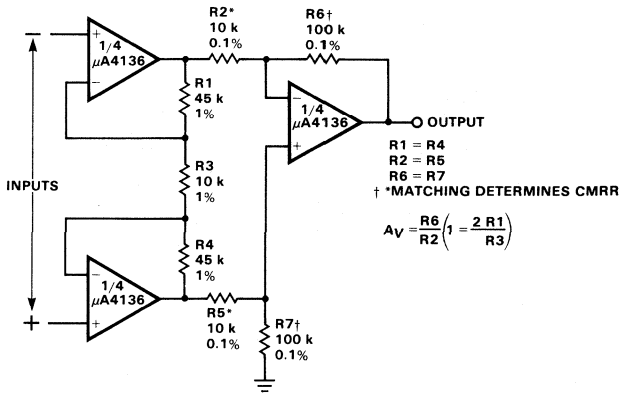
NOTCH FILTER USING THE μA4136 AS A GYRATOR



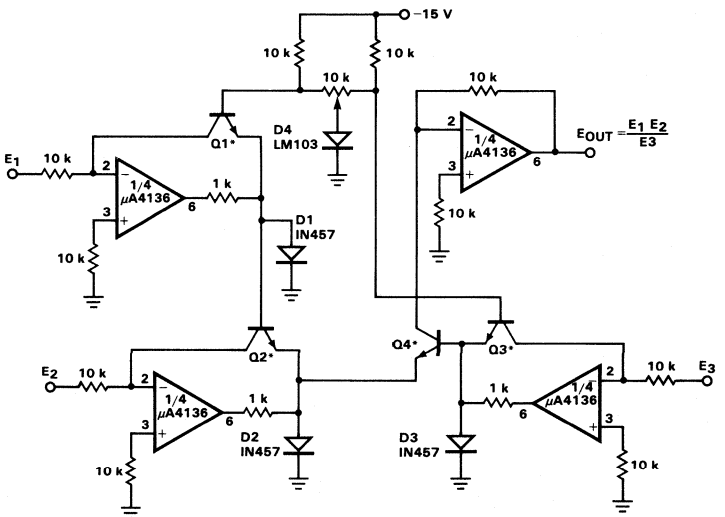
NOTCH FREQUENCY AS A FUNCTION OF C1



DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION



ANALOG MULTIPLIER/DIVIDER



μA4558

OPERATIONAL AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

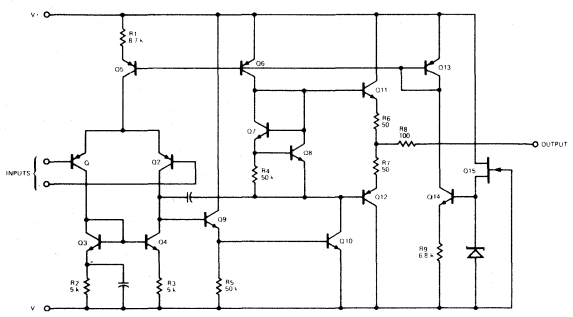
GENERAL DESCRIPTION – The μA4558 Monolithic Dual Operational Amplifiers consist of two independent high gain, internally frequency compensated operational amplifiers. The specially designed low noise input transistors allow the μA4558 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners. They are constructed using the Fairchild Planar* Epitaxial process. The simplified output stage completely eliminates crossover distortion under any load conditions, has large source and sink capacity, and is short-circuit protected. A novel current source stabilizes output parameters over a wide power supply voltage range.

- **UNITY GAIN BANDWIDTH 3 MHz**
- **CONTINUOUS SHORT CIRCUIT PROTECTION**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **NO LATCH-UP**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **PARAMETER TRACKING OVER TEMPERATURE RANGE**
- **GAIN AND PHASE MATCH BETWEEN AMPLIFIERS**

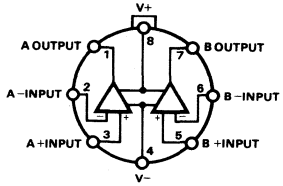
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA4558C	±18 V
μA4558	±22 V
Differential Input Voltage (Note 1)	±30 V
Input Voltage (Note 1)	±15 V
Internal Power Dissipation (Note 2)	670 mW
Output Short Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
μA4558	−55°C to +125°C
μA4558C	0°C to +70°C
Storage Temperature Range	
Molded Package	−55°C to +125°C
Hermetic Package	−65°C to +150°C
Pin Temperature	
Molded Package (Soldering, 10 s)	260°C
Hermetic Package (Soldering, 60 s)	300°C

1/2 OF EQUIVALENT CIRCUIT



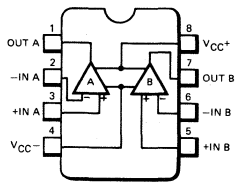
CONNECTION DIAGRAM
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B
PACKAGE CODE H



ORDER INFORMATION

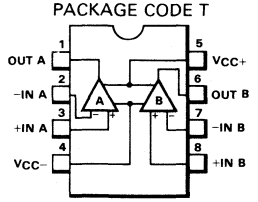
TYPE	PART NO.
μA4558C	μA4558HC
μA4558	μA4558HM

8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



TYPE	PART NO.
μA4558C	μA4558TC

8-PIN MINI CER DIP
(TOP VIEW)
PACKAGE OUTLINE 6T
PACKAGE CODE T



TYPE	PART NO.
μA4558C	μA4558RC
μA4558	μA4558RM

*Planar is a patented Fairchild process.

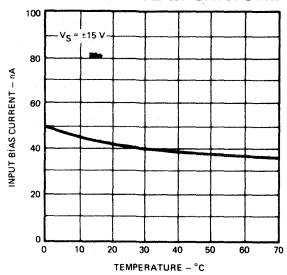
ELECTRICAL CHARACTERISTICS: T_A = 25°C, V_S = ±15 V unless otherwise specified

CHARACTERISTICS	CONDITIONS	μA4558			μA4558C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0		2.0	6.0	mV
Input Offset Current			30	200		30	200	nA
Input Bias Current			200	500		200	500	nA
Input Resistance		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	50,000	200,000		20,000	100,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Power Consumption			100	170		100	170	mW
Transient Response (unity Gain) Risetime	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF		0.13			0.13		μs
Transient Response (Unity Gain) Overshoot	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF		5.0			5.0		%
Unity Gain Bandwidth			3.0			3.0		MHz
Slew Rate (Unity Gain)	$R_L \geq 2$ kΩ		1.5			1.0		V/μs
Channel Separation (Open Loop)	f = 10 kHz, R_S = 1 kΩ		105			105		dB
	f = 10 kHz, R_S = 1 kΩ		105			105		dB
The following specifications apply for −55°C ≤ T_A ≤ +125°C for μA4136; 0°C ≤ T_A ≤ +70°C for μA4136C.								
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1500			800	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	25,000			15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ, V_S = ±15 V	±12			±10			V
Power Consumption	T_A = High		90	150		90	150	mW
	T_A = Low		120	200		120	200	

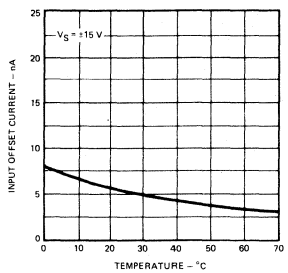
NOTES:
1. For supply voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70° C. Above T_A = 70°C, derate linearly at 6.3 °C/W for the hermetic package (5S) and 5.6°C/W for the molded package (9T).
3. Short circuit may be to ground, one amplifier only. I_{SC} = 45 mA (Typical).

TYPICAL PERFORMANCE CURVES

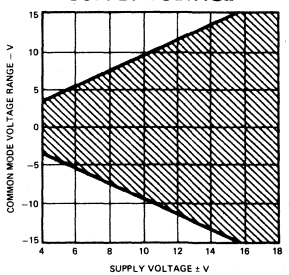
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

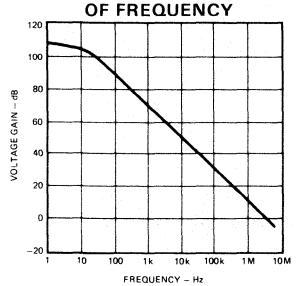


COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

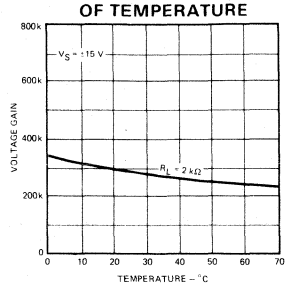


TYPICAL PERFORMANCE CURVES (Cont'd)

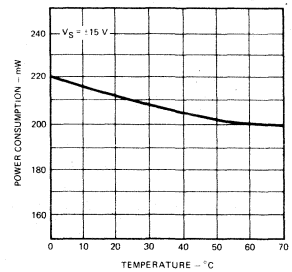
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



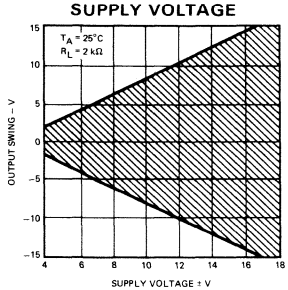
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



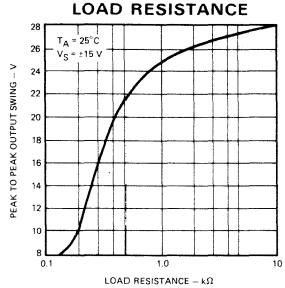
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



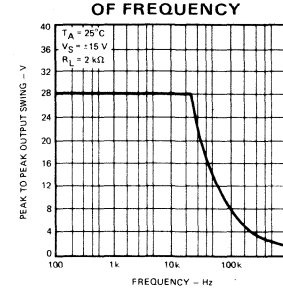
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



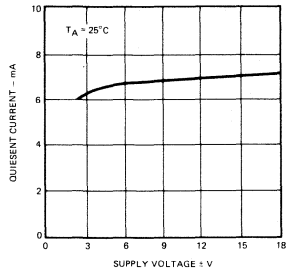
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



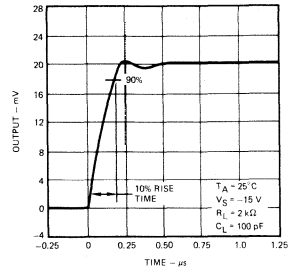
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



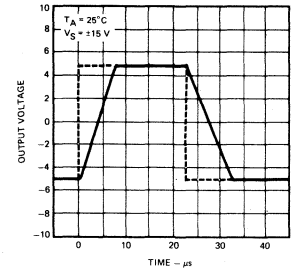
QUIESENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



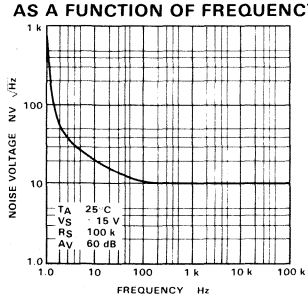
TRANSIENT RESPONSE



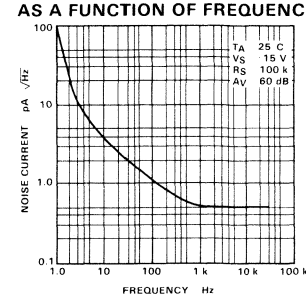
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



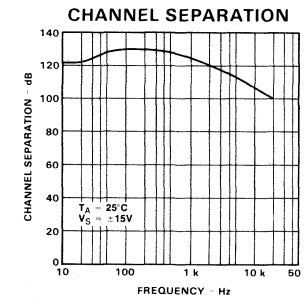
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



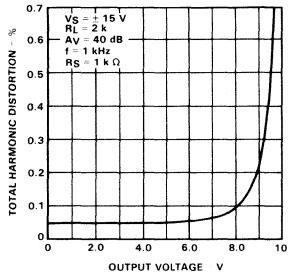
CHANNEL SEPARATION



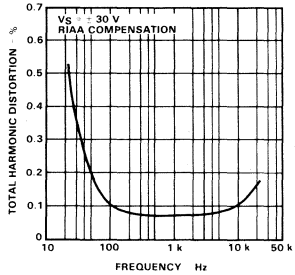
4

TYPICAL PERFORMANCE CURVES (Cont'd)

TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT VOLTAGE
f = 1 kHz



DISTORTION AS A FUNCTION OF FREQUENCY
V_{OUT} = 1 Vrms



μA7300

DOLBY B-TYPE NOISE REDUCTION SYSTEM

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA7300 is a monolithic circuit which performs *Dolby B-Type noise reduction processing on an audio signal. The Dolby B-Type noise reduction system is used to reduce hiss in consumer tape recording equipment and in FM broadcast receivers. The circuit is constructed using the Fairchild Planar** process.

The versatile circuit configuration of the μA7300 allows a complete record/playback system for a stereo tape recorder, or a complete stereo Dolby FM decoder, to be built with just two μA7300's and a few discrete components.

- **VERSATILE CONFIGURATION WITH PROGRAMMABLE INPUT, OUTPUT AMPLIFIERS**
- **SUPERIOR MATCHING TO DOLBY B-TYPE STANDARD**
- **EXCELLENT HIGH-FIDELITY CHARACTERISTICS**
- **WIDE OPERATING VOLTAGE RANGE: 10-20 V**

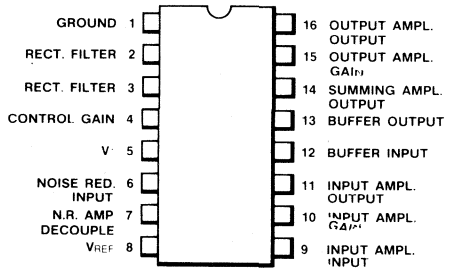
CONNECTION DIAGRAM

16-PIN DIP

TOP VIEW

PACKAGE OUTLINE 9B

PACKAGE CODE P



ORDER INFORMATION

TYPE	PART NO.
μA7300	**μA7300PC** (Note 1)

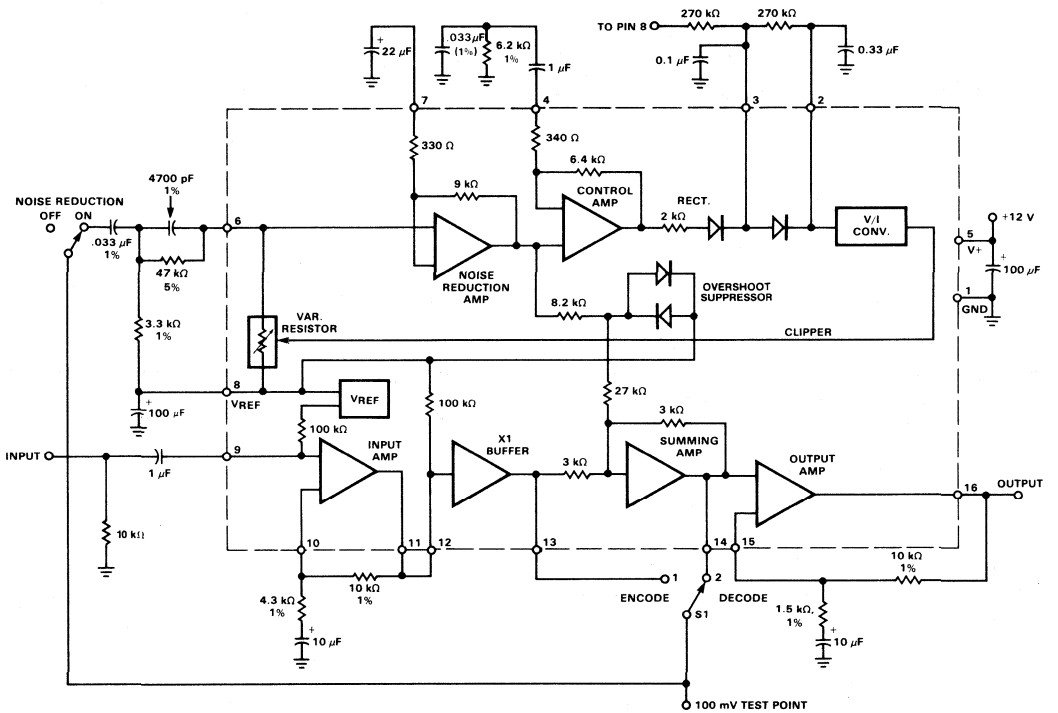
ABSOLUTE MAXIMUM RATINGS:

Supply Voltage	24 V
Operating Temperature Range	0° C to +70° C
Storage Temperature Range	-65° C to +150° C
Power Dissipation ($T_A \leq 70°$ C)	730 mW
Pin Temperature Soldering 10 s	280° C

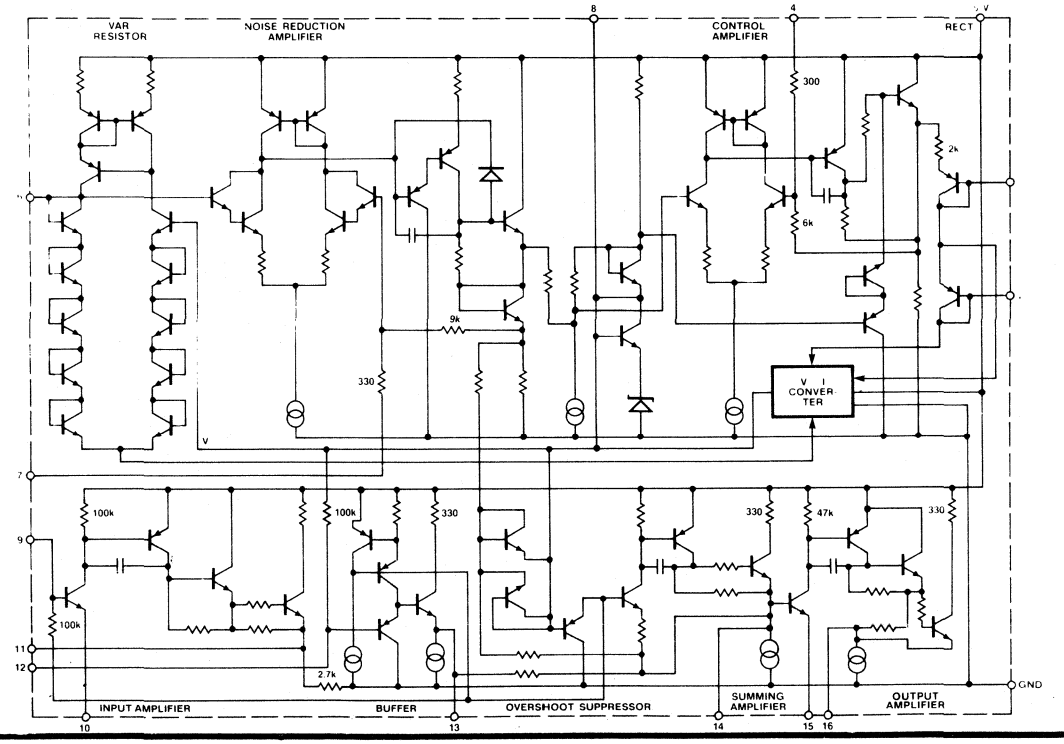
Note 1

This circuit is available only to licensees of Dolby Laboratories. Licensing and application information may be obtained from Dolby Laboratories, San Francisco.

μA7300 TEST CIRCUIT



μA7300 DOLBY NOISE REDUCTION SYSTEM EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS:

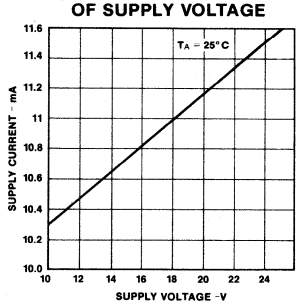
(T_A = 25° C, V+ = 12 V, input amplifier gain = 10 dB, source impedance less than 10 K, output amplifier gain = 17.7 dB (Output Level equals 775 mV for Dolby Level), encode mode, 0 dB = 100 mV_{rms} at test point unless otherwise specified. (See test circuit).

CHARACTERISTICS	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range			10		20	V
Supply Current				11	17	mA
Input Amplifier Current (Pins 10-11)				6		μA
Output Amplifier Current (Pins 15-16)				13		μA
Total Harmonic Distortion (Pin 16)	0 dB at Pin 13 +10 dB at Pin 13	f = 20-20,000 Hz f = 1 kHz		.04 0.1	0.1 0.3	% %
Signal Handling (Pin 16)	THD = 1.0%	R_L = 2 kΩ		6.4		V_{pk-pk}
Signal Handling (Pin 14)	THD = 1.0%		20			dB
Signal to Noise Ratio (Pin 16) Noise Level Relative to Dolby Level	CCIR/ARM Weighting Noise Reduction (ON)	ENCODE DECODE	65 75	68 78		dB dB
Encode Mode Frequency Response	f = 1.4 kHz Input at Pin 9	0 dB -20 dB -30 dB	-1 -17.1 -24.0	0 -15.6 -22.5	+1 -14.1 -21.0	dB dB dB
	f = 5 kHz Input at Pin 9	0 dB -20 dB -30 dB -40 dB	-0.7 -18.3 -23.3 -29.0	+0.3 -16.8 -21.8 -29.7	+1.3 -15.3 -20.3 -30.2	dB dB dB dB
	f = 20 kHz Input at Pin 9	0 dB -20 dB -30 dB -40 dB	-0.3 -18.8 -25.0 -29.0	+0.7 -17.3 -23.5 -29.7	+1.7 -15.8 -22.0 -30.2	dB dB dB dB
Back-to-Back Frequency Response	f = 20 - 20 kHz with respect to standard	+10 dB 0 dB -10 dB -20 dB -30 dB -40 dB	-1.0 -1.0 -1.0 -1.5 -1.5 -0.5		+1.0 +1.0 +1.0 +1.5 +1.5 +0.7	dB dB dB dB dB dB
Reference Voltage	I_B = -100 μA		6.0	6.6	7.2	V
Input Resistance	Pin 9		50	100		kΩ
Input Resistance	Pin 12		50	100		kΩ
Voltage Gain	Pin 12 to Pin 13;	f = 1 kHz		0		dB
Voltage Gain	Pin 12 to Pin 14;	f = 1 kHz		0		dB
Power Supply Ripple Rejection	f_R = 120 Hz			45		dB

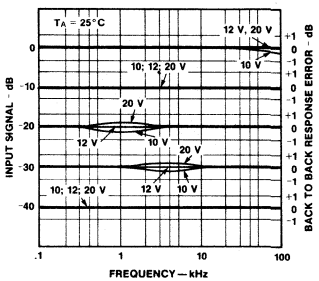
See Dolby Laboratories Engineering Field Bulletin 19/2.

TYPICAL PERFORMANCE CURVES

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

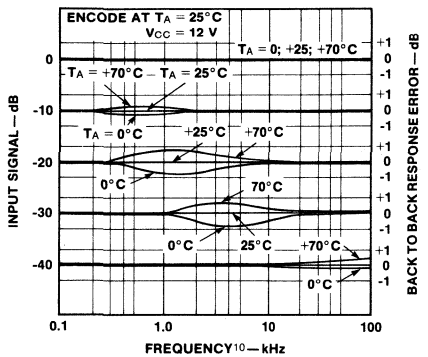


BACK TO BACK RESPONSE AS A FUNCTION OF POWER SUPPLY VOLTAGE

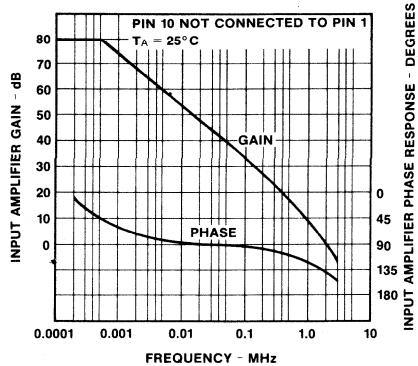


TYPICAL PERFORMANCE CURVES

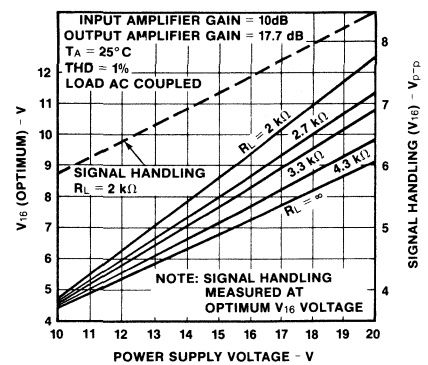
BACK TO BACK RESPONSE AS A FUNCTION OF TEMPERATURE



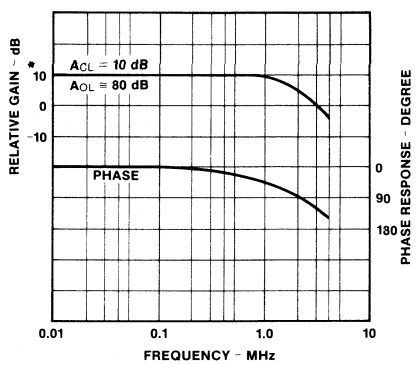
INPUT AMPLIFIER OPEN LOOP, GAIN, AND PHASE RESPONSE AS A FUNCTION OF FREQUENCY



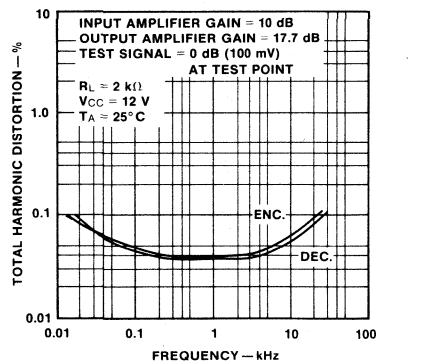
OUTPUT AMPLIFIER OPTIMUM V_{16} VOLTAGE AND SIGNAL HANDLING AS A FUNCTION OF POWER SUPPLY VOLTAGE



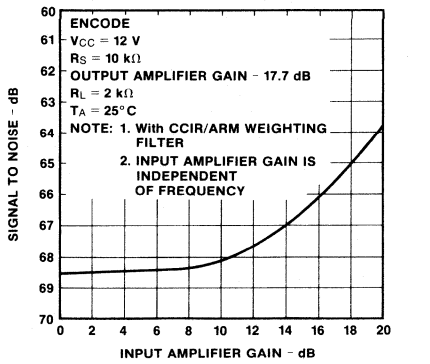
INPUT AMPLIFIER AMPLITUDE AND PHASE RESPONSE



TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY



SIGNAL TO NOISE AS A FUNCTION OF INPUT AMPLIFIER GAIN



μA7307

1.6 WATT AUDIO AMPLIFIER

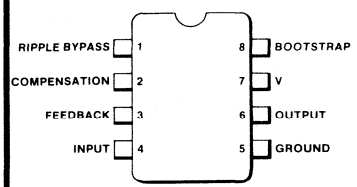
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA7307 is an integrated monolithic audio amplifier in an 8-pin plastic package. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is intended for use as a low frequency class B amplifier with wide range of supply voltage (3 to 16 V) and is primarily designed for low voltage portable radios and industrial applications where limited space and power consumption are important.

- **MINIMUM WORKING VOLTAGE OF 3 V**
- **LOW QUIESCENT CURRENT**
- **LOW NUMBER OF EXTERNAL COMPONENTS**
- **GOOD RIPPLE REJECTION**
- **NO CROSS-OVER DISTORTION**
- **TYPICAL OUTPUT POWER:**

1.6 W AT	**9 V - 4 Ω**
1.2 W AT	**9 V - 8 Ω**
0.75 W AT	**6 V - 4 Ω**
0.5 W AT	**6 V - 8 Ω**
0.22 W AT	**3.5 V - 4 Ω**
0.09 W AT	**3 V - 4 Ω**

CONNECTION DIAGRAM
8-PIN MINI-DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
7307C	**μA7307TC**

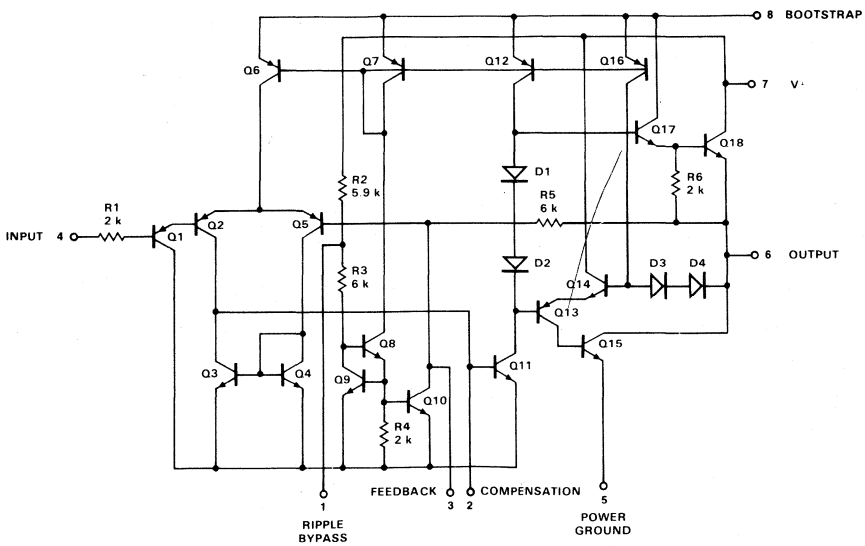
ABSOLUTE MAXIMUM RATINGS

Peak Voltage (Pin 8)	24 V
Supply Voltage	16 V
Output Peak Current	1.0 A
Power Dissipation at $T_{amb} \leq 50°C$	1.05 W
Storage and Junction Temperature	-40°C to 150°C
Lead Temperature (Soldering 10 s)	260°C

THERMAL DATA

θ_{j-amb} Thermal Resistance Junction-Ambient (copper frame) max 95°C/W

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: Power output measured at pin 6, $T_A = 25°C$ unless otherwise specified.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		3		16	V
Quiescent Output Voltage (Pin 6)	V+ = 9 V	4	4.5	5	V
Quiescent Drain Current	V+ = 9 V		4	9	mA
Bias Current (Pin 4)	V+ = 9 V		0.1	0.7	μA
Power Output, Figure 1	THD = 10%, R_{FB} = 120 Ω, f = 1 kHz,				
	V+ = 12 V, R_L = 8 Ω		2.0		W
	V+ = 9 V, R_L = 4 Ω		1.6		W
	V+ = 9 V, R_L = 8 Ω	0.9	1.2		W
	V+ = 6 V, R_L = 4 Ω		0.75		W
	V+ = 3.5 V, R_L = 4 Ω		0.22		W
	V+ = 3 V, R_L = 4 Ω		0.09		W
Input Sensitivity, Figure 1	P_{OUT} = 1.2 W, R_L = 8 Ω, V+ = 9 V, f = 1 kHz				
	R_{FB} = 33 Ω		16	24	mV
	R_{FB} = 120 Ω		60	82	mV
Input Sensitivity, Figure 1	P_{OUT} = 50 mW, R_L = 8 Ω, V+ = 9 V, f = 1 kHz				
	R_{FB} = 33 Ω		3.5		mV
	R_{FB} = 120 Ω		12		mV
Input Resistance			5		MΩ
Frequency Response (-3 dB) Figure 1	V+ = 9 V, R_L = 8 Ω, R_{FB} = 120 Ω				
	C_{FB} = 680 pF		25-7000		Hz
	C_{FB} = 220 pF		25-20,000		Hz
Total Harmonic Distortion Figure 1	P_{OUT} = 500 mW, R_L = 8 Ω, V+ = 9 V, f = 1 kHz				
	R_{FB} = 33 Ω		0.8		%
	R_{FB} = 120 Ω		0.4		%
Voltage Gain (Open Loop)	V+ = 9 V, R_L = 8 Ω, f = 1 kHz		75		dB
Voltage Gain (Closed Loop)	V+ = 9 V, R_L = 8 Ω, f = 1 kHz				
	R_{FB} = 33 Ω		45		dB
	R_{FB} = 120 Ω	31	34	37	dB
Input Noise Voltage	V+ = 9 V, BW (-3.0 dB) = 25-20,000 Hz		3.5		μV
Input Noise Current	V+ = 9 V, BW (-3.0 dB) = 25-20,000 Hz		0.4		nA
Signal Plus Noise to Noise Ratio	V+ = 9 V, R_L = 8 Ω, R_{FB} = 120 Ω				
	BW (-3.0 dB) = 25-20,000 Hz				
	R_1 = 100 kΩ, P_{OUT} = 1.2 W		70		dB
Supply Voltage Rejection, Figure 2	V = 9 V, R_L = 8 Ω, f (ripple) = 100 Hz,				
	C6 = 50 μF, R_{FB} = 120 Ω		42		dB

APPLICATIONS INFORMATION

Two typical application circuits are shown in *Figures 1* and *2*. The ripple bypass capacitor C6 may be omitted in most battery operated applications or where high ripple rejection is not required.

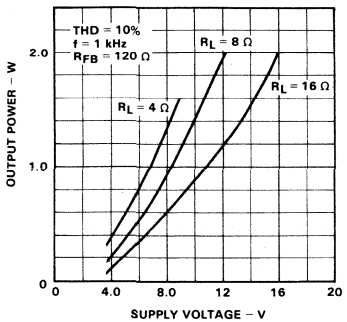
Resistor R2 must be included in series with C3 to assure stable operation of the μA7307.

A PC board layout for the circuit of *Figure 1* is shown to scale in *Figure 3*. A photograph of a finished module is shown in *Figure 4*.

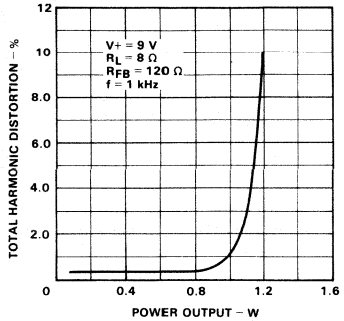
The PC board layout for the circuit of *Figure 2* is shown to scale in *Figure 5*, and a photograph is shown in *Figure 6*.

TYPICAL PERFORMANCE CURVES

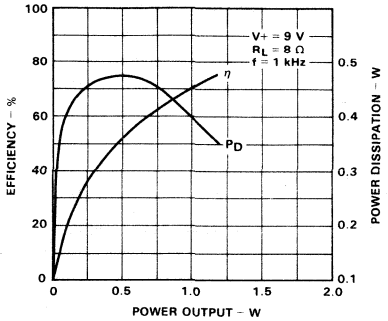
OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE



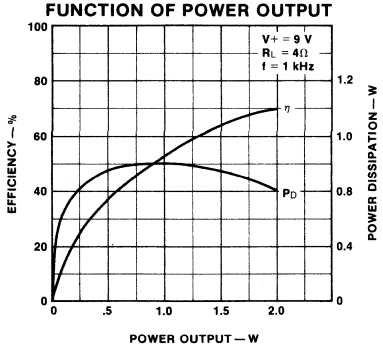
TOTAL HARMONIC DISTORTION AS A FUNCTION OF POWER OUTPUT



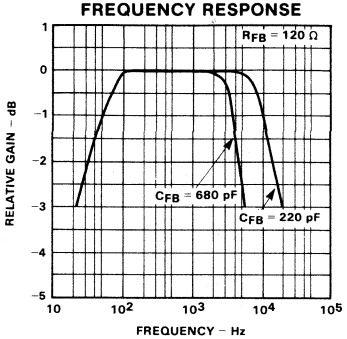
POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF POWER OUTPUT



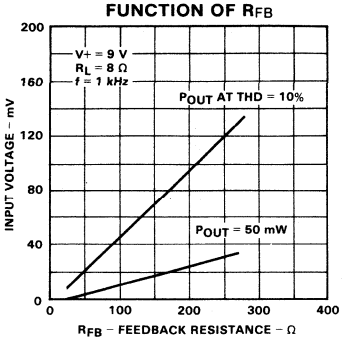
POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF POWER OUTPUT



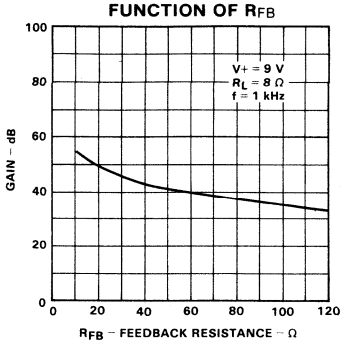
TYPICAL RELATIVE FREQUENCY RESPONSE



INPUT SENSITIVITY AS A FUNCTION OF R_{FB}

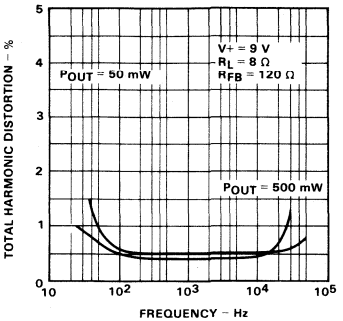


TYPICAL VOLTAGE GAIN (CLOSED LOOP) AS A FUNCTION OF R_{FB}

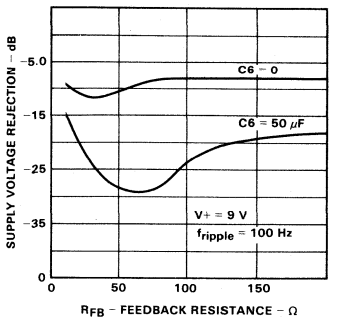


TYPICAL PERFORMANCE CURVES

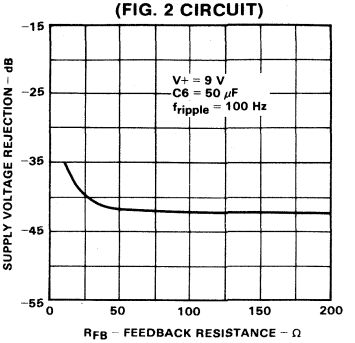
TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY



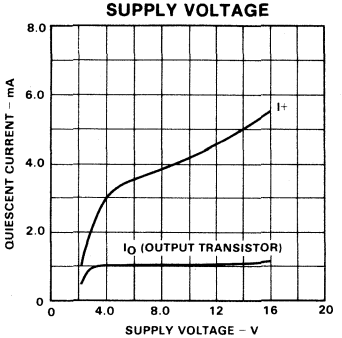
SUPPLY VOLTAGE REJECTION AS A FUNCTION OF RFB FOR FIG. 1 CIRCUIT



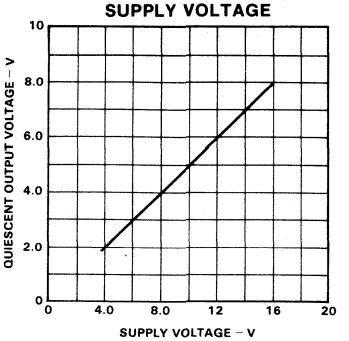
SUPPLY VOLTAGE REJECTION AS A FUNCTION OF RFB (FIG. 2 CIRCUIT)



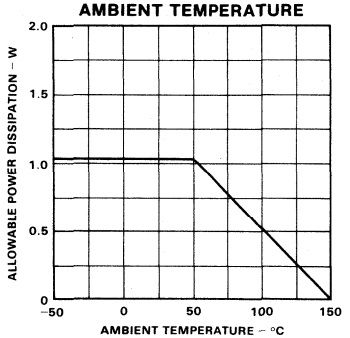
QUIESCENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



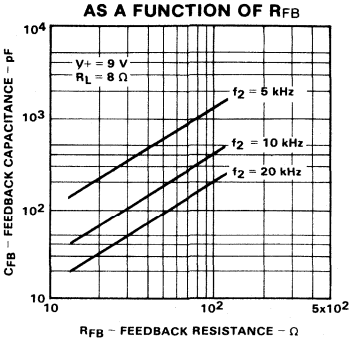
QUIESCENT OUTPUT VOLTAGE AT PIN 12 AS A FUNCTION OF SUPPLY VOLTAGE



POWER RATING CHART AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL VALUE OF CFB AS A FUNCTION OF RFB



TEST AND APPLICATION CIRCUITS

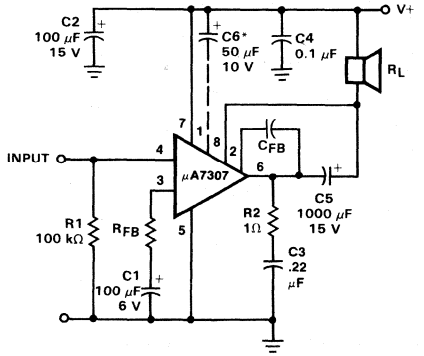
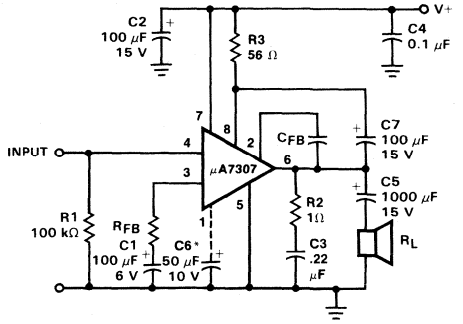


Fig. 1 Circuit Diagram with Load Connected to the Supply Voltage



*Capacitor C6 must be used when high ripple rejection is desired.

Fig. 2 Circuit Diagram with Load Connected to Ground

Bottom View

Fig. 3 1:1 Scale P.C. Board Layout for Circuit of Figure 1

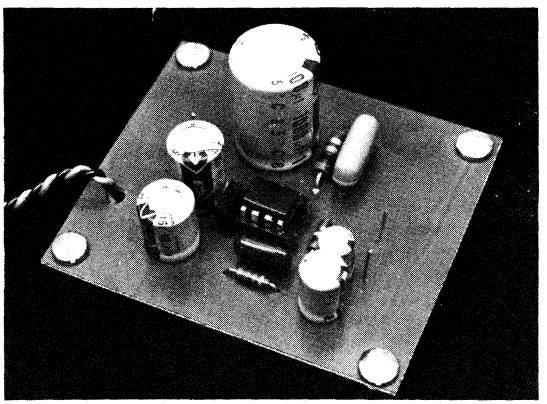


Fig. 4 Photograph of Assembled Board for Figure 1

Bottom View

Fig. 5 1:1 Scale P.C. Board Layout for Circuit of Figure 2

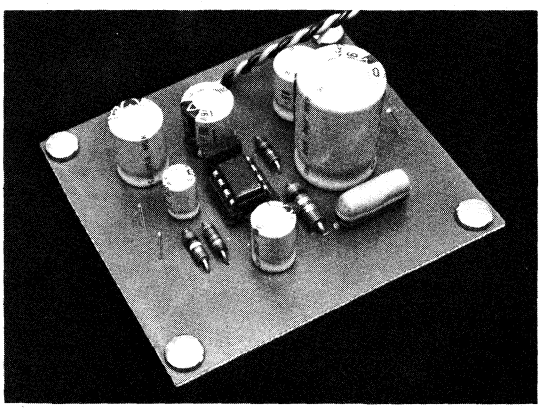


Fig. 6 Photograph of Assembled Board for Figure 2

μA7390

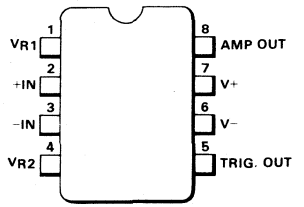
GROUND FAULT DETECTOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA7390 is a monolithic ground fault detector circuit utilizing the Fairchild Planar* Epitaxial Process. It is designed for use in class A Ground Fault Circuit Interrupters for operation directly off the ac line in either breakers or receptacles. The μA7390 contains an operational amplifier, a threshold detector, and a driver capable of providing high energy pulses for thyristor triggering.

- **OPERATES DIRECTLY FROM AC LINE**
- **BUILT IN 24 V REGULATOR**
- **HIGH GAIN OPERATIONAL AMPLIFIER**
- **50 mA OUTPUT CURRENT PULSE TO TRIGGER SCRs**
- **LOW EXTERNAL PART COUNT**
- **MINI-DIP PACKAGE**
- **HIGH NOISE IMMUNITY**

CONNECTION DIAGRAM
8-PIN MINI-DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

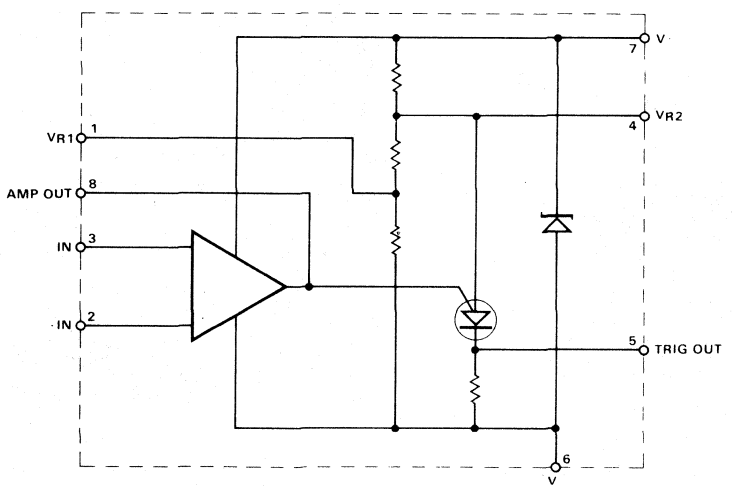
TYPE	PART NO.
μA7390	μA7390TC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Limited by Internal Zener (Note 1)	
Supply Current (Note 2)	40 mA
Power Dissipation (Note 3)	560 mW
Storage Temperature Range	−55°C to +125°C
Operating Temperature	−40°C to +85°C
Pin Temperature (soldering 10 s)	260°C

NOTES:
1. Device must always have a series resistor between the supply and pin 7, which limits current to 40 mA maximum.
2. Single cycle 60 Hz surge current. Steady state current limited by Power Dissipation.
3. Power Dissipation applies to case temperature of 25°C derate at 5.6 mW/°C.

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: T_A = 25°C. I_S = 10 mA unless otherwise specified

CHARACTERISTICS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
POWER SUPPLY					
Zener Voltage		21	23.5	26	V
Zener Series Resistance			50	100	Ω
Ratio of V_{R1} to Zener Voltage		0.3	0.33	0.37	
Ratio of V_{R2} to Zener Voltage		0.6	0.63	0.67	
OPERATIONAL AMPLIFIER					
Input Offset Voltage	$R_S \leq 50\ \Omega$		2.0	5.0	mV
Input Offset Current			30	100	nA
Input Bias Current			150	400	nA
Large Signal Voltage Gain	R_L = 100 k	8.0	15		V/mV
Output Source Current	V_{OUT} = 7.0 V	0.35	0.5	0.65	mA
Output Sink Current	V_{OUT} = 7.0 V	2.0	3.0	4.0	mA
OUTPUT TRIGGER					
Peak Output Current	V_{OUT} Trigger = 1.5 V	50	70		mA
Output Impedance	I = 10 mA	35	50	65	Ω

APPLICATIONS

GROUND FAULT BREAKER

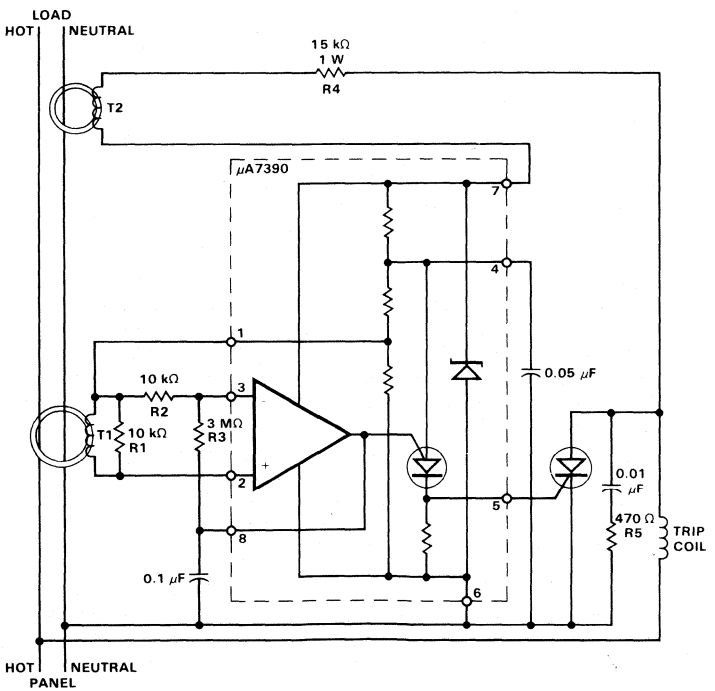


Fig. 1

APPLICATIONS (Cont'd)

FULL WAVE GFI FOR RECEPTACLE

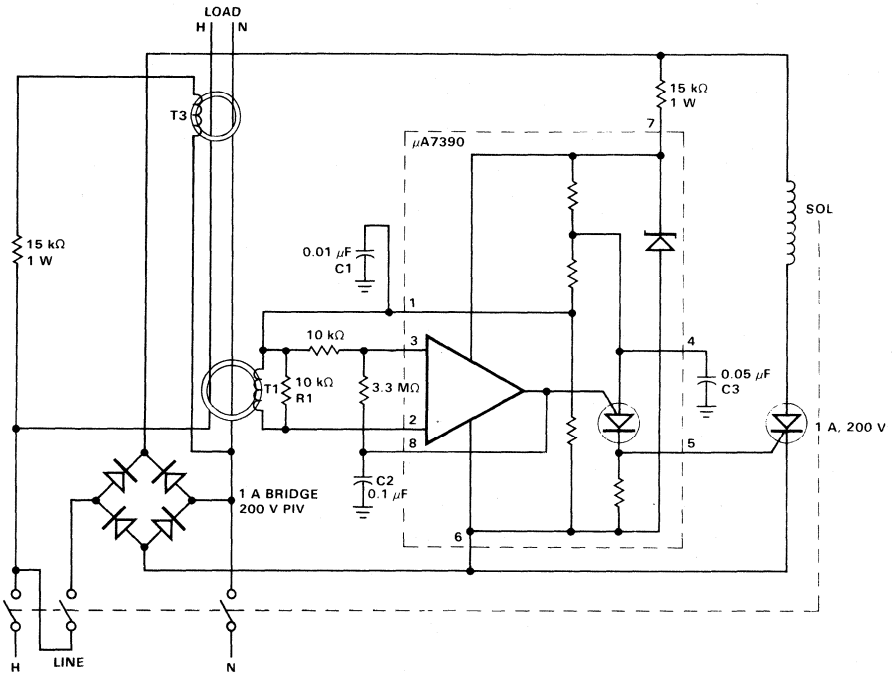


Fig. 2

Figure 1 shows the μA7390 connected in a typical Ground Fault Interrupter System. Power is applied to the V+ terminal of the μA7390 directly from the hot power line through a 15 kΩ resistor and the primary winding of transformer, T2. This limits the supply current into the μA7390 to a peak of 10 mA. The internal zener diode clamps the supply voltage to 23.5 V during the positive half-cycle and to more than minus 1 V during the negative half-cycle. The system therefore functions only on positive half-cycles of the line voltage.

Ground Fault currents (any currents in the hot line that are not returned in the neutral line) are detected by the differential current transformer, T1. The output voltage signal of T1 is amplified by the μA7390 operational amplifier and appears as a half-cycle sine wave signal referenced to V_{R2} at the output of the amplifier. The amplifier closed-loop gain is adjusted by modifying the external input and feedback resistors to compensate for transformer variations. When the peak signal amplitude equals V_{R2} + 0.6 V, the output trigger will fire and discharge the .1 μF capacitor connected to amp-out and the 0.05 μF capacitor connected to V_{R2} into the gate of the external SCR which energizes the trip coil which opens the circuit breaker. The .01 μF capacitor and the 470 Ω resistor are for transient suppression.

The transformer, T2, induces a small voltage, on the order of 10-20 mV on the neutral line with respect to ground so that a short from neutral load to ground will cause a fault current to flow in the neutral line of sufficient magnitude to cause the breaker to open as required for Class A Ground Fault Interrupter operation.

Figure 2 shows a typical full wave ground fault interrupter system. The full wave bridge supplies power to the μA7390 during both the positive and negative half-cycles of the line voltage. This allows the hot and neutral lines to be interchanged. The use of a third breaker contact allows interchanging the line and load sides of the breaker system. These two features allow the use of this system in ground fault interrupter receptacle applications.

μA7391

DC MOTOR SPEED CONTROL CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUIT

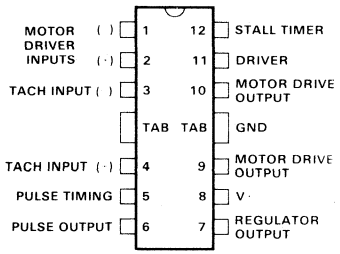
GENERAL DESCRIPTION – The μA7391 is designed for precision, closed-loop, motor speed control systems. It regulates the speed of capstan drive motors in automotive and portable tape players and is useful in a variety of industrial control applications, *e.g.,* floppy disc drive systems, data cartridge drive systems. The device is constructed using the Fairchild Planar* epitaxial process.

The μA7391 compares actual motor speed to an externally presettable reference voltage. The motor speed is determined by frequency to voltage conversion of the input signal provided by tachometer generator. The result of the comparison controls the duty cycle of the pulse width modulated switching motor drive output stage to close the system's negative feedback loop.

Thermal and over-voltage shutdown are included for self-protection, and a "stall-timer" feature allows the motor to be protected from burn-out during extended mechanical jams.

- **PRECISION PERFORMANCE – FREQUENCY-TO-VOLTAGE CONVERSION STABILITY TYPICALLY 0.1% FOR V+ FROM 10 V TO 16 V; 0.3% FOR CASE TEMPERATURE FROM −40°C TO +85°C**
- **HIGH CURRENT PERFORMANCE – 3.5 A STARTING SURGE CURRENT AND 2 A RUNNING CURRENT TO A DC MOTOR**
- **WIDE RANGE TACHOMETER INPUT – 100 mVp-p TO 1.0 Vp-p**
- **LOW EXTERNAL PARTS COUNT**
- **THERMAL SHUTDOWN, OVER-VOLTAGE AND STALL PROTECTION**
- **INTERNAL REGULATOR**
- **WIDE SUPPLY VOLTAGE RANGE – 6.3 V TO 16 V**

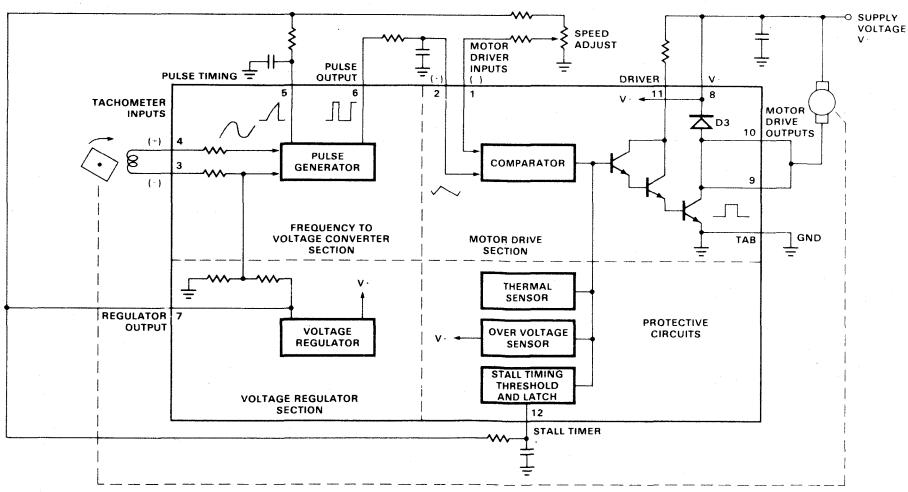
CONNECTION DIAGRAM
12-PIN POWER PACKAGE
(TOP VIEW)
PACKAGE OUTLINE 9W
PACKAGE CODE P6



ORDER INFORMATION

TYPE	PART NO.
μA7391	μA7391PC

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+), V_8	24 V
Regulator Output Current, I_7	15 mA
Voltage Applied to Pin 5 (Tachometer Pulse Timing)	7 V
Voltage Applied Between Pins 3 and 4 (Tachometer Inputs)	±6 V
DC Voltage Applied to Pin 11 (Driver)	24 V
DC Voltage Applied to Pins 9 or 10 (Motor Drive Output)	V+
Continuous Current through pins 9 and 10:	
Motor Drive Output ON	2.0 A
Repetitive Surge Current through Pins 9 and 10:	
Motor Drive Output ON	3.5 A
Motor Drive Output OFF	2.0 A
Repetitive Surge Current through Pin 11	300 mA
Power Dissipation	Internally Limited
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 s)	260°C

THERMAL DATA

θ_{JC}	Thermal Resistance Junction to Case (tab) (max)	12°C/W
θ_{JA}	Thermal Resistance Junction to Ambient (max)	**70°C/W

**Obtained with tabs soldered to a printed circuit board having a minimum area of copper surrounding the tabs.

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, TA = 25°C, unless otherwise noted

VOLTAGE REGULATOR SECTION: (TEST CIRCUIT 1)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	Excluding Current into Pins 9, 10 and 11		7.5	10	mA
Regulator Output Voltage		4.5	5.0	5.5	V
Regulator Output Line Regulation (ΔV_7)	V+ from 10 V to 16 V V+ from 6.3 V to 16 V		6.0 12	20 50	mV mV
Regulator Output Load Regulation (ΔV_7)	I_7 from 10 mA to 0		40		mV

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, TA = 25°C, unless otherwise noted

FREQUENCY TO VOLTAGE CONVERTER SECTION: (TEST CIRCUIT 2)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Tachometer (−) Input Bias Voltage			2.4		V
Tachometer (+) Input Bias Current	$V_4 = V_3$		1.0	10	μA
Tachometer Input Positive Threshold	($V_4 - V_3$)	10	25	50	mV_{pk}
Tachometer Input Hysteresis		20	50	100	mV_{p-p}
Pulse Timing ON Resistance	$V_5 = 1$ V		300	500	Ω
Pulse Timing Switch Threshold		45	50	55	$\%V_7$
Output Pulse Rise Time			0.3		μs
Output Pulse Fall Time			0.1		μs
Pulse Output LOW Saturation (V_6)			0.13	0.25	V
Pulse Output HIGH Saturation ($V_7 - V_6$)			0.12	0.2	V
Pulse Output HIGH Source Current	$V_6 = 1$ V	−340	−260	−180	μA
Frequency-to-Voltage Conversion Supply Voltage Stability (Note 1)	$V_{FV} = 0.25\ V_7$ (Note 2) V+ from 10 V to 16 V		0.1		%
Frequency-to-Voltage Conversion Temperature Stability (Note 3)	$V_{FV} = 0.25\ V_7$ (Note 2) T_A from −40°C to +85°C		0.3		%

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, TA = 25°C, unless otherwise noted

MOTOR DRIVE SECTION: (TEST CIRCUIT 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage				±20	mV
Input Bias Current			0.1	10	μA
Common Mode Range		0.8		2.5	V
Driver Saturation	$I_9 + I_{10}$ = 2 A, I_{11} = 175 mA		1.9	2.5	V
Driver Leakage Current	V_{11} = 16 V			5.0	μA
Motor Drive Output Saturation	$I_9 + I_{10}$ = 2 A, I_{11} = 55 mA		0.6	1.1	V
Motor Drive Output Leakage	$V_8 = V_9 = V_{10}$ = 16 V			100	μA
Flyback Diode Leakage	$V_9 = V_{10}$ = 1 V			30	μA
Flyback Diode Clamp	$I_9 + I_{10}$ = 2 A Motor Drive Output Off		1.6	2.5	V

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, TA = 25°C, unless otherwise noted

PROTECTIVE CIRCUITS: (TEST CIRCUIT 4)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Junction Temperature	Note 4		160		°C
Overvoltage Shutdown	Note 4	18	21	24	V
Stall Timer Threshold Voltage	Note 5	2.5	2.9	3.5	V
Stall Timer Threshold Current	Note 5		0.3	3.0	μA

NOTES:

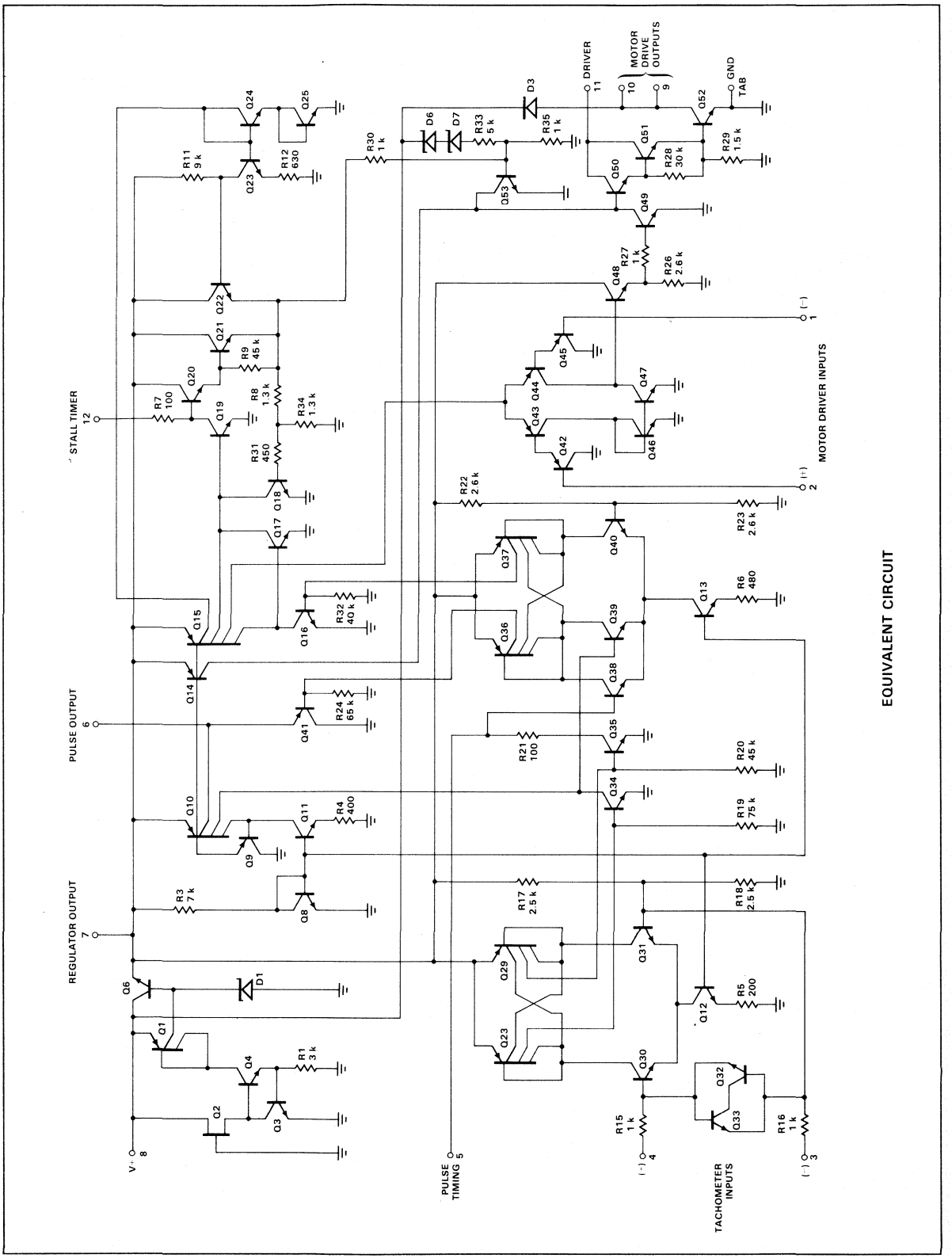
1. Frequency-to-Voltage Conversion, Supply Voltage Stability is defined as:

$$\left[\frac{V_{FV(16\ V)}}{V_{7(16\ V)}}\right] - \left[\frac{V_{FV(10\ V)}}{V_{7(10\ V)}}\right] \div \left[\frac{V_{FV(14.5\ V)}}{V_{7(14.5\ V)}}\right] \times 100\%$$

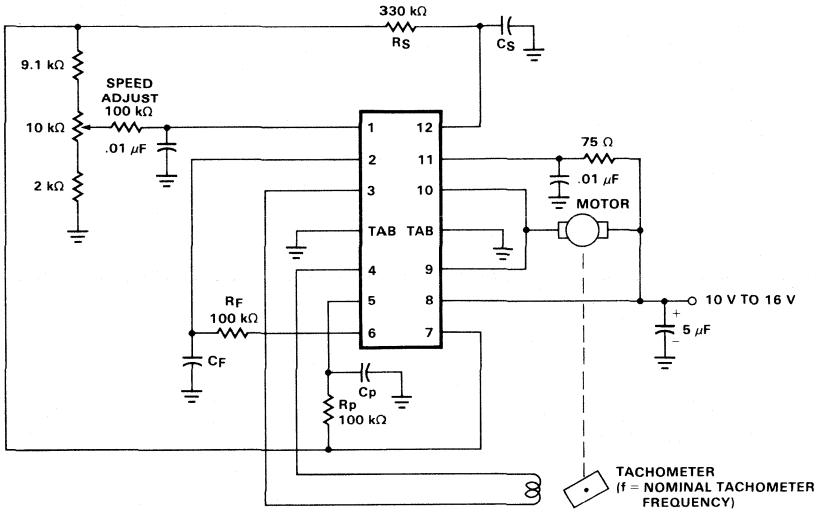
2. V_{FV} is the integrated dc output voltage from the pulse generator (Pin 6)
3. Frequency-to-Voltage Conversion Temperature Stability is defined as:

$$\left[\frac{V_{FV(85°C)}}{V_{7(85°C)}}\right] - \left[\frac{V_{FV(-40°C)}}{V_{7(-40°C)}}\right] \div \left[\frac{V_{FV(25°C)}}{V_{7(25°C)}}\right] \times 100\%$$

4. "Driver" and "Motor Drive" circuitry is disabled when these limits are exceeded. If the condition continues for the duration set by the external stall timer components, the circuit is latched off until reset by temporarily opening the power supply input line.
5. If stall timer protection is not required, Pin 12 should be grounded.


EQUIVALENT CIRCUIT
STALL TIMER 12
PULSE OUTPUT 6
REGULATOR OUTPUT 7
V+ 8
PULSE TIMING 5
(-) 4
TACHOMETER INPUTS
(-) 3
(+) 2
(-) 1
MOTOR DRIVER INPUTS
DRIVER 11
MOTOR DRIVE OUTPUTS 10
9
GND TAB
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q22 Q23 Q24 Q25 Q26 Q27 Q28 Q29 Q30 Q31 Q32 Q33 Q34 Q35 Q36 Q37 Q38 Q39 Q40 Q41 Q42 Q43 Q44 Q45 Q46 Q47 Q48 Q49 Q50 Q51 Q52 Q53
D1 D2 D3 D4 D5 D6 D7
R1 3 k
R2 7 k
R3 7 k
R4 400
R5 200
R6 480
R7 100
R8 1.3 k
R9 45 k
R10 1 k
R11 9 k
R12 630
R13 1 k
R14 1 k
R15 1 k
R16 1 k
R17 2.5 k
R18 2.5 k
R19 75 k
R20 45 k
R21 100
R22 2.6 k
R23 2.6 k
R24 65 k
R25 1 k
R26 2.6 k
R27 1 k
R28 30 k
R29 1.5 k
R30 1 k
R31 450
R32 40 k
R33 5 k
R34 1.3 k
R35 1 k

TYPICAL APPLICATION USING MAGNETIC TACHOMETER



TYPICAL COMPONENT VALUES:

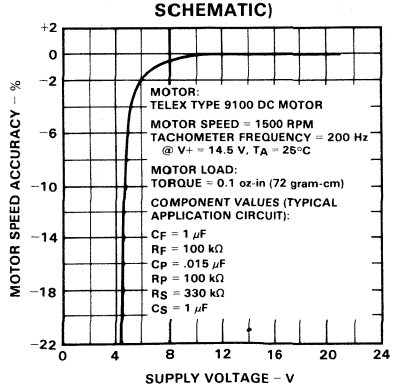
$$Cp = \frac{1}{4\ Rpf}$$

C_F = 10 Cp to 1000 Cp depending on system requirements

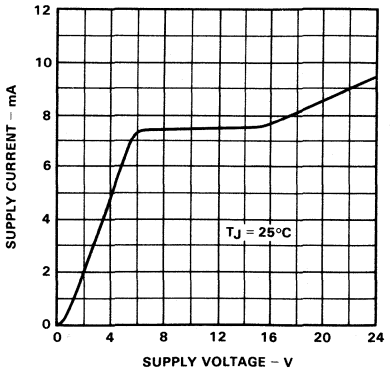
$$CS = \frac{2 \times \textit{stall time-out}}{RS}$$

$R_{Motor} \geqslant 5\ \Omega$

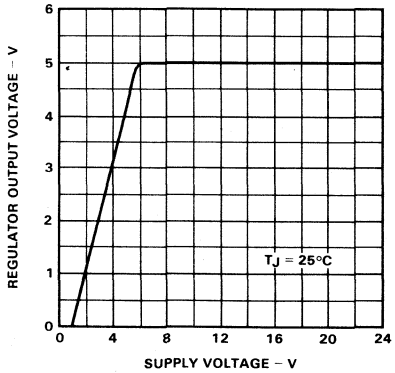
MOTOR SPEED ACCURACY AS A FUNCTION OF SUPPLY VOLTAGE (REFER TO APPLICATION SCHEMATIC)



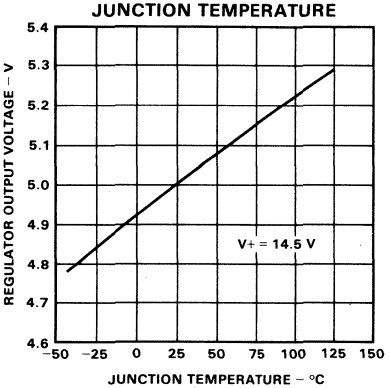
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



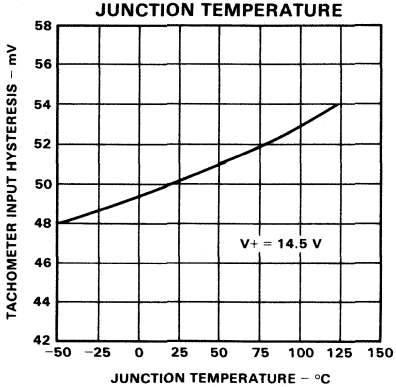
REGULATOR OUTPUT VOLTAGE AS A FUCTION OF SUPPLY VOLTAGE



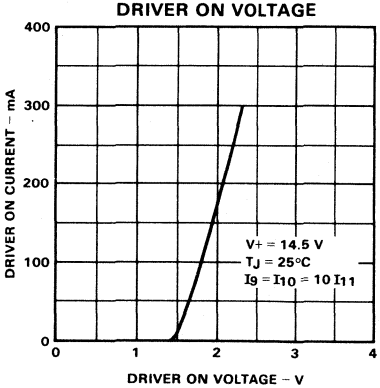
REGULATOR OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



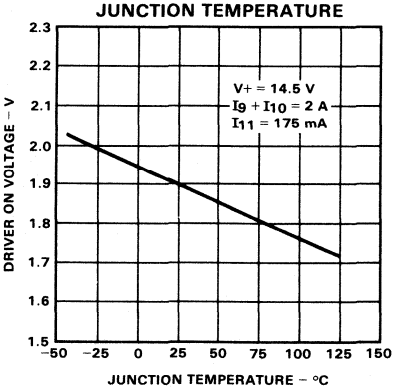
TACHOMETER INPUT HYSTERESIS AS A FUNCTION OF JUNCTION TEMPERATURE



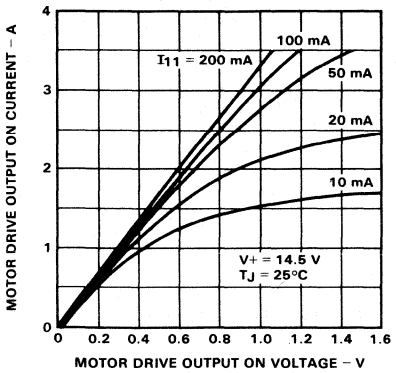
DRIVER ON CURRENT AS A FUNCTION OF DRIVER ON VOLTAGE



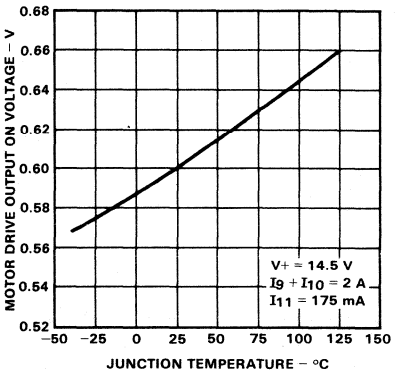
DRIVER ON VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



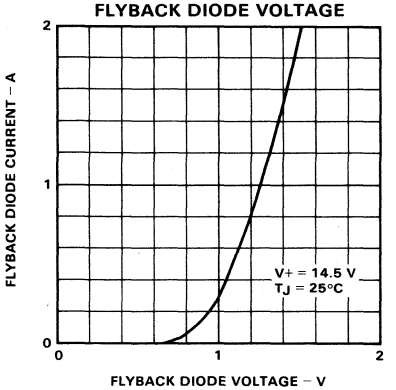
MOTOR DRIVE OUTPUT ON CURRENT AS A FUNCTION OF MOTOR DRIVE OUTPUT ON VOLTAGE



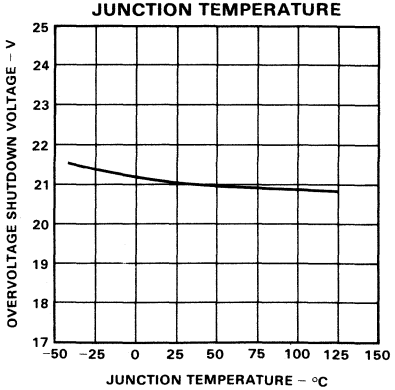
MOTOR DRIVE OUTPUT ON VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



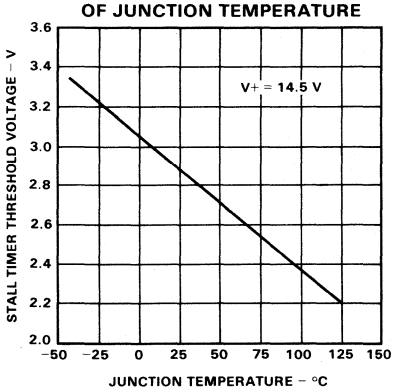
FLYBACK DIODE (D3) CURRENT AS A FUNCTION OF FLYBACK DIODE VOLTAGE



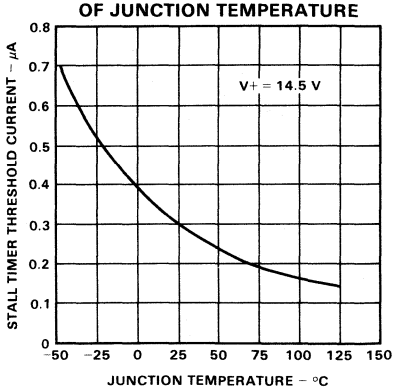
OVERVOLTAGE SHUTDOWN VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



STALL TIMER THRESHOLD VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

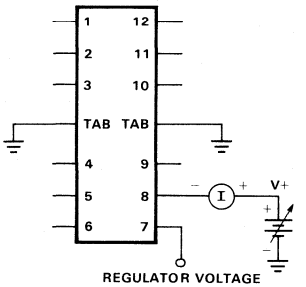


STALL TIMER THRESHOLD CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE

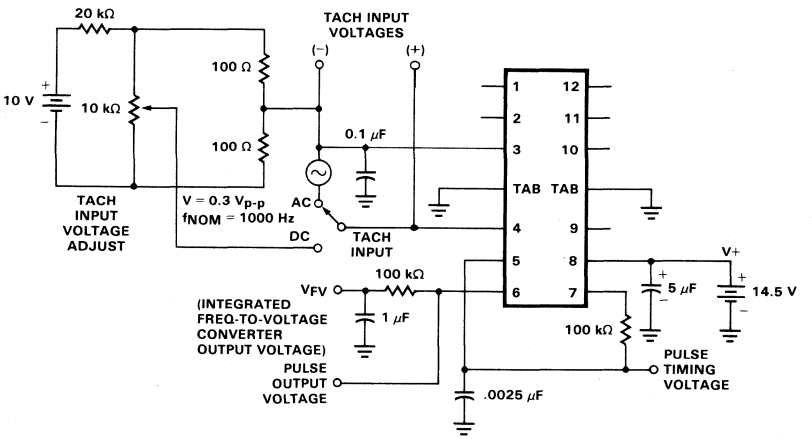


4

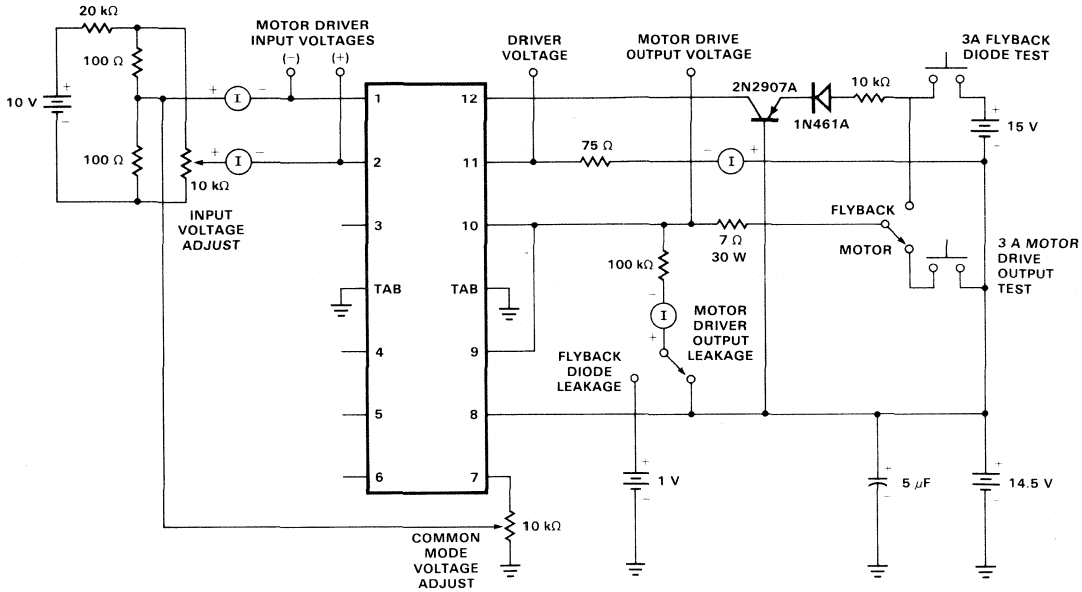
TEST CIRCUIT 1



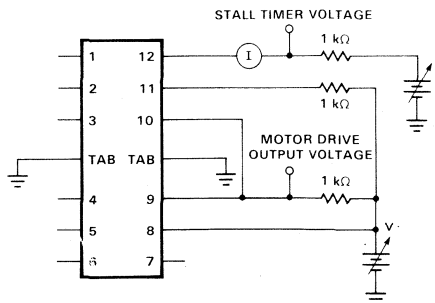
TEST CIRCUIT 2



TEST CIRCUIT 3



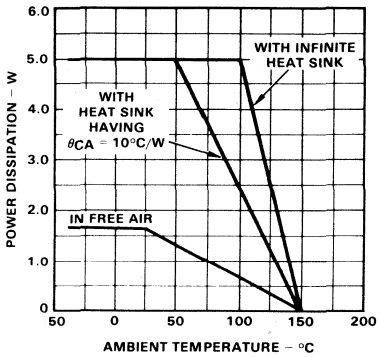
TEST CIRCUIT 4



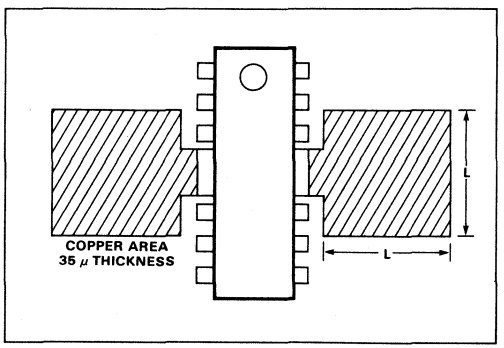
MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by soldering the tabs to an area of copper on the printed circuit board. During soldering the tabs temperature must not exceed 260°C and the soldering temperature time must not be longer than 10 seconds.

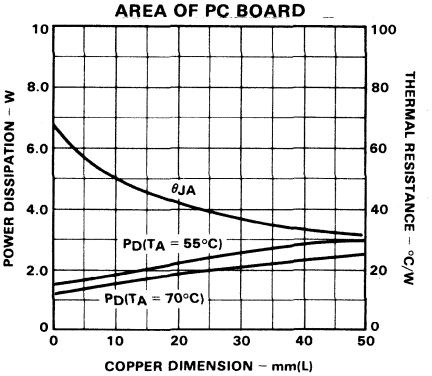
MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



PC BOARD



MAXIMUM POWER DISSIPATION AND TOTAL THERMAL RESISTANCE AS A FUNCTION OF COPPER AREA OF PC BOARD



μA7392

DC MOTOR SPEED CONTROL CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION—The μA7392 is designed for precision, closed-loop, motor speed control systems. It regulates the speed of capstan drive motors in automotive and portable tape players and is useful in a variety of industrial and military control applications, e.g., floppy disc drive systems and data cartridge drive systems. The device is constructed using the Fairchild Planar* epitaxial process.

The μA7392 compares actual motor speed to an externally presettable reference voltage. The motor speed is determined by frequency to voltage conversion of the input signal provided by the tachometer generator. The result of the comparison controls the duty cycle of the pulse width modulated switching motor drive output stage to close the system's negative feedback loop.

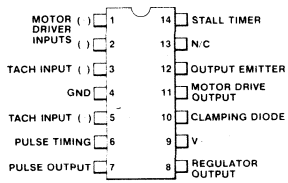
Thermal and over-voltage shutdown are included for self-protection, and a "stall-timer" feature allows the motor to be protected from burn-out during extended mechanical jams.

The μA7392 is a low current compliment to the μA7391 for those applications requiring less current and also to drive high current output stages for very high current applications.

- **PRECISION PERFORMANCE—FREQUENCY-TO-VOLTAGE CONVERSION STABILITY TYPICALLY 0.1% FOR V+ FROM 10 V TO 16 V; 0.3% FOR CASE TEMPERATURE FROM -40°C TO +85°C**
- **HIGH CURRENT PERFORMANCE—1.0 A STARTING SURGE CURRENT AND 300 mA RUNNING CURRENT TO A DC MOTOR**
- **WIDE RANGE TACHOMETER INPUT—100 mVp-p TO 1.0 Vp-p**
- **LOW EXTERNAL PARTS COUNT**
- **THERMAL SHUTDOWN, OVER-VOLTAGE AND STALL PROTECTION**
- **INTERNAL REGULATOR**
- **WIDE SUPPLY VOLTAGE RANGE—6.3 V TO 16 V**
- **EMITTER OF OUTPUT STAGE AVAILABLE FOR EASE IN DRIVING POWER TRANSISTOR OUTPUT STAGES**
- **CLAMPING DIODE AVAILABLE ON SEPARATE PIN**

CONNECTION DIAGRAM
14-PIN DIP
TOP VIEW

PACKAGE OUTLINE 6A, 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA7392	μA7392DM
μA7392C	μA7392DC
μA7392C	μA7392PC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+), V_9, V_{10}, V_{11}	24 V
Regulator Output Current, I_8	15 mA
Voltage Applied to Pin 6 (Tachometer Pulse Timing)	7 V
Voltage Applied Between Pins 3 and 5 (Tachometer Inputs)	±6 V
Continuous Current through Pins 11 and 12 Motor Drive Output ON	0.3 A
Repetitive Surge Current through Pins 11 and 12 (Motor Drive ON)	1.0 A
Repetitive Surge Current through Pins 10 and 11 (Motor Drive OFF)	0.3 A
Power Dissipation	Internally Limited
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range (μA7392)	-55°C to +125°C
Operating Temperature Range (μA7392C)	-40°C to +85°C
Pin Temperature (Soldering 10 s)	260°C

Planar is a patented Fairchild process

μA7392 and μA7392C

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, T_A = 25°C, unless otherwise noted

VOLTAGE REGULATOR SECTION: (TEST CIRCUIT 1)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	Excluding Current into Pin 11		7.5	10	mA
Regulator Output Voltage		4.5	5.0	5.5	V
Regulator Output Line Regulation (ΔV_8)	V+ from 10 V to 16 V V+ from 6.3 V to 16 V		6.0 12	20 50	mV mV
Regulator Output Load Regulation (ΔV_8)	I_8 from 10 mA to 0		40		mV

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, T_A = 25°C, unless otherwise noted

FREQUENCY TO VOLTAGE CONVERTER SECTION: (TEST CIRCUIT 2)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Tachometer (−) Input Bias Voltage			2.4		V
Tachometer (+) Input Bias Current	$V_5 = V_3$		1.0	10	μA
Tachometer input Positive Threshold	(V_5 − V_3)	10	25	50	mV_{pk}
Tachometer Input Hysteresis		20	50	100	mV_{pk-pk}
Pulse Timing ON Resistance	V_6 = 1 V		300	500	Ω
Pulse Timing Switch Threshold		45	50	55	$\%V_8$
Output Pulse Rise Time			0.3		μs
Output Pulse Fall Time			0.1		μs
Pulse Output LOW Saturation (V_7)			0.13	0.25	V
Pulse Output HIGH Saturation (V_8 − V_7)			0.12	0.2	V
Pulse Output HIGH Source Current	V_7 = 1 V	−340	−260	−180	μA
Frequency-to-Voltage Conversion Supply Voltage Stability (Note 1)	V_{FV} = 0.25 V_8 (Note 2) V+ from 10 V to 16 V		0.1		%
Frequency-to-Voltage Conversion Temperature Stability (Note 3)	V_{FV} = 0.25 V_8 (Note 2) T_A from −40°C to +85°C		0.3		%

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, T_A = 25°C, unless otherwise noted

MOTOR DRIVE SECTION: (TEST CIRCUIT 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage				±20	mV
Input Bias Current			0.1	10	μA
Common Mode Range		0.8		2.5	V
Motor Drive Output Saturation	I_{11} = 300mA		1.3	1.6	V
Motor Drive Output Leakage	$V_{11} = V_{10}$ = 16 V			5	μA
Flyback Diode Leakage	V_{10} = 16 V, V_{11} = 0 V			30	μA
Flyback Diode Clamp Voltage	I_{11} = 300mA Motor Drive Output Off		1.1	1.3	V

μA7392, μA7392C

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, T_A = 25°C unless otherwise noted

PROTECTIVE CIRCUITS: (TEST CIRCUIT 4)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Junction Temperature	Note 4		160		°C
Overvoltage Shutdown	Note 4	18	21	24	V
Stall Timer Threshold Voltage	Note 5	2.5	2.9	3.5	V
Stall Timer Threshold Current	Note 5		0.3	3.0	μA

μA7392 ONLY

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted

VOLTAGE REGULATOR SECTION: (TEST CIRCUIT 1)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	Excluding Current into Pin 11		7.5	12	mA
Regulator Output Voltage		4.5	5.0	6.0	V
Regulator Output Line Regulation (ΔV_8)	V+ from 10 V to 16 V V+ from 6.3 V to 16 V		6.0 12	20 50	mV mV
Regulator Output Load Regulation (ΔV_8)	I_8 from 10 mA to 0		40	100	mV

FREQUENCY TO VOLTAGE CONVERTER SECTION: (TEST CIRCUIT 2)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Tachometer (−) Input Bias Voltage			2.4		V
Tachometer (+) Input Bias Current	$V_5 = V_3$		1.0	15	μA
Tachometer Input Positive Threshold	($V_5 - V_3$)	10	25	50	mV_{pk}
Tachometer Input Hysteresis		20	50	100	mV_{p-p}
Pulse Timing ON Resistance	V_6 = 1 V		300	670	Ω
Pulse Timing Switch Threshold		45	50	55	$\%V_8$
Output Pulse Rise Time			0.3		μs
Pulse Fall Time			0.1		μs
Pulse Output LOW Saturation (V_7)			0.13	0.25	V
Pulse Output HIGH Saturation ($V_8 - V_7$)			0.12	0.2	V
Pulse Output HIGH Source Current	V_7 = 1 V	−370	−260	−150	μA
Frequency-to-Voltage Conversion Supply Voltage Stability (Note 1)	$F_{FV} = 0.25\ V_8$ (Note 2) V+ from 10 V to 16 V		0.1		%
Frequency-to-Voltage Conversion Temperature Stability (Note 3)	$V_{FV} = 0.25\ V_8$ (Note 2) T_A from −40°C to +85°C		0.3		%

4

μA7392 ONLY

ELECTRICAL CHARACTERISTICS Cont. : V+ = 14.5 V, -55°C ≥ TA ≤ +125°C, unless otherwise noted.

MOTOR DRIVE SECTION: (TEST CIRCUIT 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage				±30	mV
Input Bias Current			0.1	10	μA
Common Mode Range		0.8		2.5	V
Motor Drive Output Saturation	I_{11} = 300mA		1.3	1.6	V
Motor Drive Output Leakage	$V_{11} = V_{10}$ = 16 V			10	μA
Flyback Diode Leakage	V_{10} = 16 V, V_{11} = 0 V			30	μA
Flyback Diode Clamp Voltage	I_{11} = 300mA Motor Drive Output Off		1.1	1.3	V

PROTECTIVE CIRCUITS: (TEST CIRCUIT 4)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Junction Temperature	Note 4		160		°C
Overvoltage Shutdown	Note 4	18	21	24	V
Stall Timer Threshold Voltage	Note 5	1.8	2.9	4.0	V
Stall Timer Threshold Current	Note 5		0.3	4.0	μA

NOTES:

1. Frequency-to-Voltage Conversion, Supply Voltage Stability is defined as:

$$\left[\frac{V_{FV}(16\ V)}{V_8(16\ V)}\right] - \left[\frac{V_{FV}(10\ V)}{V_8(10\ V)}\right] \div \left[\frac{V_{FV}(14.5\ V)}{V_8(14.5\ V)}\right] \times 100\%$$

2. V_{FV} is the integrated dc output voltage from the pulse generator (Pin 7)
3. Frequency-to-Voltage Conversion Temperature Stability is defined as:

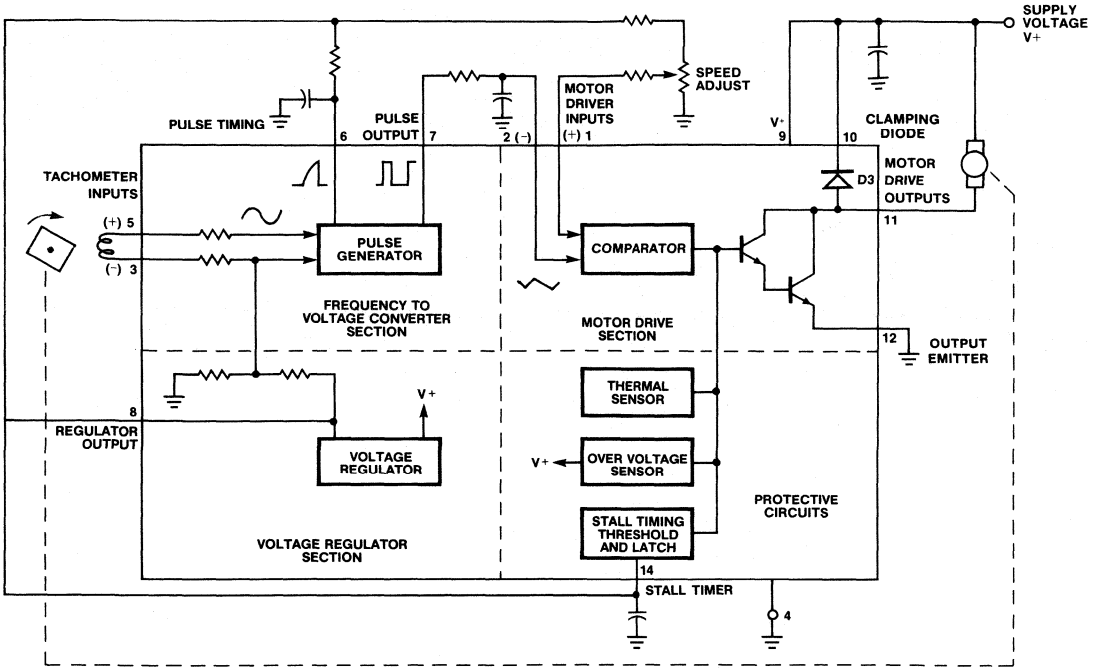
$$\left[\frac{V_{FV}(85°\ C)}{V_8(85°\ C)}\right] - \left[\frac{V_{FV}(-40°\ C)}{V_8(-40°\ C)}\right] \div \left[\frac{V_{FV}(25°\ C)}{V_8(25°\ C)}\right] \times 100\%$$

4. "Motor Drive" circuitry is disabled when these limits are exceeded. If the condition continues for the duration set by the external stall timer components, the circuit is latched off until reset by temporarily opening the power supply input line.
5. If stall timer protection is not required, Pin 14 should be grounded.

THERMAL DATA

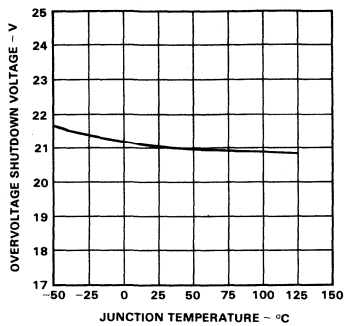
	TYP	MAX	
θ_{JA} THERMAL RESISTANCE, JUNCTION TO AMBIENT			
PLASTIC (9A)	70	80	°C/W
CERAMIC (6A)	100	120	°C/W

BLOCK DIAGRAM

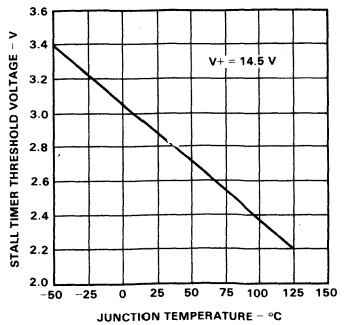


TYPICAL PERFORMANCE CURVES

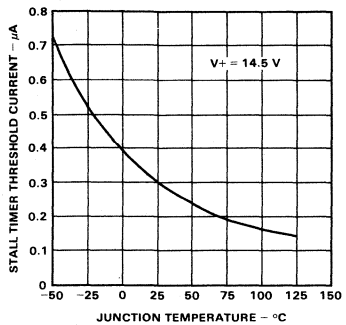
OVERVOLTAGE SHUTDOWN VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



STALL TIMER THRESHOLD VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

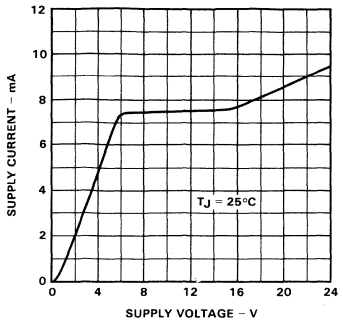


STALL TIMER THRESHOLD CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE

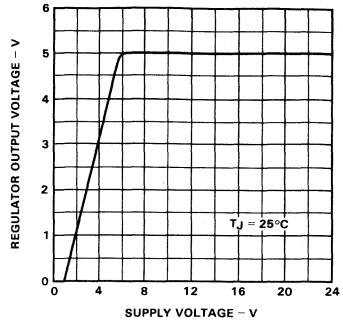


TYPICAL PERFORMANCE CURVES (Cont'd.)

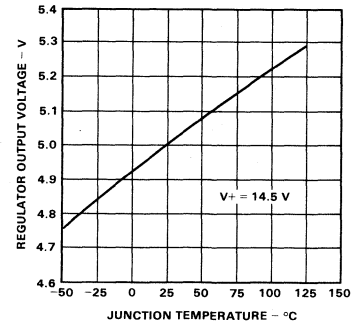
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



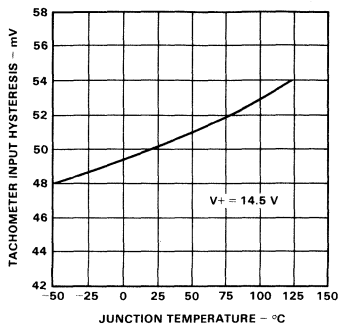
REGULATOR OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



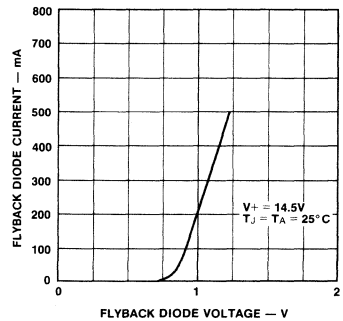
REGULATOR OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



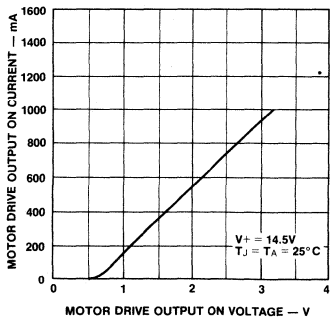
TACHOMETER INPUT HYSTERESIS AS A FUNCTION OF JUNCTION TEMPERATURE



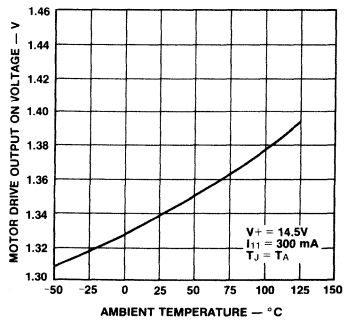
FLYBACK DIODE (D3) CURRENT AS A FUNCTION OF FLYBACK DIODE VOLTAGE



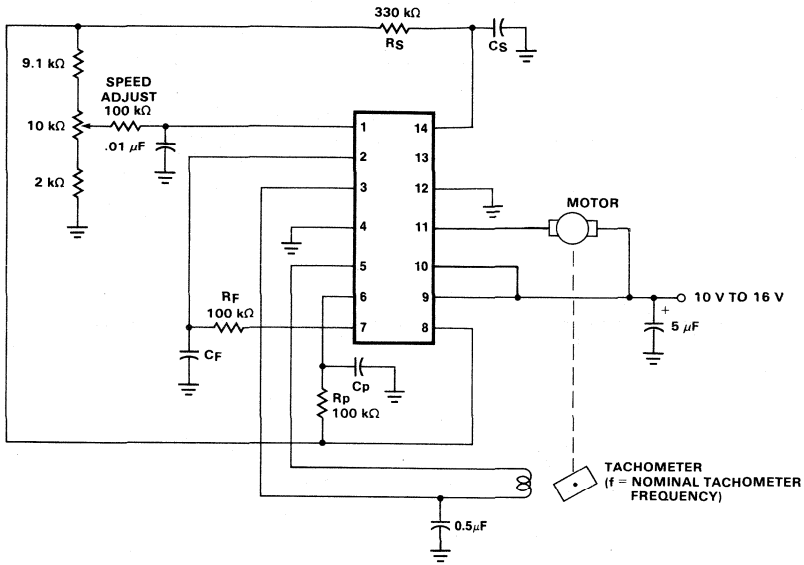
MOTOR DRIVE OUTPUT ON CURRENT AS A FUNCTION OF MOTOR DRIVE OUTPUT ON VOLTAGE



MOTOR DRIVE OUTPUT ON VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL APPLICATION USING MAGNETIC TACHOMETER



TYPICAL COMPONENT VALUES:

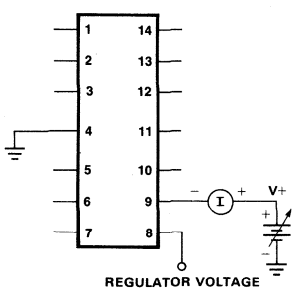
$Cp = \frac{}{4\ Rpf}$

Cf = 10 Cp to 1000 Cp depending on system requirements

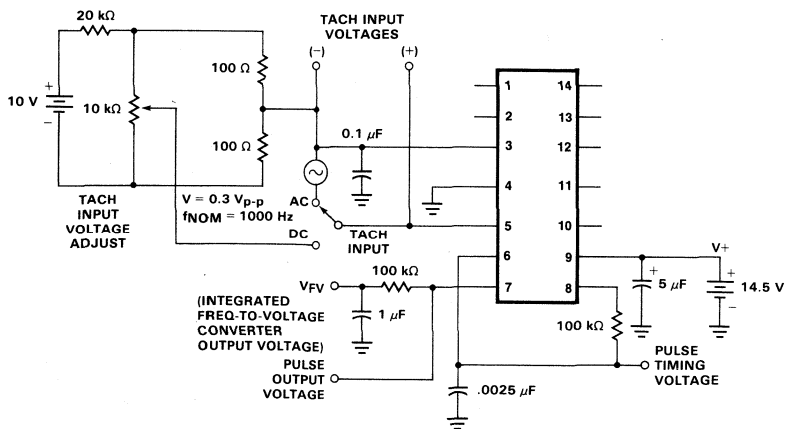
$Cs = \frac{2 \times \text{stall time-out}}{RS}$

$R_{Motor} \geq 5\ \Omega$

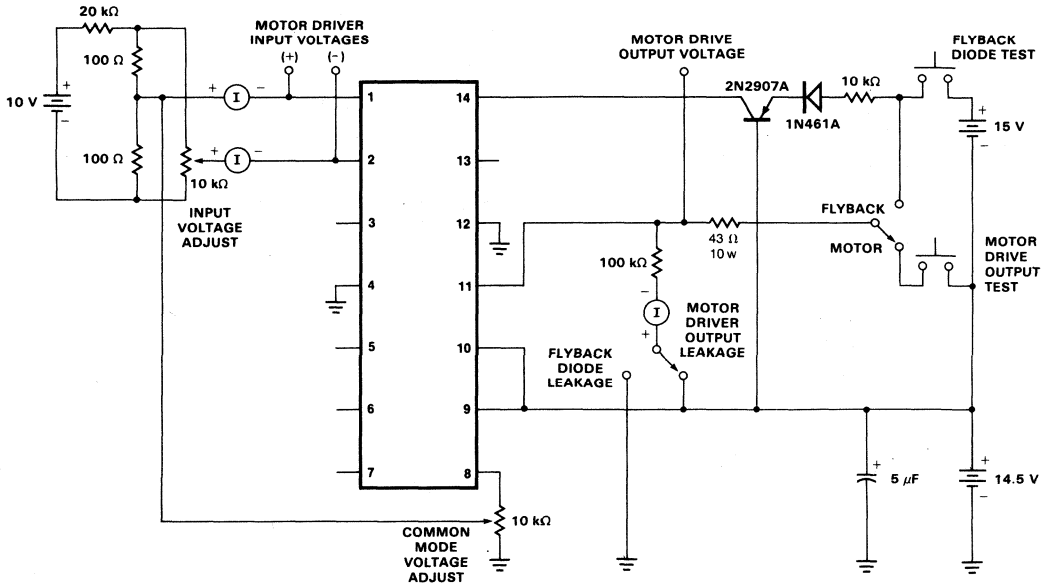
TEST CIRCUIT 1



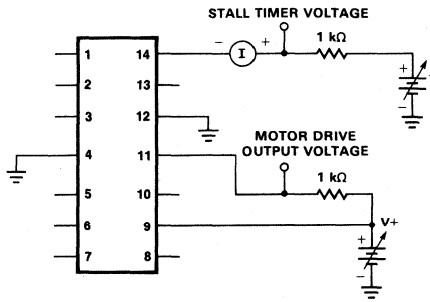
TEST CIRCUIT 2



TEST CIRCUIT 3



TEST CIRCUIT 4



TAA630S

PAL CHROMA DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

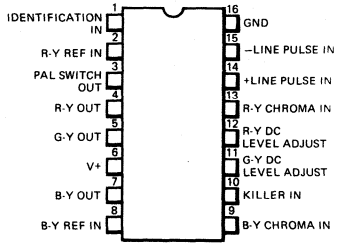
GENERAL DESCRIPTION – The TAA630S is a synchronous demodulator for direct drive of color video output stages. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The TAA630S is designed for use in color television receivers operating on the Phase Alternate Line (PAL) system. This circuit consists of two synchronous demodulators, a decoding matrix, a PAL switch with internal multivibrator and a color killer switch.

- **DOUBLE BALANCED SYNCHRONOUS DEMODULATOR**
- **INTERNAL DECODING MATRIX**
- **EMITTER FOLLOWER OUTPUTS**
- **INTERNAL PAL SWITCH**
- **INTERNAL COLOR KILLER**
- **PROVISION FOR OUTPUT DC LEVEL MATCHING**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	13.2 V
Internal Power Dissipation (Note 1)	550 mW
Color Difference Output Currents	5.0 mA
Voltage on Identification Input	5.0 V
Current Into Identification Input	1.0 mA
Operating Temperature Range	−20°C to +60°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B

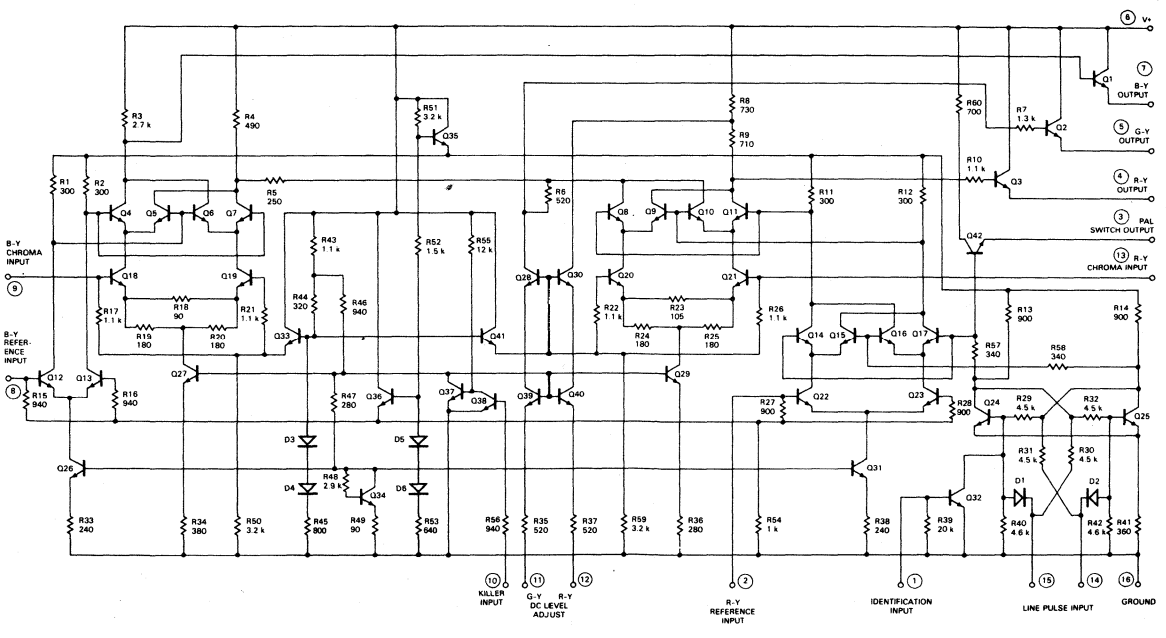


ORDER INFORMATION

TYPE	PART NO.
630S	TAA630S
(630T)	(TAA630T)†

†Not recommended for new designs.

EQUIVALENT CIRCUIT



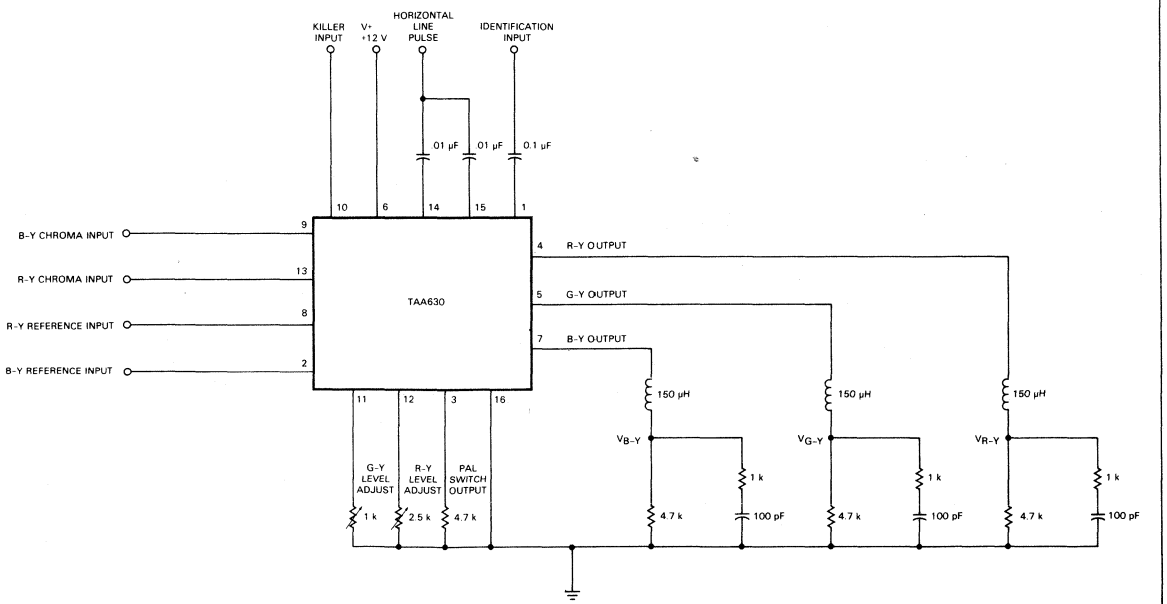
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_+ = 12V$, See Test Circuit, unless otherwise specified.

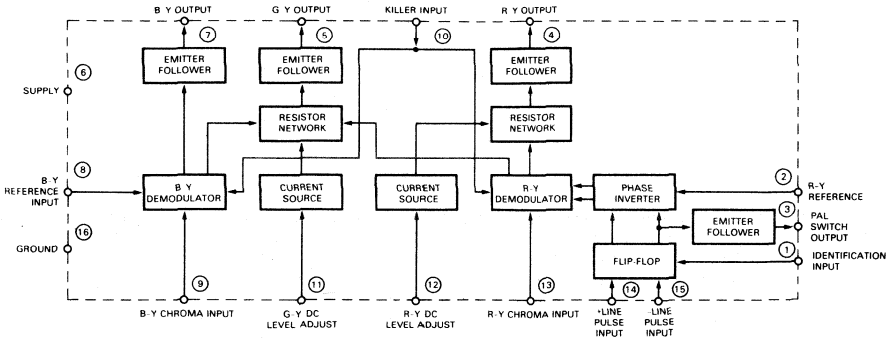
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_6)			32		mA
Color Difference Gain	$V_9 = V_{13} = 50$ mV p-p				
R-Y Channel	f = 4.4 MHz		7.0		
B-Y Channel/R-Y Channel			1.78		
G-Y Channel			Note 2		
Maximum Color Difference Output Voltage	Notes 3, 4				
R-Y Output (V_4 p-p)			3.2		Vp-p
B-Y Output (V_7 p-p)			4.0		Vp-p
G-Y Output (V_5 p-p)			1.8		Vp-p
Color Difference DC Output Voltage					
R-Y Output (V_4)	Note 5		Adjustable to V_7		
B-Y Output (V_7)			7.4		V
G-Y Output (V_5)	Note 5		Adjustable to V_7		
Input Resistance of Chroma Inputs (R_9, R_{13})	$V_9 = V_{13} = 20$ mV RMS	800			Ω
Input Capacitance of Chroma Inputs (C_9, C_{13})	f = 4.4 MHz (sinusoidal)			10	pF
Output Resistance at Color Difference Terminals (R_4, R_5, R_7)				100	Ω
Input Resistance of Reference Inputs (R_2, R_8)	Note 7	660		1250	Ω
Peak-to-Peak PAL Switch Output Voltage (V_3 p-p)	Note 6		2.5		Vp-p
Activation Threshold Voltage (V_1)	Identification circuit is active	0.75			V
Activation Threshold Current (I_1)		80			μA
Deactivation Threshold Voltage (V_1)	Identification circuit is inactive			0.4	V
DC Voltage at Color Killer Input (V_{10}):					
Color On		0.9			V
Color Off				0.3	V

NOTES:
1. 16 V is permissable during warm-up.
2. G-Y Output is typically equal to −0.51 (R-Y) −0.19 (B-Y).
3. Gain is equal to 0.7 of small signal gain.
4. Reference input (V_2 p-p and V_8 p-p) range is 0.5 V to 2.0 V.
5. To be adjusted with a variable voltage ($V \leq 1.2$ V) or with resistors connected between pin 11 and ground for G-Y and pin 12 and ground for R-Y.
6. f_{out} = 0.5 x Line Pulse Frequency, $V_{14} = V_{15}$ = −2.5 V to −5.0 V (Peak), PAL identification signal required, V_1 = 2.0 to 6.0 V p/p.
7. $V_2 = V_8$ = 400 mV RMS, f = 4.4 MHz (sinusoidal).

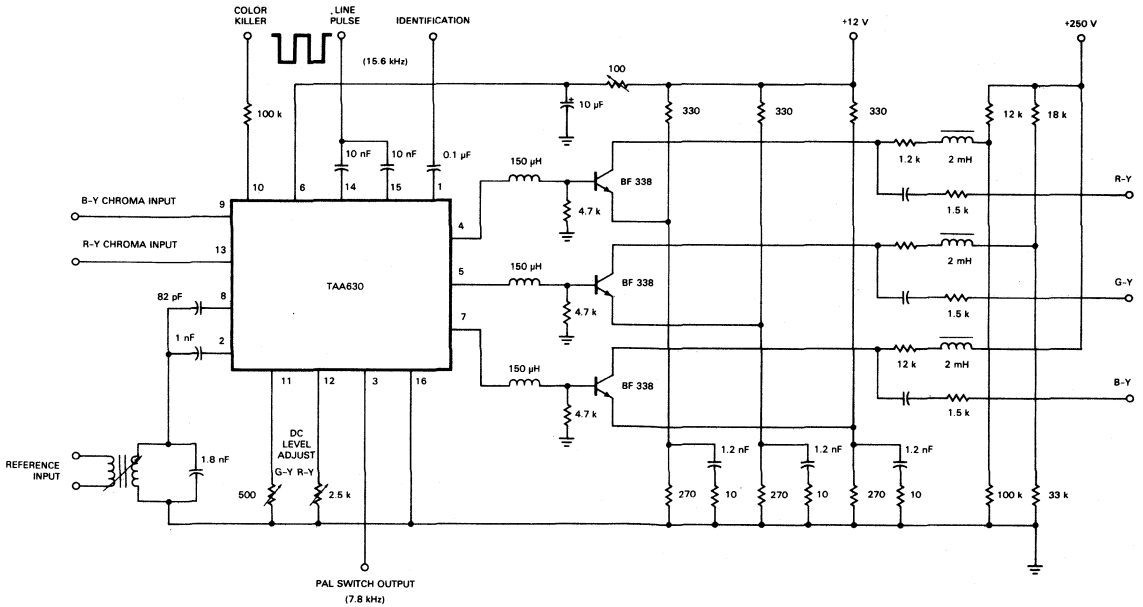
TEST CIRCUIT



BLOCK DIAGRAM



TYPICAL APPLICATION



TBA510

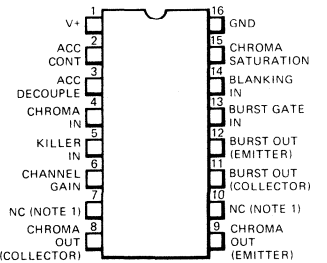
CHROMA PROCESSING CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA510 is a monolithic integrated circuit designed to perform the chrominance amplifier function for television receivers. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. A dc chroma gain control, which can be ganged to the receiver contrast control, is provided. Also incorporated is a variable gain automatic color control (ACC) stage, chroma blanking, burst gating, burst output stage. Two single output transistors provide burst and chroma output.

- **DC CHROMA CONTROL**
- **PAL DELAY LINE DRIVER**
- **ACC AMPLIFIER**
- **COLOR KILLER**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

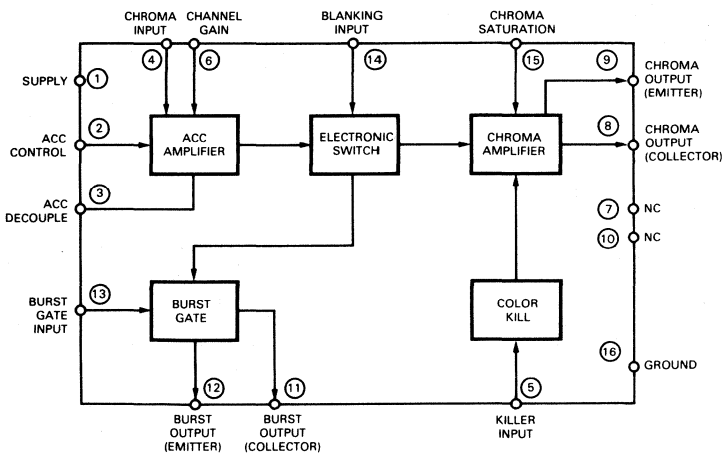
TYPE	PART NO.
510	TBA510
(510Q)	(TBA510Q)†

†Not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

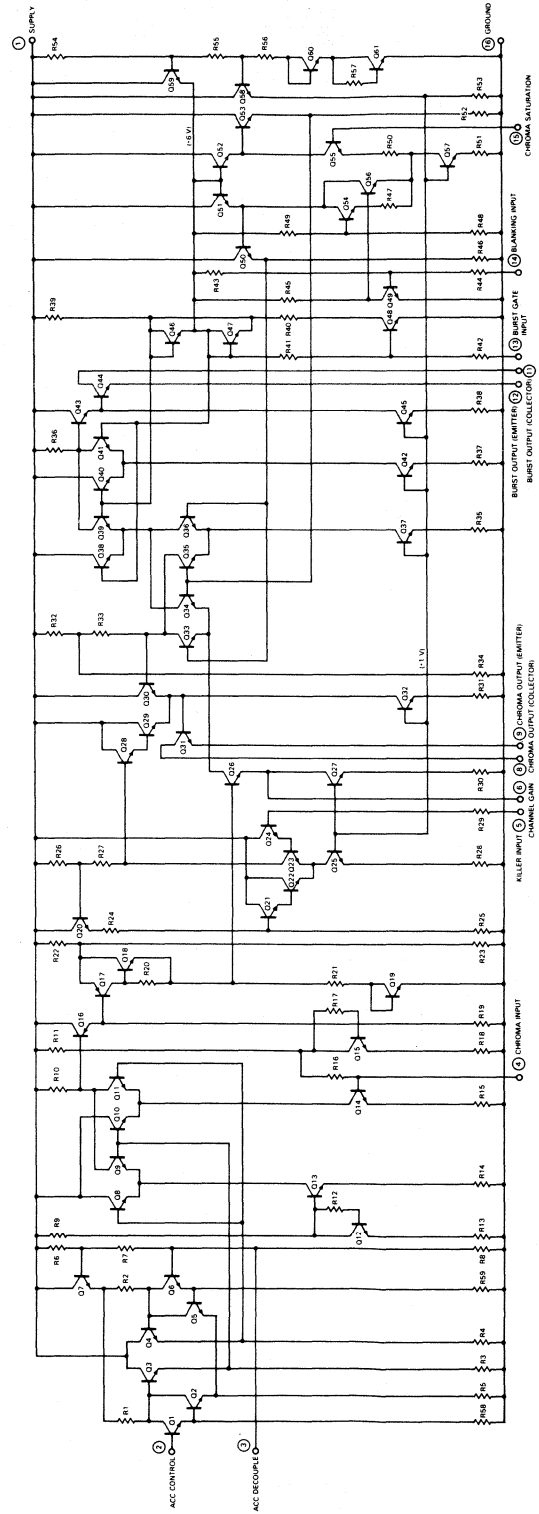
Supply Voltage	13.2 V
Internal Power Dissipation	550 mW
Current into Chroma Delay Line Driver (Collector)	20 mA
Current into Color Burst Output (Collector)	20 mA
Current out of Color Burst Output (Emitter)	20 mA
Current out of Chroma Delay Line Driver (Emitter)	20 mA
Operating Temperature Range	−20°C to +60°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT

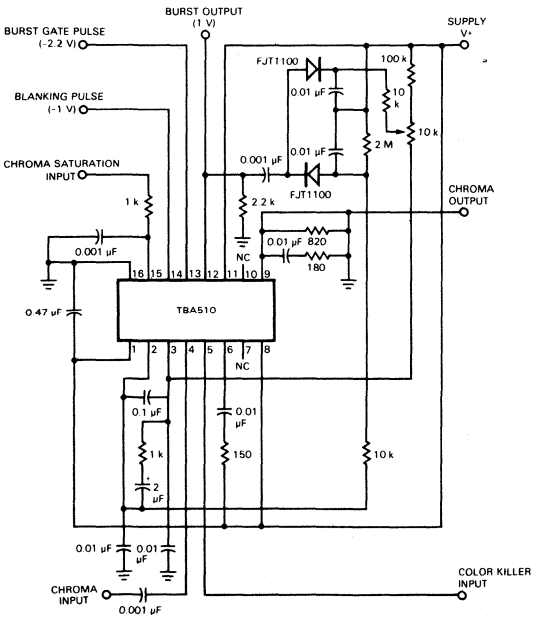


○ = Pin Numbers

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_+ = 12V$, See Test Circuit, unless otherwise specified.

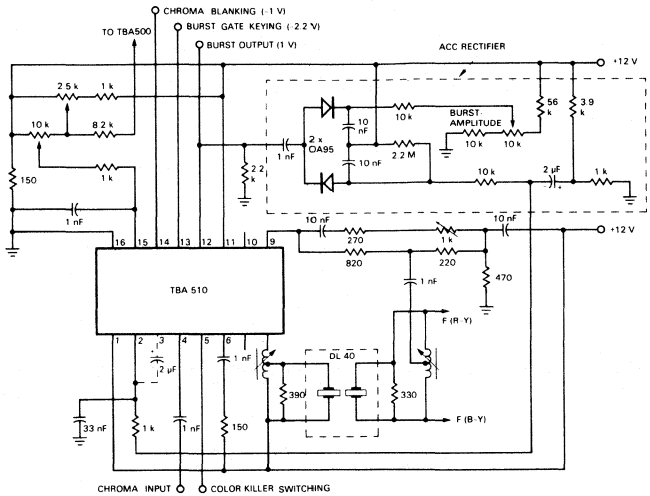
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Chroma Input (pin 4)					
Peak-to-Peak Signal at Chroma Input (V_{4p-p})		15	150	300	mV_{p-p}
Input Impedance of Chroma Signal (Z_4)			3.0		kΩ
Burst Output (pin 11 and 12)					
DC Voltage at Color Burst Output (V_{12})			8.0		V
Peak-to-Peak Signal at Color Burst Output (V_{12p-p})	(Note 2)		1.0		V_{p-p}
Collector Current of Color Burst Output (I_{11})			4.0		mA
Chroma Output (pin 8 and 9)					
DC Voltage at Chroma Output (V_9)			7.0		V
Peak-to-Peak Signal at Chroma Output (V_{9p-p})	(Note 3)		1.0		V_{p-p}
Range of Contrast and Saturation Control		−30		+6.0	dB
Collector Current at Chroma Output (I_8)			5.0		mA
ACC Input (pin 2)					
ACC Input Voltage (V_2) for Maximum Gain (Note 4)			2.5		V
Input Impedance of ACC Control (Z_2)		50			kΩ
Chroma Saturation Control Input (pin 15)					
Control Voltage Range (V_{15}) (Note 4)		1.5		4.5	V
Input Impedance (Z_{15})		50			kΩ
Chroma Blanking Input (pin 14)					
Switching Level Range (V_{14})		−5.0		−1.0	V
Input Impedance (Z_{14})			2.0		kΩ
Burst Gate Input (pin 13)					
Switching Level Range (V_{13})		−5.0		−2.2	V
Input Impedance (Z_{13})			4.0		kΩ
Color Killer Input (pin 5)					
Input Voltage (V_5) for:					
Color on		2.5		4.0	V
Color off		0		1.8	V
Signal Suppression at Color Off		50			dB
Input Impedance (Z_5)		100			kΩ

TEST CIRCUIT



NOTES:
1. NC — no connection (not to be used as a tie point).
2. Color burst output kept constant by ACC circuit.
3. Chroma output (emitter) at nominal saturation and maximum contrast.
4. Gain control characteristic positive.

APPLICATION INFORMATION



The function is quoted against the corresponding pin number.

1. **Positive 12 V supply**
2. **A.C.C. control potential input**
   The potential required at pin 2 for maximum gain is about 2.5 V; gain reduction occurs when this potential is reduced; Zin > 50 kΩ.
3. **A.C.C. bias ripple compensation**
   The internal A.C.C. circuit consists of differential pair. The "cold" side is established internally at +2.5 V and is brought out on pin 3. This enables a decoupling capacitor to be connected and returned to the point which secures the lowest supply line ripple amplitude injection into the A.C.C. loop.
4. **Chroma signal input**
   The allowable input voltage range is from 15 mV to 300 mV peak-to-peak with a color bar signal. The input impedance is greater than 2 kΩ.
5. **Color killer switching input**
   The input impedance is greater than 50 kΩ. Color "on" 2.5 to 4 V; color "off" 0 to 1.8 V. The chroma signal suppression when killed is greater than 50 dB.
6. **Emitter decoupling network**
   The series network decouples an emitter of an amplifier stage in the chroma channel. The value of resistance influences the chroma channel gain.
7. **No connection**
   Not to be used as a tie point. It is recommended that pins 7 and 10 be grounded.
8. **Delay line driver (collector)**
   Supplies the chroma signal drive to the delay line driver transformer, the "cold" end of which is connected to +12 V. The maximum permitted voltage excursion at this pin is 20 V peak. Maximum current, 12 mA peak.
9. **Delay line driver (emitter)**
   Supplies the chroma to the network which provides the non-delayed signal to the delay line output transformer. The emitter is established internally at a potential of 6.8 ± 1.0 V and the external network, which must incorporate a resistive dc path to ground, must not demand more than 20 mA peak current.
10. **No connection**
    Not to be used as a tie point. (See pin 7.)
11. **Color burst output (collector)**
    If a low impedance color burst is required (from the emitter of the color burst output, pin 12) pin 11 will be connected to the +12 V supply. The maximum voltage and current excursions permitted on pin 11 are 20 V peak and 20 mA peak.
12. **Color burst output (emitter)**
    An external load resistor of 2.0 kΩ is required connected to ground and dc potential of 7.7 ± 1.0 V is established on pin 12 due to the internal circuitry. The burst output voltage is 1.0 V peak-to-peak.
13. **Burst gate gating pulse**
    The horizontal flyback pulse can be used as a source of gating waveform. A negative-going pulse of not greater than 5.0 V amplitude is necessary, the input impedance is 4.0 kΩ and the switching level is between −2.2 V and −5.0 V.
14. **Chroma blanking pulse input**
    A negative going horizontal flyback pulse can be used here. Its amplitude should not exceed −5.0 V. The input impedance at this pin is 2.0 kΩ and the switching level is about −1.0 V. During scan time, the dc voltage on this pin should not be negative.
15. **Chroma saturation control**
    The dc control voltage range required is from 1.5 to 4.5 V (highest gain at 4.5 V). The input impedance is > 50 kΩ and a control range from +6.0 to −30 dB is given.
16. **Ground**

TBA520

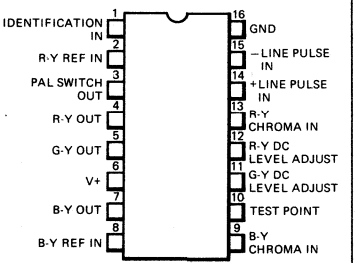
PAL TV CHROMA DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA520 is a synchronous demodulator for direct drive of color video output stages. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The TBA520 is designed for use in color television receivers, operating on the Phase Alternate Line (PAL) system. This circuit consists of two synchronous demodulators, a decoding matrix and a PAL switch with internal multivibrator.

- **DOUBLE BALANCED SYNCHRONOUS DEMODULATOR**
- **INTERNAL DECODING MATRIX**
- **INTERNAL PAL SWITCH**
- **PROVISION FOR OUTPUT DC LEVEL MATCHING**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

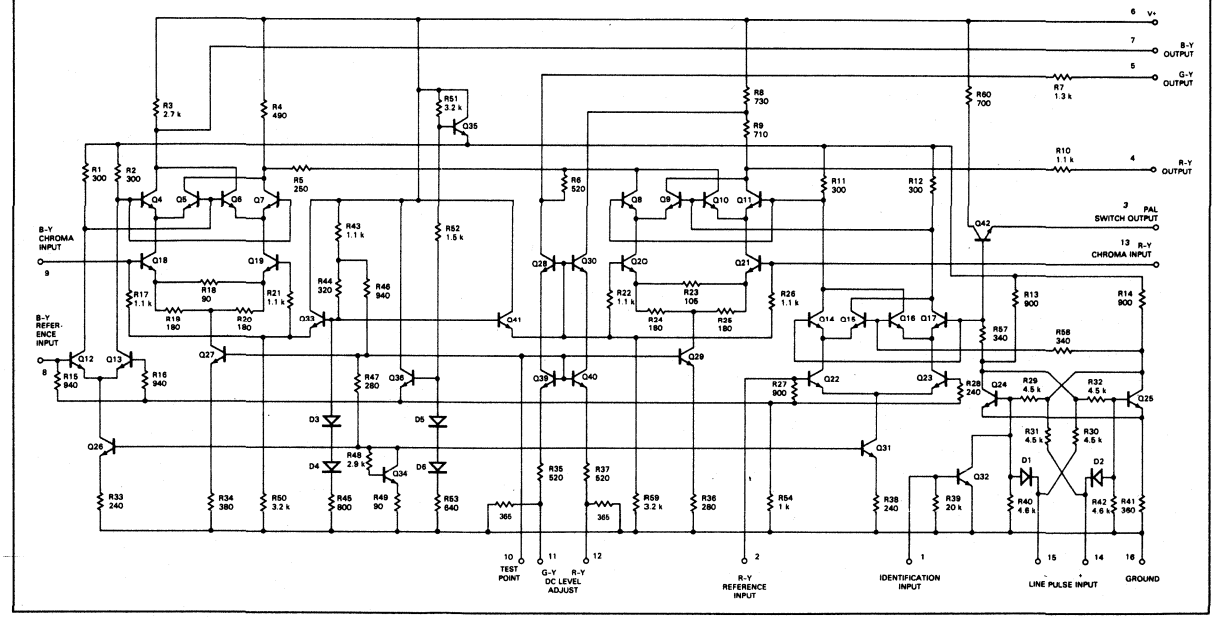
TYPE	PART NO.
520	TBA520
(520 Q)	(TBA520 Q)†

†Not recommended for new design.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	13.2 V
Internal Power Dissipation	550 mW
Voltage on Identification Input	5.0 V
Current into Identification Input	1.0 mA
Operating Temperature Range	–20°C to +60°C
Storage Temperature Range	–55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



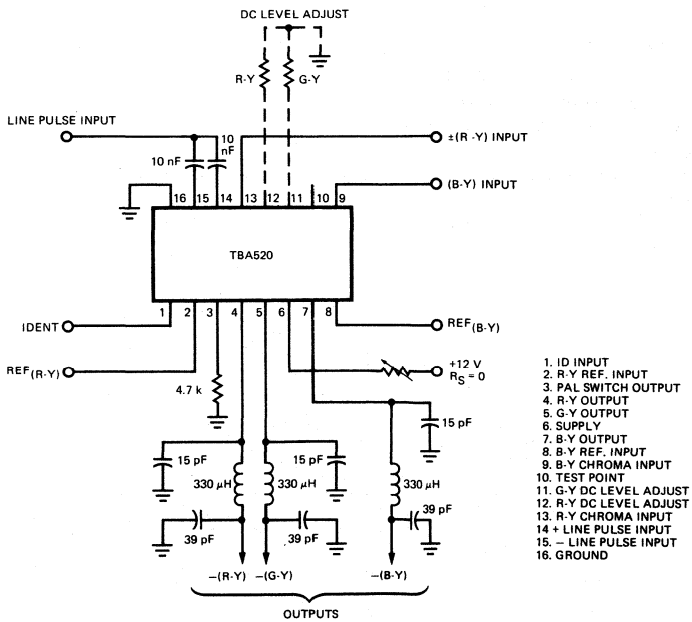
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_+ = 12V$, See Test Circuit, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_6)			32		mA
Color Difference Gain					
R-Y Channel	$V_9 = V_{13} = 50\ mV_{pk\text{-}pk}$, f = 4.4 MHz		7.0		V/V
B-Y Channel			12.5		V/V
G-Y Channel			(Note 1)		
Maximum Color Difference Output Voltage (Notes 2,3)					
R-Y Output ($V_{4\ pk\text{-}pk}$)	(Notes 2,3)		3.2		$V_{pk\text{-}pk}$
B-Y Output ($V_{7\ pk\text{-}pk}$)			4.0		$V_{pk\text{-}pk}$
G-Y Output ($V_{5\ pk\text{-}pk}$)			1.8		$V_{pk\text{-}pk}$
Color Difference dc Output Voltage					
R-Y Output (V_4)			7.9		V
B-Y Output (V_7)			7.9		V
G-Y Output (V_5)			7.9		V
Input Resistance of Chroma Inputs (R9, R13)	$V_9 = V_{13} = 20\ mV_{rms}$ (Sinusoidal)	800			Ω
Input Capacitance of Chroma Inputs (C9, C13)	f = 4.4 MHz			10	pF
Output Resistance at Color Difference Terminals (R4, R5, R7)			2.7		kΩ
Input Resistance of Reference Inputs (R2, R8)			1.0		kΩ
Peak-to-Peak PAL Switch Output Voltage ($V_{3\ pk\text{-}pk}$)	(Note 4)		2.5		$V_{pk\text{-}pk}$
Activation Threshold Voltage (V_1)	Identification Circuit is Active	0.75			V
Activation Threshold Current (I_1)		80			μA
Deactivation Threshold Voltage (V_1)	Identification Circuit is Inactive			0.4	V

NOTES:
1. G-Y output is typically equal to −0.51 (R-Y) −0.19 (B-Y).
2. Gain is equal to 0.7 of small signal gain.
3. Reference input ($V_{2pk\text{-}pk}$ and $V_{8pk\text{-}pk}$) range is 0.5 V to 2.0 V.
4. f_{out} = 0.5 x line pulse frequency; $V_{14} = V_{15}$ = −3.0 V to −4.5 V (peak).

TEST CIRCUIT



APPLICATION INFORMATION

The function is quoted against the corresponding pin numbers.

1. **Identification bias**
   The input current required to stop the flip-flop, "Ident on": $I_{on} \geq 80\,\mu A$. For "Ident off": $V_{off} = -5.0$ to $+0.4$ V.
2. **R-Y subcarrier reference input**
   An 1.0 V peak-to-peak signal is required via a dc blocking capacitor. Under no circumstances should this signal be less than 0.5 V peak-to-peak. The input resistance at this pin is typically 1 kΩ.
3. **PAL square wave output** The amplitude is 2.5 V peak-to-peak from an emitter follower.
4. **R-Y signal output** (G-Y at pin 5 and B-Y at pin 7)
   No external dc load needed except that direct connection must be made via the low pass filter to the R G B matrix of the TBA530.
   The signals produced are in the following ratios:

$$V_{B-Y} = 1.3\ V_{R-Y}$$
$$\text{(a)}\quad V_{G-Y} = 0.76\ V_{R-Y}$$
$$\text{(b)}\quad V_{G-Y} = 0.26\ V_{R-Y}$$

   Condition (a) refers to (B-Y) + (R-Y) addition in the G-Y matrix. Condition (b) refers to the phase reversed (R-Y) input signal where (G-Y) is obtained by subtraction.

   The dc levels should each be adjusted, starting with the (B-Y) to +7.5 V at nominal supply voltage.

   The maximum peak-to-peak voltages for the condition $m \geq 0.7$ (m = ratio of minimum to maximum differential gains) are:

$$V_{R-Y(pk-pk)} = 3.2\ V$$
$$V_{G-Y(pk-pk)} = 1.8\ V$$
$$V_{B-Y(pk-pk)} = 4.0\ V$$

   The output impedance for each signal is 2.7 kΩ.

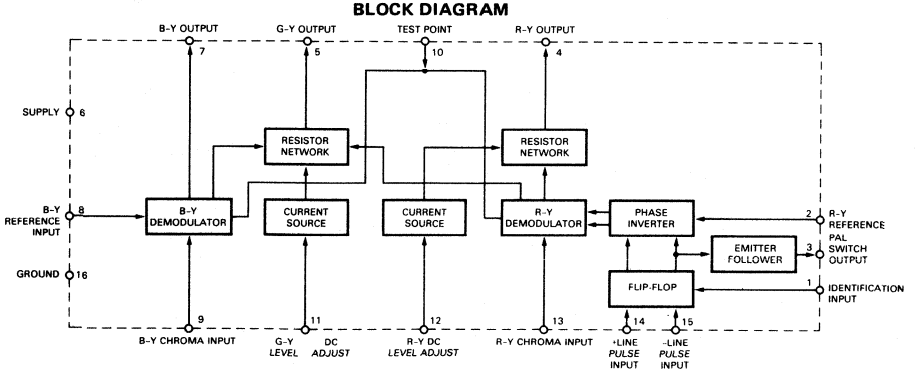
   The drifts in dc levels of the color difference output signals for a change in ambient temperature of 40°C (after equilibrium is reached from switch-on) are typically:

Absolute shift	−50 to +50 mV
V_{R-Y} relative to V_{B-Y}	−20 to +20 mV
V_{G-Y} realtive to V_{B-Y}	−20 to +20 mV
V_{R-Y} relative to V_{G-Y}	−20 to +20 mV

   The changes in dc level with supply voltage are approximately linear and track together.

   The −3.0 dB bandwidth of the color difference signals is 1.5 MHz.
5. **G-Y signal output** (see pin 4)
6. **Positive supply**
   Also dc level setting for B-Y output (pin 7). The maximum allowable voltage on this pin is 13.2 V. The minimum supply voltage to insure setting the B-Y output dc level correctly (+7.5 V) is 11.6 V (in such case R_S would be set to zero).
7. **B-Y signal output** (see pin 4)
8. **B-Y subcarrier reference input** The requirements here are identical with those for pin 2.
9. **Chrominance B-Y input signal**
   An input signal up to 360 mV peak-to-peak (color bars) is advisable. For driving the TBA530 an input signal of 160 mV is required.
10. **Internally connected** No external connection should be made.
11. **DC level setting for G-Y output signal** (circuit diagram on page 2).
12. **DC level setting for R-Y output** (see circuit diagram on page 2).
13. **Chrominance R-Y input signal**
    An input signal up to 500 mV peak-to-peak (color bars) is advisable. The input impedance is the same as for pin 9.
14. **Line pulse input** (flip-flop synchronizing)
    A 4.0 V peak negative going line flyback pulse should be applied via separate 10 nF capacitors to pins 14 and 15. Pulse amplitude to lie between 3.0 V and 4.5 V peak-to-peak.
15. **Line pulse input** (see pin 14).
16. **Ground.**

BLOCK DIAGRAM



TBA530

RGB MATRIX PREAMPLIFIER

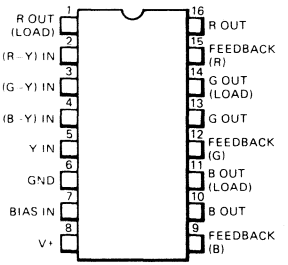
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The TBA530 is an integrated circuit for color T.V. receivers incorporating a matrix preamplifier for RGB cathode or grid drive of the picture tube without clamping circuits. The chip layout has been designed to insure tight thermal coupling between all the transistors in each channel to minimize and equalize thermal drifts between channels.

This device is constructed on a single silicon chip using the Fairchild Planar* epitaxial process and is designed to be driven from the TBA520 or TBA990 synchronous demodulators.

- **THREE MATCHED CHANNELS FOR MATRIXING**
- **MATCHED FREQUENCY RESPONSE**
- **MATCHED TEMPERATURE STABILITY**
- **DIRECT DRIVE OF RGB OUTPUT TRANSISTORS WHEN USING TBA520 OR TBA990**
- **RGB DRIVE WITH OR WITHOUT CLAMPING**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

TYPE	PART NO.
530	TBA530
530Q	TBA530Q†

†Not Recommended for New Designs.

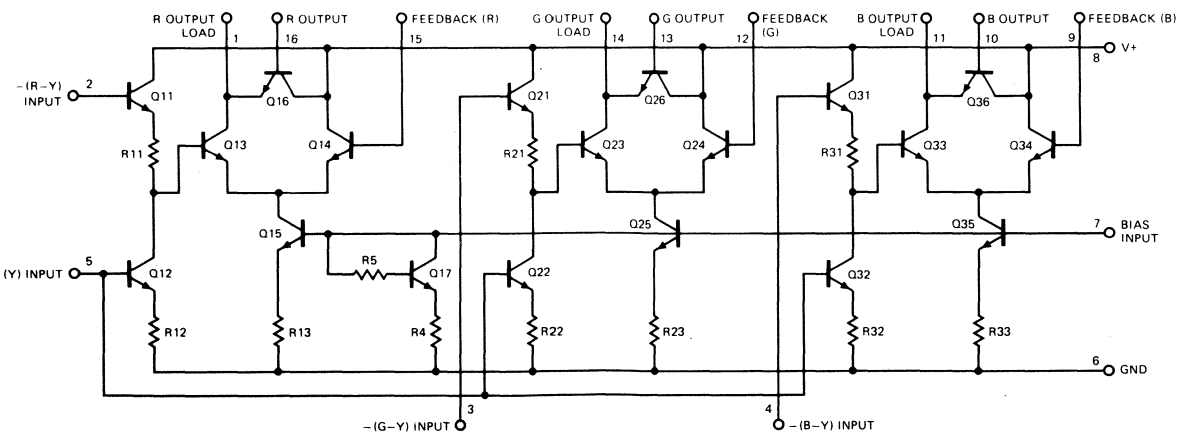
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	13.2 V
Supply Currents (I_1, I_{11}, I_{14})	10 mA
Supply Currents (I_{10}, I_{13}, I_{16}) (Note 1)	50 mA
Total Power Dissipation (Note 1)	400 mW
Storage Temperature	−55°C to +125°C
Operating Ambient Temperature	−20°C to +60°C
Pin Temperature (Soldering, 10 s)	260°C

NOTE:

1. In case of breakdown in the output transistors, 50 mA MAX is permitted from pins 10, 13 and 16 each to pin 8. P_D is then 500 mW MAX.

EQUIVALENT CIRCUIT



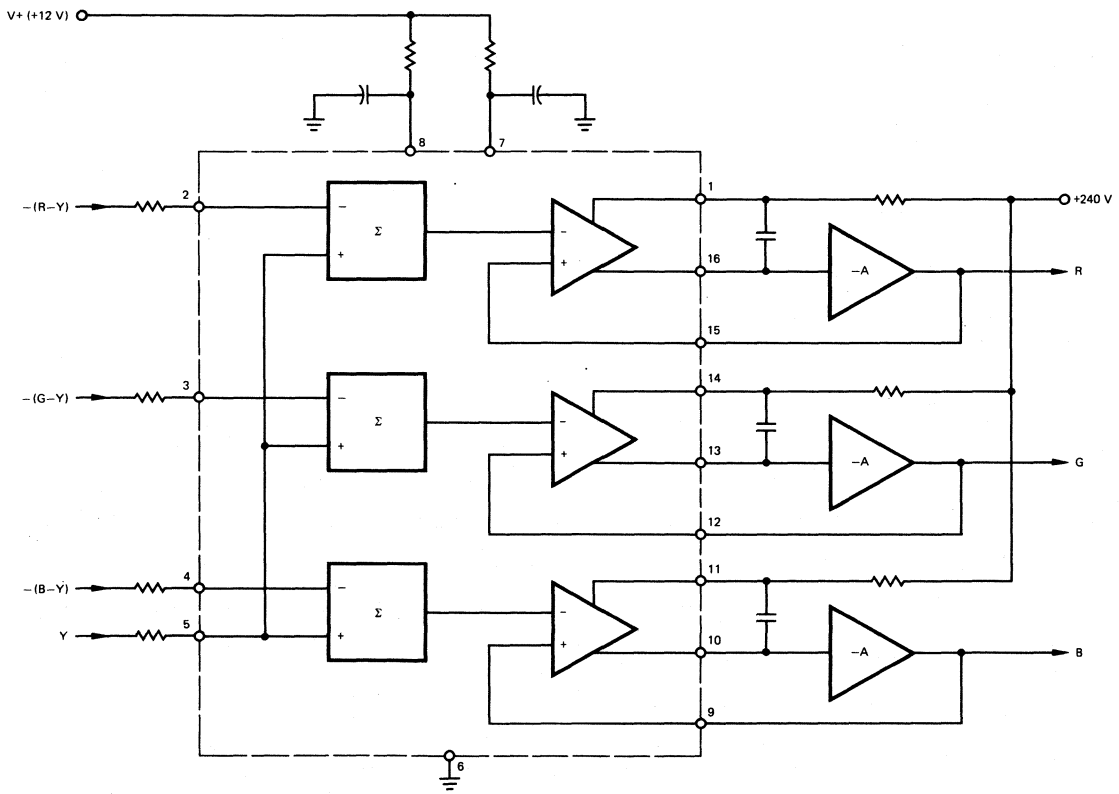
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_8 = 12V$, see application circuit.
Black level settings: $V_{R-Y} = V_{G-Y} = V_{B-Y} = 7.5$ V, $V_Y = 1.5$ V

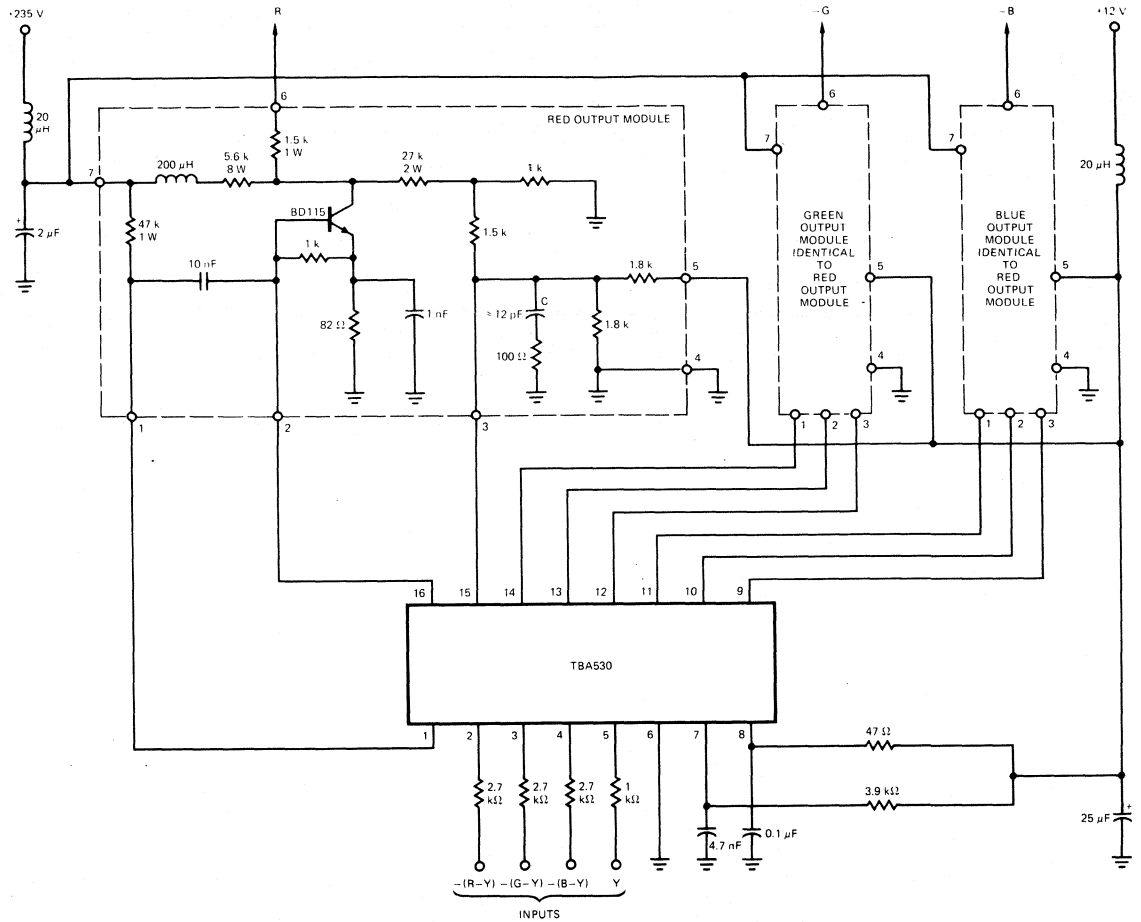
CHARACTERISTICS	MIN	TYP	MAX	UNITS
Supply Current I		30		mA
Required Input Signals				
R-Y (V_2)		1.4		V_{pk-pk}
G-Y (V_3)		0.82		V_{pk-pk}
B-Y (V_4)		1.78		V_{pk-pk}
Y (V_5)		1.0		V_{pk-pk}
Gain of Channels				
(B-Y; G-Y, R-Y) at f = 0.5 MHz (Note 2)		100		
Gain Ratio Luminance to Each Color Amplifier		1.0		
DC Output Voltage, Each Channel		165		V
Input Resistance (Color) f = 1 kHz (R2, R3, R4)		60		kΩ
Input Resistance (Luminance) f = 1 kHz (R5)		20		kΩ
Input Capacitance (Color) f = 1 kHz (C2, C3, C4)		3.0		pF
Input Capacitance (Luminance) f = 1 kHz (C5)		10		pF
Bandwidth, Each Channel 3 dB		6.0		MHz

NOTE:
2. Gain is defined as the voltage ratio between the input signals at pins 2, 3, 4 and the output signals at the collectors of the output transistors.

BLOCK DIAGRAM



APPLICATION CIRCUIT



NOTE:
When using a socket for the IC, shut off the power supplies before inserting or changing devices.

APPLICATIONS INFORMATION

The function is quoted against the corresponding pin number:

1. **Output load resistor, red signal** (pin 11, blue signal; pin 14, green signal). Resistors (47 kΩ, 1 W) connected to +235 V provide the high value loads for the internal amplifying stages. The nominal operating potential on these pins is defined by an internal Zener type junction and the dc feedback and is approximately +8 V. The maximum current which can be allowed at each of these pins is 10 mA.
2. **R-Y input signal** (pin 3: G-Y input signal, pin 4: B-Y input signal). This signal is fed via a low-pass filter from the TBA520 or TBA990 demodulator having a dc level of +7.5 V and an amplitude of 1.40 $V_{pk\text{-}pk}$.
3. **G-Y input signal** The dc black level of this signal is +7.5 V and its amplitude is 0.82 $V_{pk\text{-}pk}$ (pin 2).
4. **B-Y input signal** The dc black level of this signal is +7.5 V and its amplitude is 1.78 $V_{pk\text{-}pk}$ (pin 2).
5. **Luminance signal input** The dc level on this pin for picture black is +1.5 V. The required signal amplitude is 1.0 V black-to-white with negative-going sync (or blanking) for cathode drive as shown.
6. **Ground**
7. **Current feed point** – A current of approximately 2.5 mA is required at this pin, fed via a 3.9 kΩ resistor from +12 V, to bias the internal differential amplifiers. A decoupling capacitor of 4.7 nF is necessary.
8. **Positive 12 V supply** – Maximum supply voltage permitted, 13.2 V.
9. **Blue channel feedback** (pin 12, green channel; pin 15, red channel). The dc working points and gains of both the output stages and the IC amplifier stages are stabilized by the feedback circuits. The black level potentials at the collectors of the output stages (tube cut-off) are adjusted by correctly setting the dc level of the color difference signals produced by the demodulator IC. The gains of the RGB output stages are adjusted to give the correct white temperature setting on the picture tube by adjusting the 1.5 kΩ resistor in the feedback paths. (See applications circuit)
10. **Blue signal output** (green and red signal outputs on pins 13 and 16). These pins internally connected with pins 11, 14 and 1 respectively via Zener type junctions to give a dc level shift appropriate for driving the output transistor bases directly. To by-pass the Zener junctions at high frequencies three 10 nF capacitors are required.
11. **Output load resistor,** blue channel (see pin 1).
12. **Green channel feedback** (see pin 9).
13. **Green channel output** (see pin 10).
14. **Output load resistor,** green channel (see pin 1).
15. **Red channel feedback** (see pin 9).
16. **Red signal output** (see pin 10).

BRIEF PERFORMANCE DETAILS AND COMMENTS

1. Spread of the ratio of voltage gains for color difference and luminance signal inputs 0.9 to 1.1.
2. Very careful attention to ground paths should be given, avoiding common impedances between the input (decoder) side and the output stages. Also, to enable matched performance to be achieved, a symmetrical board and component layout should be adopted for the three output stages. To compensate for the effect upon high frequency response of inevitable differences, e.g., the absence of a potentiometer in one of the stages, the compensating capacitors (C) may be appropriately selected for any given board layout.
3. The signal black level at the collectors of the RGB output stages depends upon the +12 V supply, the dc level of the color difference signals from the demodulator IC and the black level potential of the luminance signal applied to the TBA530 matrix IC. The dc levels of the signals produced and handled by the ICs are designed to have approximately proportional tracking with the 12 V supply potential.

$$\text{i.e., } \frac{\Delta V \text{ (dc level, signal)}}{\Delta V+} \approx \frac{V\text{nom (dc level, signal)}}{12}$$

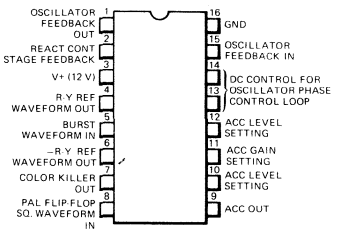
To ensure that changes in picture black level due to variations on the 12 V supply to the ICs occur in a predictable way, all the ICs should be operated from a common supply line. This is specially important for the TBA520 or TBA990 and TBA530. Furthermore, to limit the changes in picture black level during receiver operation, the 12 V supply should have a stability of not worse than ± 3% due to operational variations, and preferably be tracked with the screen-grid supply of the picture tube.

TBA540
REFERENCE COMBINATION
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA540 is an integrated reference oscillator circuit for PAL color television receivers. It incorporates an automatic phase and amplitude controlled crystal oscillator. The half-line frequency synchronous demodulator circuit compares the phases and amplitude of the swinging burst ripple with the PAL flip-flop waveform, and generates appropriate ACC, color killer and identification signals. The use of synchronous demodulation for these functions permits high noise immunity. This circuit is constructed on a single silicon chip using the Fairchild Planar* process.

- **COMPLETE SUBCARRIER REGENERATOR**
- **ACC AMPLIFIER**
- **COLOR KILLER**
- **AUTOMATIC PHASE CONTROL LOOP**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

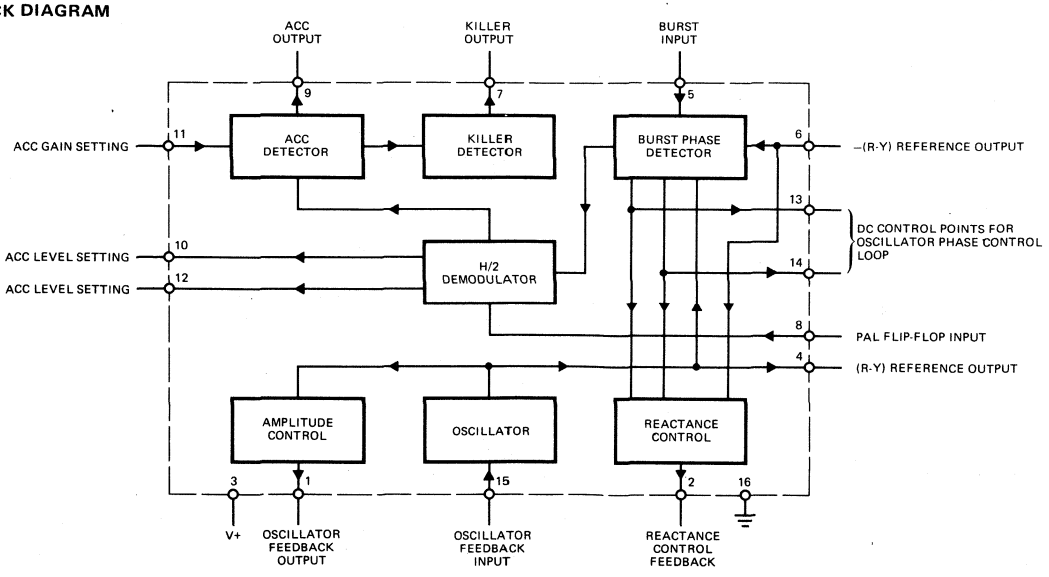
TYPE	PART NO.
540	TBA540
(540Q)	(TBA540Q)†

†Not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	13.2 V
Total Power Dissipation at $T_A = 50°C$	680 mW
Storage Temperature	−55 to +125°C
Operating Ambient Temperature	−20 to +60°C
Pin Temperature (Soldering, 10 s)	260°C

BLOCK DIAGRAM

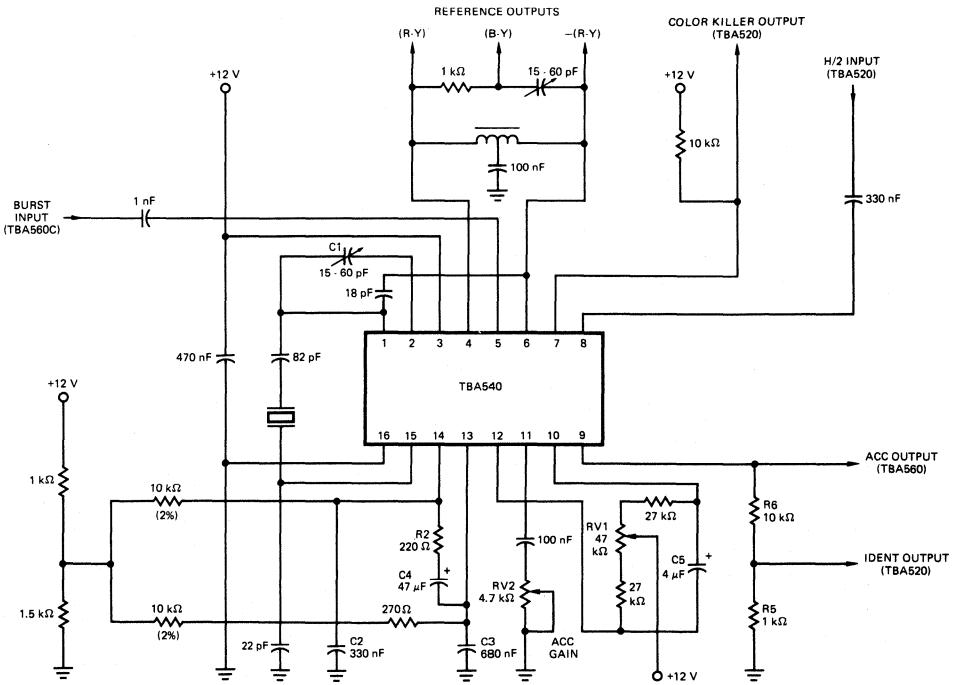


*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $V_{3-16} = 12$ V; $T_A = 25°C$; $V_{5-16} = 1.0\ V_{p\text{-}p}$ (burst signal input); $V_{8-16} = 2.5\ V_{p\text{-}p}$ (PAL Square wave input). Measured in circuit shown in Application Information.

CHARACTERISTICS		MIN	TYP	MAX	UNITS
Output Signals					
R-Y Reference Signal Output	V_{4-16}		1.5		$V_{p\text{-}p}$
Color Killer Output					
Color On	V_{7-16}		12		V
Color Off	V_{7-16}			250	mV
ACC Output Signal Range					
at Correct Phase of PAL Switch	V_{9-16}		+4.0 to +0.2		V
at Incorrect Phase of PAL Switch	V_{9-16}		+4.0 to +11.0		V
Oscillator Section (Amplifier)					
Input Resistance	R_{15}		3.5		kΩ
Input Capacitance	C_{15}		5.0		pF
Voltage Gain	V_{15}/V_1		4.7		V/V
Reactance Control Section					
Voltage Gain with Leads 13 and 14 Interconnected	V_{15}/V_2		1.3		V/V
Rate of Change of Gain V_{15}/V_2 with Phase Difference Between Burst and Reference Signal	$\frac{\Delta(V_{15}/V_2)}{\Delta(\phi_5 - \phi_4)}$		5.0		$\frac{1}{\text{rad}}$
Supply Current Consumption	I_3		38		mA

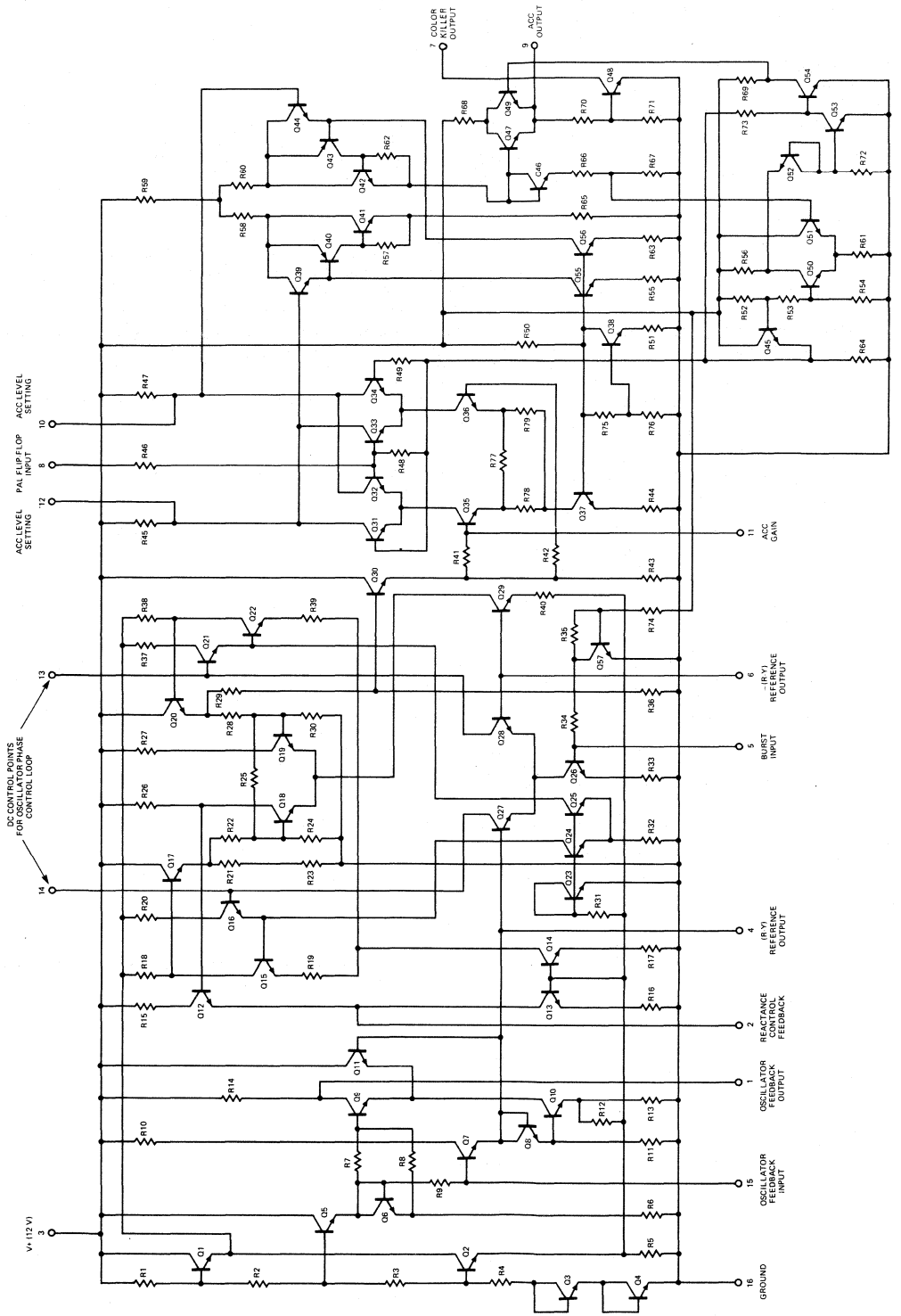
APPLICATION



LEAD NAMES

1. Oscillator Feedback Output
2. Reactance Control Stage Feedback
3. Supply Voltage (12 V)
4. Reference Waveform Output (+)
5. Burst Waveform Input
6. Reference Waveform Output (−)
7. Color Killer Output
8. PAL Flip-Flop Square Wave Input
9. ACC Output
10. ACC Level Setting (see also Lead 12)
11. ACC Gain Setting
12. ACC Level Setting (see also Lead 10)
13. DC Control Points for
14. Oscillator Phase Control Loop
15. Oscillator Feedback Input
16. Ground (Negative Supply)

EQUIVALENT CIRCUIT – TBA540



4

APPLICATION INFORMATION

The function is quoted against the corresponding lead number.

1. **Oscillator Feedback Output**
   The crystal receives its energy from this lead. The input impedance is approximately 2 kΩ in parallel with 5 pF.
2. **Reactance Control Stage Feedback**
   This lead is fed internally with a sinewave derived from the reference input (lead 6) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from lead 2 to the crystal via C1 is such that the value of C1 is effectively increased. Lead 2 is held internally at a very low impedance, therefore, the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.
3. **Positive 12 V Supply**
   The maximum voltage must not exceed 13.2 V.
4. **Reference Waveform Output**
   This lead is driven internally by the regenerated subcarrier waveform in R-Y phase. An output amplitude of nominally 1.5 V peak-to-peak is produced at low impedance. No dc load to ground is required. A dc connection between leads 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on lead 6, a signal of equal amplitude and opposite phase [-(R-Y)] to that on lead 4. A center tap on the inductor, connected to ground via a dc blocking capacitor, is therefore necessary.
5. **Burst Waveform Input**
   A burst waveform amplitude of 1 V peak-to-peak is required to be ac coupled to this lead. The amplitude of the burst will normally be controlled by the adjustment and operation of the ACC circuit. The input impedance at this lead is approximately 1 kΩ and a threshold level of 0.7 V must be exceeded before the burst signal becomes effective. A dc bias of 400 mV is internally derived for lead 5. The absolute level of the tip of the burst at lead 5 will normally reach 1.25 V (1.5 V peak-to-peak burst amplitude). Under abnormal conditions, the burst amplitude should not be allowed to exceed 3 V peak-to-peak and a limiting condition will be reached in the IC which inhibits the performance of the phase lock loop.
6. **Reference Waveform Output**
   This lead requires a reference waveform in the -(R-Y) phase, derived from lead 4 via a bifilar transformer (see lead 4), to drive the internal balanced reactance control stage. A dc connection between leads 4 and 6 must be made via the transformer.
7. **Color Killer Output**
   This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typical 10 kΩ) connected to +12 V. The unkilled and killed voltages on this lead are then +12 V and < 250 mV respectively. (The voltage on lead 9 at which switching of the color killer output on lead 7 occurs is nominally +2.5 V.)
8. **PAL Flip-Flop Square Wave Input**
   A 2.5 V peak-to-peak square wave derived from the PAL flip-flop (in the TBA520 demodulator IC) is required at this lead, ac coupled via a capacitor. The input impedance is about 3.3 kΩ.
9. **ACC Output**
   An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero input signal, the dc potential produced at lead 9 is set to be +4 V (RV1). The appearance of a burst signal on lead 5 will cause the potential on lead 9 to go in a negative direction in the event that the PAL flip-flop is identified to be in the correct phase. The range of potential over which full ACC control is exercised at lead 9 is determined by the control characteristics of the ACC amplifier (i.e. for the TBA560C from 1 V to 0.2 V). The potential at lead 9 will fall to a value within this range as the burst input signal is stabilized at 1.5 V peak-to-peak. The latter condition is achieved by correct adjustment of RV2. If, however, the PAL flip-flop phase is wrong, the potential on lead 9 will move positively. The potential divider R5, R6 will then operate a PAL switch cutoff function in the TBA520 demodulator IC. The switching of the color killer output at lead 7 is designed to occur as the potential on lead 9 moves past +2.5 V.
10. **ACC Level Setting**
    The network connected between leads 10 and 12 balances the ACC circuit and RV1 is adjusted to give +4 on lead 9 with no burst input signal to lead 5. C5 provides filtering.
11. **ACC Gain Control**
    RV2 is adjusted to give the correct amplitude of burst signal on lead 5 (1.5 V peak-to-peak) under ACC control.
12. See lead 10.
13. See lead 14.
14. **DC Control Points in Reference Control Loop**
    Leads 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purposes of dc balancing the reactance stage and the connection of the bandwidth-determining filter network. The conventional double time constant filter networks are R2, C2, R3, C3, and R4, C4. The dc potentials on these leads are nominally +7.2 V.
15. **Oscillator Feedback Input**
    The input impedance at this lead is nominally 3.5 k in parallel with 5 pF. No dc connection is required on this lead. The signal voltage ratio in the IC between lead 15 and lead 1 is nominally 4.7 times.
16. **Negative Supply (Ground)**

PERFORMANCE AND COMMENTS

Initial Adjustment

(a) Remove burst signal.
(b) Short circuit leads 13-14. Adjust oscillator to correct frequency by C1. Remove short circuit.
(c) Set the ACC level adjustment RV1, to give +4 V on lead 9.
(d) Apply burst signal.
(e) Adjust ACC gain, RV2, to give a burst amplitude of 1.5 V peak-to-peak on lead 5.

Phase Lock Loop Performance

(a) Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency, ±10°.
(b) Typical holding range, ±600 Hz.
(c) Typical pull in range, ±300 Hz.
(d) Temperature coefficient of oscillator frequency, IC only, 2 Hz/°C.

TBA560C

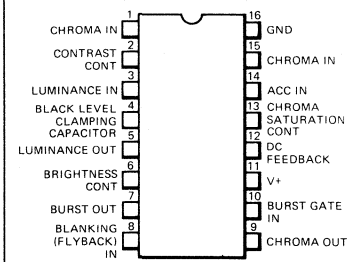
LUMINANCE AND CHROMINANCE CONTROL COMBINATION

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA560C is a monolithic integrated circuit used in the decoding system of color television receivers. It is constructed on a single silicon chip using the Fairchild Planar* process. The circuit consists of a luminance and a chroma amplifier. The luminance amplifier input is matched to the delay line. DC contrast, brightness, black level clamping, blanking, and beam current limiting functions are provided by the luminance amplifier portion of the circuit. The chroma amplifier performs functions such as gain controlled amplification, chroma gain control tracked with contrast control, separate saturation control, PAL delay line driver, burst gating and color killer.

- **DC CONTRAST CONTROL**
- **DC BRIGHTNESS CONTROL**
- **BLACK LEVEL CLAMPING**
- **BEAM CURRENT LIMITING**
- **COLOR KILLER**
- **PAL DELAY LINE DRIVER**
- **CHROMA GAIN/CONTRAST TRACKING**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

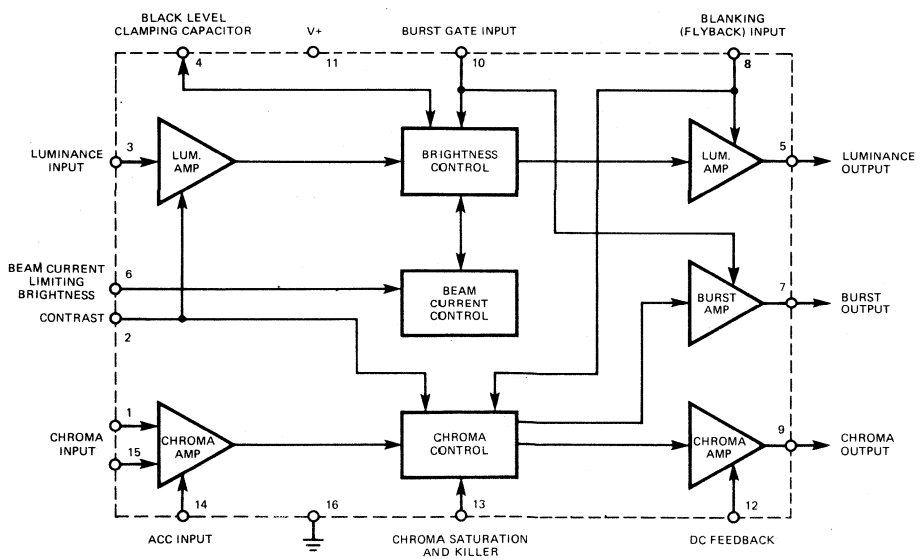
TYPE	PART NO.
560C	TBA560C
(560CQ)	(TBA560CQ)†

†Not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS (Cont'd on Page 2)

Supply Voltage (Note 1)	13 V
Total Power Dissipation (Note 1)	510 mW
Storage Temperature	−55 to +125°C
Operating Ambient Temperature	0 to +60°C
Pin Temperature (Soldering, 10 s)	260°C

BLOCK DIAGRAM



Notes on following page.

*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS (Cont'd)

Voltages

V_{1-16}	0 to +5.0 V	V_{10-16}	−5.0 V
V_{2-16}	0 to +12 V (Note 2)	V_{12-16}	−5.0 to +6.0 V
V_{4-16}	0 to +6.0 V	V_{13-16}	−3.0 to +6.5 V (Note 2)
V_{6-16}	0 to +3.0 V	V_{14-16}	−5.0 V
V_{8-16}	−5.0 to +5.0 V	V_{15-16}	0 to +5.0 V

Currents (Positive when flowing into the integrated circuit)

I_1	0 to +1.0 mA	I_9	−10 to 0 mA
I_3	−1.0 to +3.0 mA	I_{10}	+3.0 mA
I_5	−5.0 to 0 mA	I_{14}	+1.0 mA
I_6	−1.0 to +1.0 mA	I_{15}	0 to +1.0 mA
I_7	−3.0 to +2.0 mA		

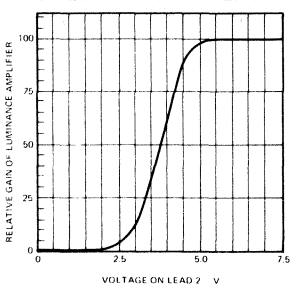
ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_{11-16} = 12V$, as shown in Test Circuit, unless otherwise specified.

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{11}			30		mA
Required Input Signals						
Chrominance Input Signal (Peak-to-Peak Value)	$V_{1-15\ (p\text{-}p)}$			4 to 80		mV
Luminance Input Current (Black to White Value)	$I_{3\ (p\text{-}p)}$			1.5		mA
Contrast Control Voltage Range (for 20 dB of Control)	V_{2-16}	See Typical Performance Curves				
Brightness Control Voltage (Note 3)	V_{6-16}	See Typical Performance Curves				
Saturation Control Voltage Range (for 20 dB of Control)	V_{13-16}	See Typical Performance Curves				
Burst Keying Pulse (Positive) (Peak-to-Peak Value)	$I_{10\ (p\text{-}p)}$		0.05	1.0		mA
Flyback Blanking Pulses (Negative) (Peak-to-Peak Value)						
for 0 V Blanking Level at Lead 5	$V_{8-16\ (p\text{-}p)}$			−0.5		V
for 1.5 V Blanking Level at Lead 5	$V_{8-16\ (p\text{-}p)}$			−2.5		V
Color Killer	V_{13-16}				1.0	V
Automatic Chrominance Control Threshold (Note 4)	V_{14-16}			1.2		V
Obtainable Output Signals						
Luminance Output Voltage at Nominal Contrast (Peak-to-Peak Value)	$V_{5-16\ (p\text{-}p)}$	Note 5		3.0		V
Burst Signal (Peak-to-Peak Value)	$V_{7-16\ (p\text{-}p)}$	Note 6		1.0		V
Chrominance Signal at Nominal Contrast & Saturation (Peak-to-Peak Value)	$V_{9-16\ (p\text{-}p)}$	Note 5		1.0		V
3.0 dB Bandwidth of Chrominance and Luminance Amplifier				5.0		MHz
Change of Ratio, Luminance to Chrominance Signals at 10 dB Contrast Control				2.0		dB

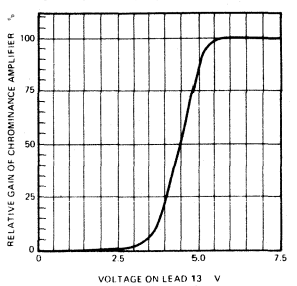
NOTES:
1. Permissible while tubes are heating up: $V_{11-16\ (max)}$ 16 V and $P_{tot\ (max)}$ 700 mW.
2. V_{2-16} and V_{13-16} must always be lower than V_{11-16}.
3. When V_{6-16} is increased above 1.7 V the black level of the output signal remains at 2.7 V.
4. A negative going potential provides a 26 dB ACC range with negligible signal distortion. Maximum gain reduction is obtained at an input voltage of 500 mV typical.
5. Nominal setting: maximum contrast and/or saturation minus 6.0 dB.
6. Burst signal is kept constant at 1.0 V peak-to-peak by automatic gain control (AGC Circuit).

TYPICAL PERFORMANCE CURVES

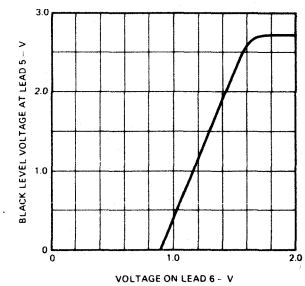
CONTRAST CONTROL OF LUMINANCE AMPLIFIER



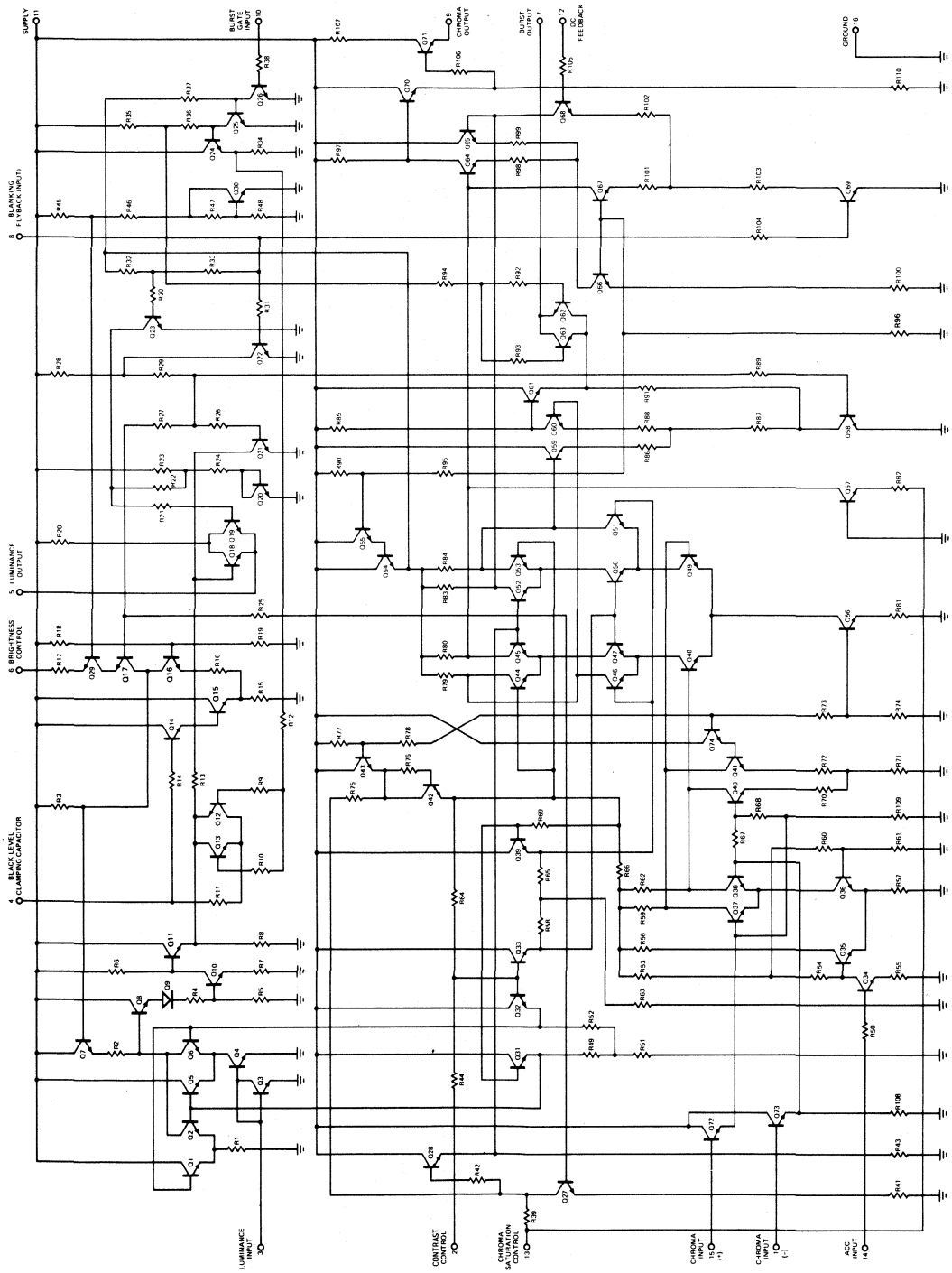
SATURATION OF CHROMINANCE AMPLIFIER



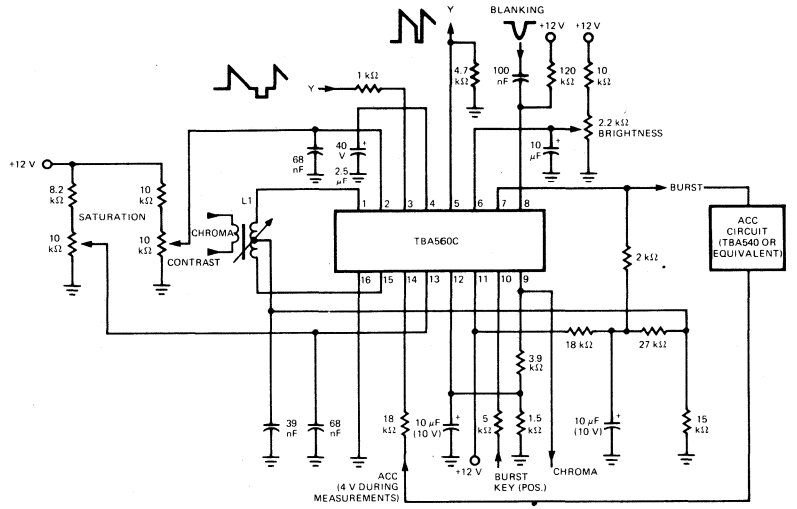
CONTROL OF BLACK LEVEL AT OUTPUT LUMINANCE AMPLIFIER



EQUIVALENT CIRCUIT – TBA560C



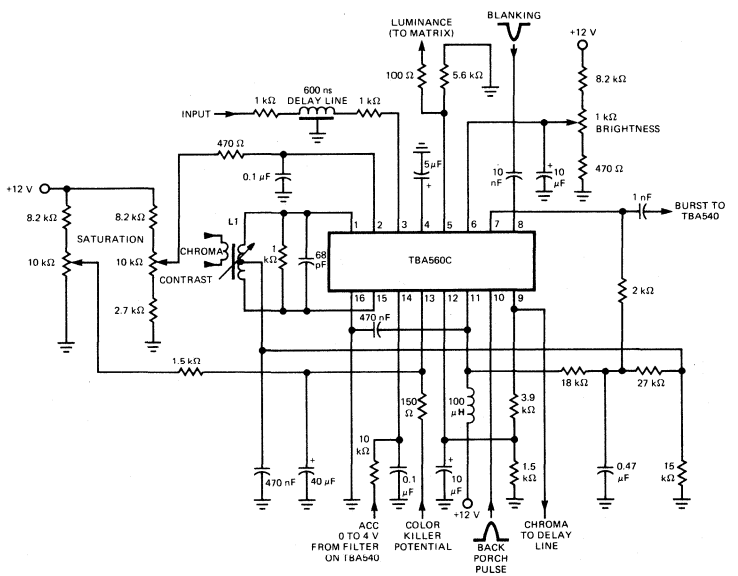
TEST CIRCUIT



APPLICATION INFORMATION

PIN NAMES

1. Balanced Chroma Signal Input
2. Contrast Control
3. Luminance Signal Input
4. Black Level Clamp Capacitor
5. Luminance Signal Output
6. Brightness Control
7. Burst Output
8. Flyback Blanking Input
9. Chroma Signal Output
10. Burst Gate and Clamping Pulse Input
11. Supply Voltage (12 V)
12. DC Feedback for Chroma Channel
13. Chroma Saturation Control
14. ACC Input
15. Chroma Signal Input
16. Ground (Negative Supply)



Application diagram for operation in combination with the TBA540.

APPLICATION INFORMATION (Cont'd)

The function is quoted against the corresponding pin number.

1. **Balanced Chroma Signal Input** (in conjunction with lead 15)
   This is derived from the chroma signal bandpass filter, designed to provide the balanced input. A differential input signal amplitude of at least 4 mV peak-to-peak is required on leads 1 and 15. Both leads require a dc potential of approximately +3.0 V. This is derived as a common-mode signal from a network connected to lead 7 (burst output). In this way, dc feedback is provided over the burst channel to stabilize its operation.
   All figures for the chominance signals are based on a color bar signal with 75% saturation: i.e. burst to chroma ratio of input signal is 1:2.
2. **DC Contrast Control**
   With +3.7 V on this lead, the gain in the luminance channel is such that a 1.5 mA peak-to-peak input signal to lead 3 gives a luminance output signal amplitude on lead 5 of 3 V black to white. A variation of voltage on lead 2 between +6 V and +2 V gives a corresponding gain variation of +6 to > −14 dB. A similar variation in gain in the chroma channel occurs in order to provide the correct tracking between the two signals.
3. **Luminance Signal Input**
   This terminal has a very low input impedance and acts as a current sink. The luminance signal from the delay line is fed via a series terminating resistor and must have about 1.5 mA black to white amplitude.
4. **Charge Storage Capacitor for Black Level Clamp**
   Brightness control can also be achieved on this lead by inserting a negative going line flyback pulse, clipped by a diode to be rectangular, across a resistor of approximately 47 Ω in series with the storage capacitor (5.0 μF). Variation of the amplitude of this pulse shifts the black level of the clamped luminance signal and thus controls the picture brightness.
5. **Luminance Signal Output**
   An emitter follower provides a low impedance output signal of 3 V black to white amplitude at nominal contrast setting having a black level in the range 0 to +3 V. An external emitter load resistor is required, greater than 1 kΩ.
   Black level shift at contrast control is typically in the range of ±10 mV if the luminance input current during black level is about 0.75 mA. When this current has a different value a larger black level shift has to be taken into account. If the input current during black level differs 1 mA from the nominal value of 0.75 mA, the black level shift will be about 100 mV over the complete contrast control range. For smaller differences of the input current, the black level shift will be correspondingly smaller.
   Black level shift with video signal content occurs only when the input signal is ac coupled. The value depends on the drive current amplitude and can be calculated from the figures given above (for maximum contrast; for a lower contrast setting the variation is correspondingly smaller).
   Black level shift over an ambient temperature variation of 30°C is typically −140 mV.
6. **The DC Level of the Luminance Output Signal May be Controlled by the DC Potential Applied to this Lead.**
   Over the range of potential +0.9 to +1.7 V, the black level of the luminance output signal (lead 5) is increased from 0 to +2.7 V. The output signal black level remains at +2.7 V when the potential on lead 6 is increased above +1.7 V.
7. **Burst Output**
   A 1 V peak-to-peak burst (kept constant by the ACC system) is produced here. Also, to achieve good dc stability by negative feedback in the burst channel, the dc potential at this lead is fed back to leads 1 and 15 via the chroma input transformer. When limiting occurs, the burst amplitude is typically 3.0 V.
8. **Flyback Blanking Input Waveform**
   Negative going horizontal and vertical blanking pulses may be applied here. If rectangular blanking pulses of less than −1 V negative excursion are applied, the signal level at the luminance output (lead 5) during blanking will be 0 V. However, if the blanking pulses applied to lead 8 have an amplitude of −2 to −3 V, the signal level at the luminance output during blanking will be +1.5 V.
9. **Chroma Signal Output**
   With a 1 V peak-to-peak burst output signal (lead 7) and at nominal contrast and saturation setting (leads 2 and 13), the chroma signal output amplitude is 1 V peak-to-peak. An external dc network is required which provides negative feedback in the chroma channel via lead 12.
10. **Burst Gating and Clamping Pulse Input**
    A positive pulse of minimum 50 μA is required on this lead to provide gating in the burst channel and luminance channel black level clamp circuit. The timing and width of this current pulse should be such that no appreciable encroachment occurs into the sync pulse or picture line periods during normal operation of the receiver.
11. **+12 V Power Supply**
    Correct operation occurs within the range 10 to 13 V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design, this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels. The power dissipation must not exceed 510 mW at 60°C ambient temperature.
12. **DC Feedback for Chroma Channel** (See lead 9)
13. **Chroma Saturation Control**
    A control range of +6 to > −14 dB is provided over a range of dc potential on lead 13 from +2.7 to +6.2 V. Color killing is also done at this terminal by reducing the dc potential to less than +1 V, e.g. from the TBA540 color killer output terminal. The kill factor is min 40 dB.
14. **ACC Input**
    A negative going potential gives a 26 dB range of ACC starting at +1.2 V and giving maximum gain reduction at an input voltage of typically 500 mV.
15. **Chroma Signal Input** (See lead 1)
16. **Negative Supply** (Ground)

TBA641

AUDIO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

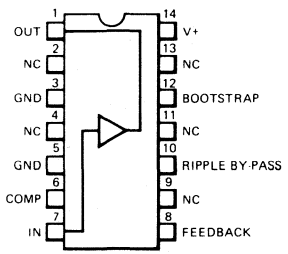
GENERAL DESCRIPTION – The TBA641 is a monolithic integrated circuit designed for use as an audio power amplifier in portable radio receivers, tape recorders, record players and in industrial applications which require high output power, low distortion and high reliability performance.

Special features of the circuit include low quiescent current, self-centering bias operation at supply voltages ranging from 6 V to 12 V (16 V on TBA641 B11) and direct coupling of the input. The circuit requires a minimum of external components. It is constructed on a single silicon chip using the Fairchild Planar* process.

- **OUTPUT POWER 2.2 W (9 V – 4 Ω) – TBA641 A12**
- **OUTPUT POWER 4.5 W (14 V – 4 Ω) – TBA641 B11**
- **LOW DISTORTION**
- **LOW QUIESCENT CURRENT**
- **SELF-CENTERING BIAS**
- **HIGH INPUT IMPEDANCE**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE	9H	9J
PACKAGE CODE	A12	B11



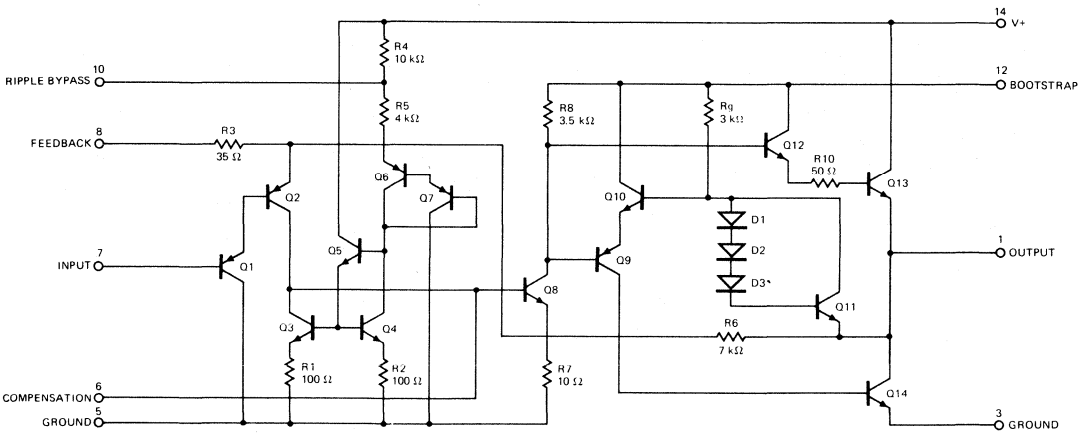
ORDER INFORMATION

TYPE	PART NO.
TBA641 A	TBA641A12
TBA641 B	TBA641B11

ABSOLUTE MAXIMUM RATINGS	**TBA641 A12**	**TBA641 B11**
Supply Voltage (no signal)	12 V	18 V
Supply Voltage	12 V	16 V
Input Voltage	−0.5 V to V+	−0.5 V to V+
Peak Output Current	2A	2.5A
Storage Temperature	−40°C to +150°C	−40°C to +150°C
Power Dissipation ($T_A \leq 25°C$)	1.5 W	2.3 W
Power Dissipation ($T_A = 70°C$)		1.45 W
Power Dissipation ($T_C = 70°C$)		6 W
Max. Junction Temperature	150°C	150°C

THERMAL DATA (Typical)	**TBA641 A12**	**TBA641 B11**
$\theta_{J\text{-}C}$ (thermal resistance junction to case)	13°C/W	13°C/W
$\theta_{J\text{-}A}$ (thermal resistance junction to ambient)	83°C/W	55°C/W

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

TBA641 B11

ELECTRICAL CHARACTERISTICS: V+ = 14 V, R_L = 4 Ω, T_A +25°C unless otherwise specified. (See Test Circuit)

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Total Supply Current		P_{OUT} = 0		16	32	mA
Quiescent Current of Output Transistors		P_{OUT} = 0		13		mA
Input Bias Current (Pin 7)				250		nA
DC Output Level (Pin 1)			6.5	7	8	V
Voltage Gain		R_f = 0 Ω		46		dB
Output Power		THD = 10%, f = 1 kHz, A_V = 46 dB	4	4.5		W
Total Harmonic Distortion		P_{OUT} = 50 mW, f = 1 kHz, A_V = 46 dB		0.3		%
		P_{OUT} = 2W, f = 1 kHz, A_V = 46 dB		0.8		%
Equivalent Input Noise Voltage		R_S = 22 kΩ, BW = 10 kHz		3.4		μV
Total Supply Current		P_{OUT} = 4.5W		485		mA
Internal Feedback Resistors (see equivalent circuit)	R6			7		kΩ
	R3			35		Ω
Input Impedance (Pin 7)		A_V = 46 dB, f = 1 kHz		3		MΩ

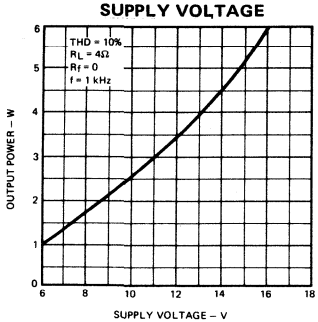
TBA641 A12

ELECTRICAL CHARACTERISTICS V+ = 9 V, R_L = 4 Ω, T_A = 25°C unless otherwise specified. (See Test Circuit)

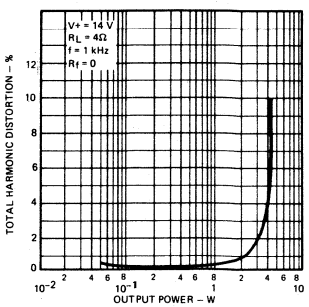
CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Total Supply Current		P_{OUT} = 0		8	18	mA
Quiescent Current of Output Transistors		P_{OUT} = 0		6		mA
Input Bias Current (Pin 7)				100		nA
DC Output Level (Pin 1)			4	4.5	5	V
Voltage Gain		R_f = 0 Ω		46		dB
Output Power		THD = 10%, f = 1 kHz, A_V = 46 dB	1.8	2.2		W
Total Harmonic Distortion		P_{OUT} = 50 mW, f = 1 kHz, A_V = 46 dB		0.6		%
		P_{OUT} = 1W, f = 1 kHz, A_V = 46 dB		0.6		%
Equivalent Input Noise Voltage		R_S = 22 kΩ, BW = 10 kHz		2.5		μV
Total Supply Current		P_{OUT} = 2.2W		340		mA
Internal Feedback Resistors (see equivalent circuit)	R6			7		kΩ
	R3			35		Ω
Input Impedance (Pin 7)		A_V = 46 dB, f = 1 kHz		3		MΩ

TYPICAL PERFORMANCE CURVES FOR TBA641 B11

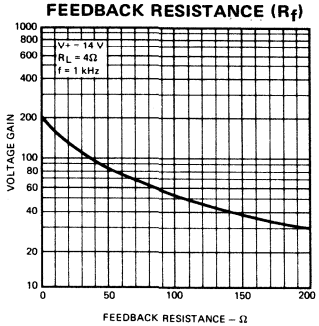
OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE



DISTORTION AS A FUNCTION OF OUTPUT POWER

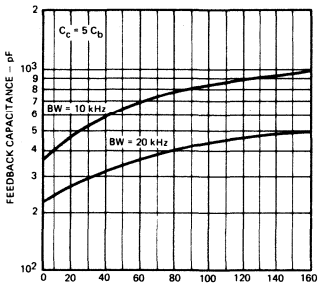


VOLTAGE GAIN AS A FUNCTION OF FEEDBACK RESISTANCE (R_f)

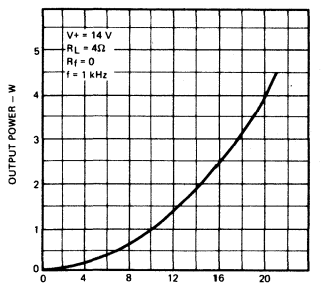


TYPICAL PERFORMANCE CURVES FOR TBA641 B11 (Cont'd)

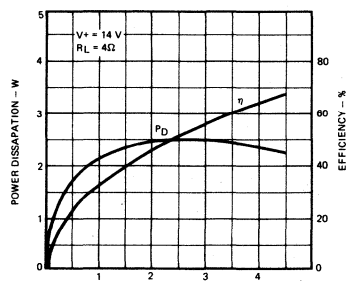
C_b AS A FUNCTION OF R_f FOR VARIOUS VALUES OF BANDWIDTH



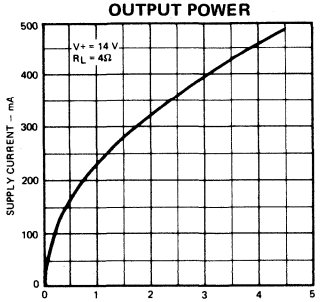
OUTPUT POWER AS A FUNCTION OF INPUT VOLTAGE



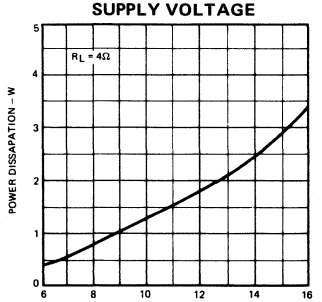
POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF OUTPUT POWER



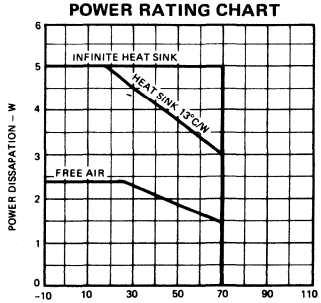
SUPPLY CURRENT AS A FUNCTION OF OUTPUT POWER



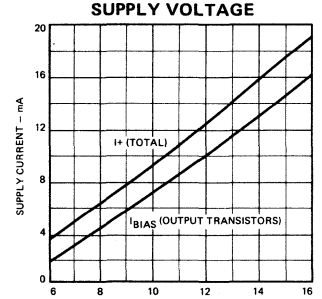
MAXIMUM POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE



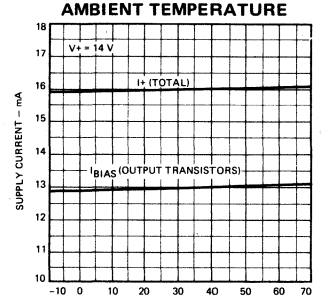
POWER RATING CHART



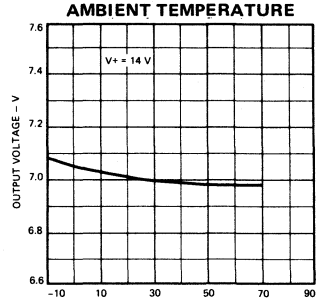
QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



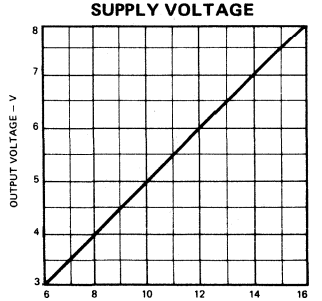
QUIESCENT SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



QUIESCENT OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

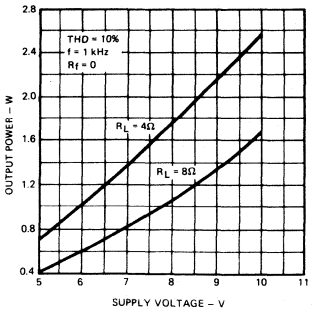


QUIESCENT OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

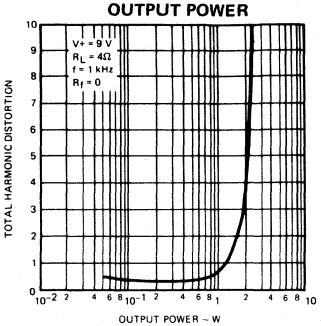


TYPICAL PERFORMANCE CURVES FOR TBA641 A12

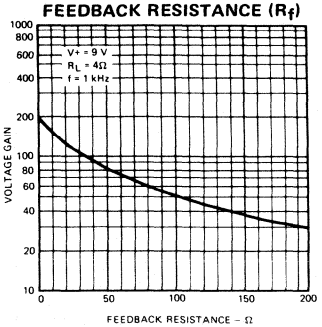
OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE



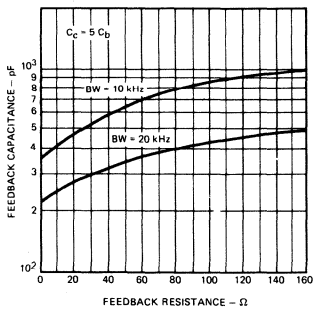
DISTORTION AS A FUNCTION OF OUTPUT POWER



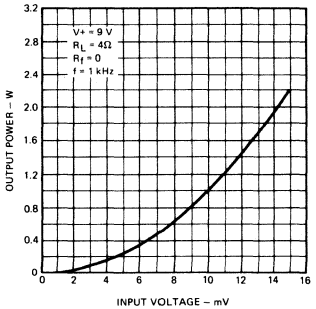
VOLTAGE GAIN AS A FUNCTION OF FEEDBACK RESISTANCE (R_f)



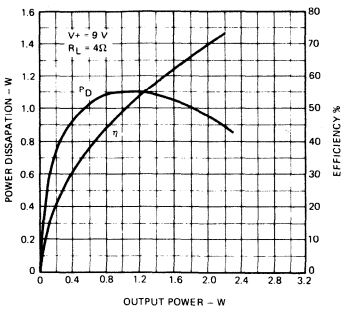
C_b AS A FUNCTION OF R_f FOR VARIOUS VALUES OF BANDWIDTH



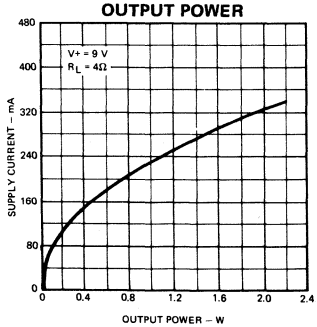
OUTPUT POWER AS A FUNCTION OF INPUT VOLTAGE



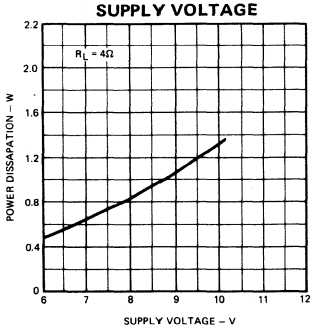
POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF OUTPUT POWER



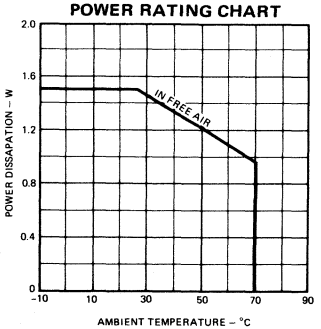
SUPPLY CURRENT AS A FUNCTION OF OUTPUT POWER



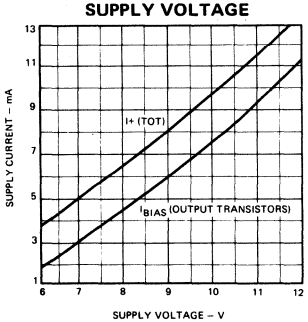
MAXIMUM POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE



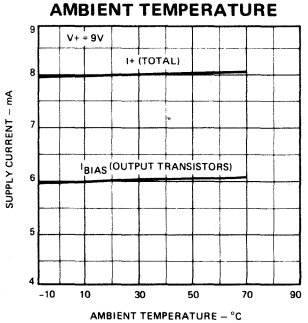
POWER RATING CHART



QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

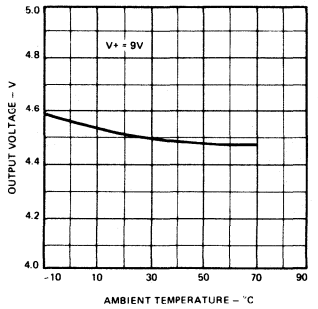


QUIESCENT SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

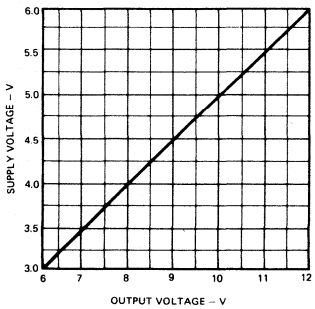


TYPICAL PERFORMANCE CURVES FOR TBA641 A12 (Cont'd)

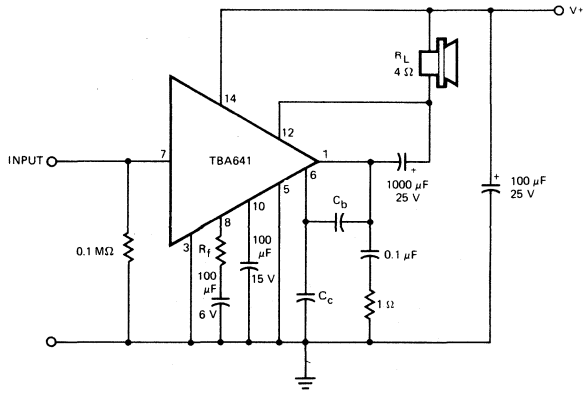
QUIESCENT OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



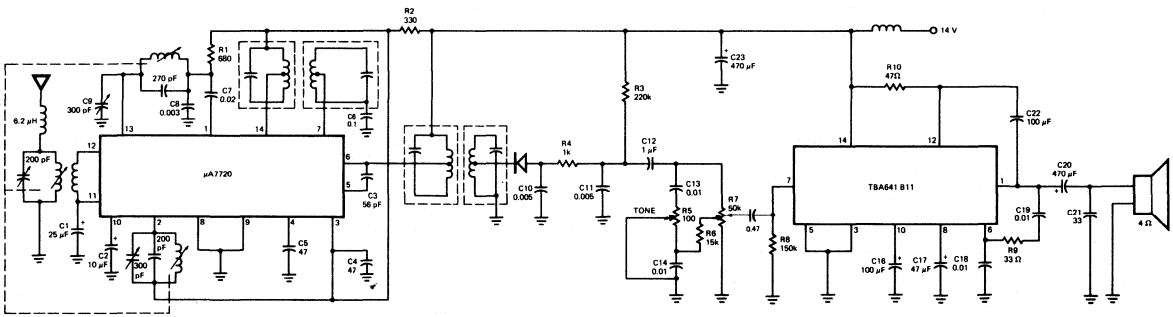
QUIESCENT OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



TEST AND APPLICATION CIRCUIT – TBA641



AM CAR RADIO APPLICATION TBA641 B11



ELECTRICAL PERFORMANCE

Output power (THD = 10%)	4.5 W
Useable sensitivity (S/N = 20 dB)	10 μV
S/N (5 mV Input)	40 dB
AGC Range (ΔV_{OUT} = 10 dB)	80 dB

MOUNTING INSTRUCTIONS – TBA641 B11 Power dissipation can be increased by means of an additional external heat sink fixed with two screws or by soldering the pins of the external bar to suitable copper areas on the PC board (TBA641 B11).

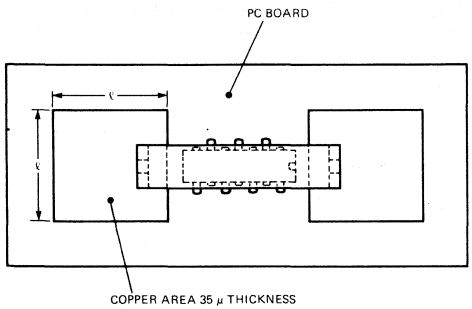
A. In the former case, the thermal resistance case-ambient of the added heat sink can be calculated as follows:

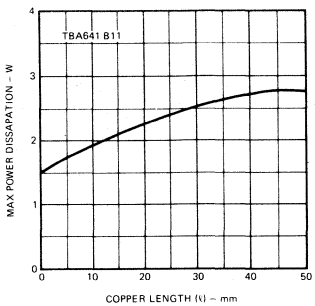
$$\theta_{C\text{-}A} = \frac{(T_{J(MAX)} - T_A) - (P_D)\ (\theta_{J\text{-}C})}{P_D}$$

where:

$T_{J(MAX)}$ = Max junction temperature
T_A = Ambient temperature
P_D = Power dissipation
$\theta_{J\text{-}C}$ = Thermal resistance junction to case

B. If copper areas on the PC board are used (TBA641 B11) the diagrams below give the maximum power dissipation as a function of copper area, with copper thickness 35 μ and ambient temperature 55°C.





TBA800 • TBA800A

5-WATT AUDIO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA800 is a monolithic Audio Power Amplifier constructed using the Fairchild Planar* Epitaxial process. The external cooling tabs enable 2.5 W output power to be achieved without external heat sink and 5 W output power using a small area of the pc board copper as a heat sink.

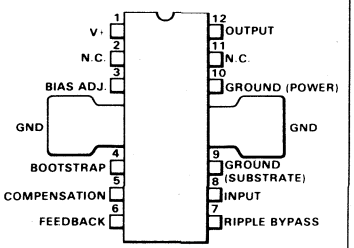
It is ideally suited as an audio amplifier in solid state television receivers and other Class B audio amplifier applications over a wide range of supply voltage (5-30 V).

- **OUTPUT POWER 5 W (24 V – 16 Ω)**
- **LOW DISTORTION**
- **WIDE SUPPLY VOLTAGE RANGE (5-30 V)**
- **HIGH PEAK OUTPUT CURRENT (1.5 A)**
- **HIGH EFFICIENCY**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	30 V
Output Peak Current (Non-Repetitive)	2 A
Output Current (Repetitive)	1.5 A
Power Dissipation: (T_A = 80°C)	1 W
(T_{tab} = 90°C)	5 W
Storage and Junction Temperature	−40°C to +150°C
Pin Temperature (Soldering 10 s)	230°C

CONNECTION DIAGRAM
12-PIN POWER PACKAGE
(TOP VIEW)
PACKAGE OUTLINE 9W
PACKAGE CODE P3, P4

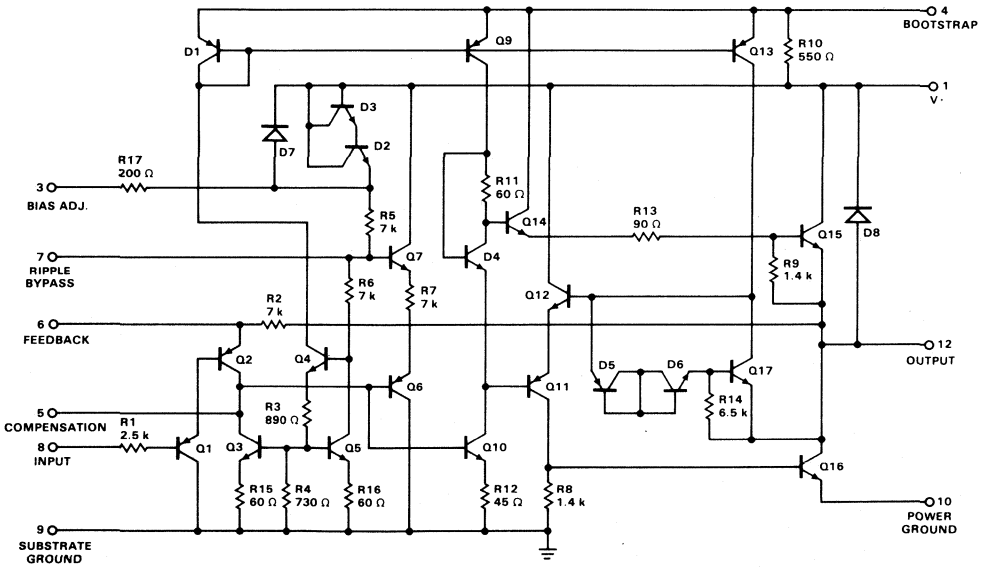


ORDER INFORMATION

TYPE	PART NO.
800 (P3)	TBA800
800A (P4)	TBA800A

*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



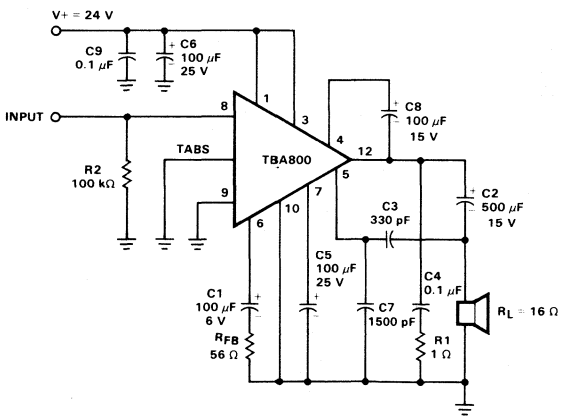
ELECTRICAL CHARACTERISTICS: T_A = 25°C (see Test Circuit)

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		5.0		30	V
Quiescent Output Voltage (Pin 12)	V+ = 24 V	11	12	13	V
Quiescent Drain Current (Pin 1)	V+ = 24 V		9.0	20	mA
Bias Current (Pin 8)	V+ = 24 V		1.0	5.0	μA
Output Power	THD = 10%, R_L = 16 Ω, V+ = 24 V, f = 1 kHz	4.4	5.0		W
Input Saturation Voltage (rms)		220			mV
Input Sensitivity (rms)	P_{OUT} = 5 W, V+ = 24 V, R_L = 16 Ω, f = 1 kHz		80		mV
Input Resistance (Pin 8)			5.0		MΩ
Frequency Response −3.0 dB	V+ = 24 V, R_L = 16 Ω, C_3 = 330 pF		40 – 20,000		Hz
Total Harmonic Distortion	P_{OUT} = 50 mW to 2.5 W, V+ = 24 V, R_L = 16 Ω, f = 1 kHz		0.5		%
Voltage Gain (Open Loop)	V+ = 24 V, R_L = 16 Ω, f = 1 kHz		80		dB
Voltage Gain (Closed Loop)	V+ = 24 V, R_L = 16 Ω, f = 1 kHz	39	42	45	dB
Input Noise Voltage	V+ = 24 V, Rg = 0 Ω, BS (−3.0 dB) = 40–20,000 Hz		5.0		μV
Input Noise Current	V+ = 24 V, BW (−3.0 dB) = 40–20,000 Hz		0.2		nA
Efficiency	P_{OUT} = 5 W, V+ = 24 V, R_L = 16 Ω, f = 1 kHz		75		%

PACKAGE THERMAL RESISTANCE		TBA800		TBA800A
θJ_{tab}	Thermal resistance junction-tab	max	12 °C/W	10 °C/W
θJ_A	Thermal resistance junction-ambient	max	70* °C/W	80 °C/W

*Obtained with tabs soldered to printed circuit with minimum copper area.

TEST CIRCUIT



C3, C7 see Performance Curves

TYPICAL PERFORMANCE CURVES

OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE

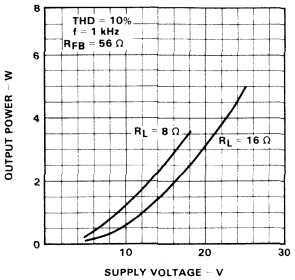


Fig. 1

MAXIMUM POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE

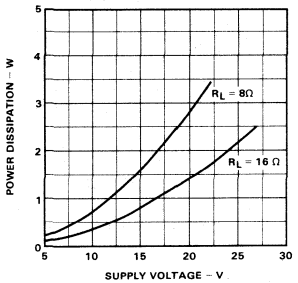


Fig. 2

TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER

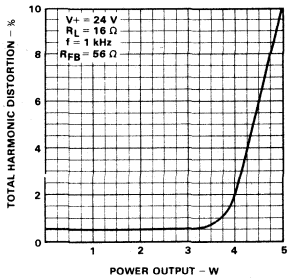


Fig. 3

TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY

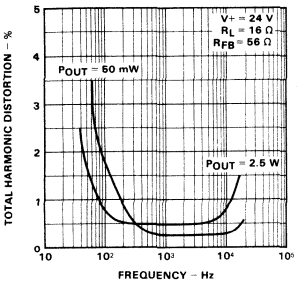


Fig. 4

VALUE OF C3 AS A FUNCTION R_{FB} FOR VARIOUS VALUES OF BW

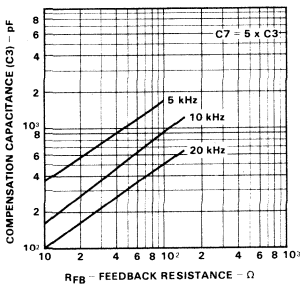


Fig. 5

VOLTAGE GAIN (CLOSED LOOP) AND INPUT VOLTAGE AS A FUNCTION OF R_{FB}

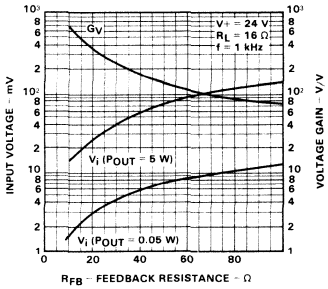


Fig. 6

POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF OUTPUT POWER

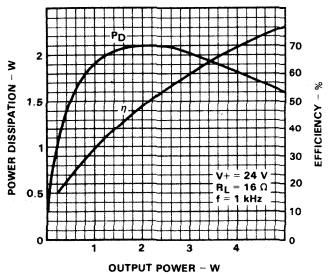


Fig. 7

QUIESCENT OUTPUT VOLTAGE (PIN 12) AS A FUNCTION OF SUPPLY VOLTAGE

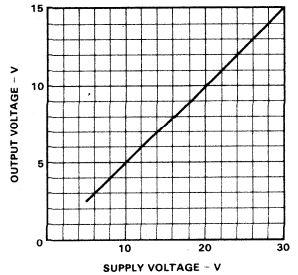


Fig. 8

QUIESCENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

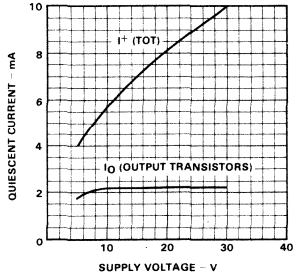


Fig. 9

TYPICAL PERFORMANCE CURVES (cont'd)

TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER (FIG. 15 CIRCUIT)

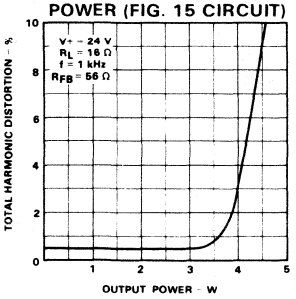


Fig. 10

OUTPUT POWER VERSUS SUPPLY VOLTAGE (FIG. 15 CIRCUIT)

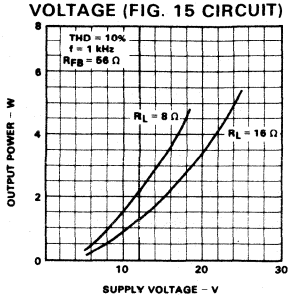


Fig. 11

POWER THAT CAN BE DISSIPATED AS A FUNCTION OF COPPER LENGTH

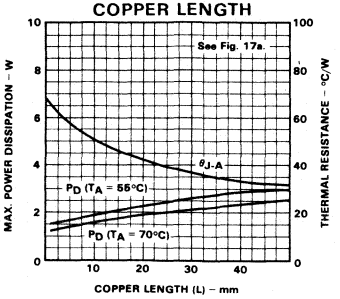


Fig. 12

POWER RATING CHARACTERISTICS

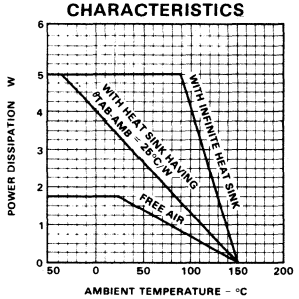
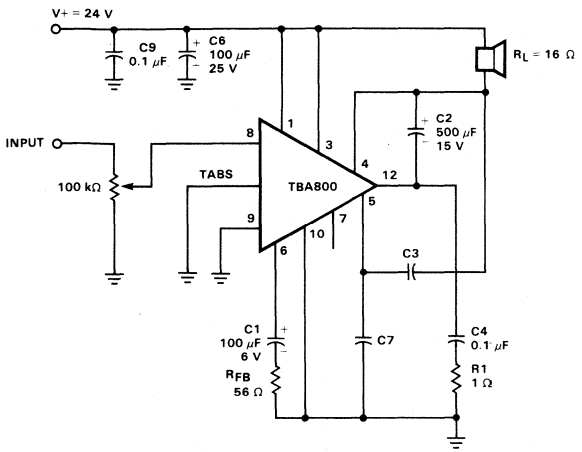


Fig. 13

APPLICATION INFORMATION



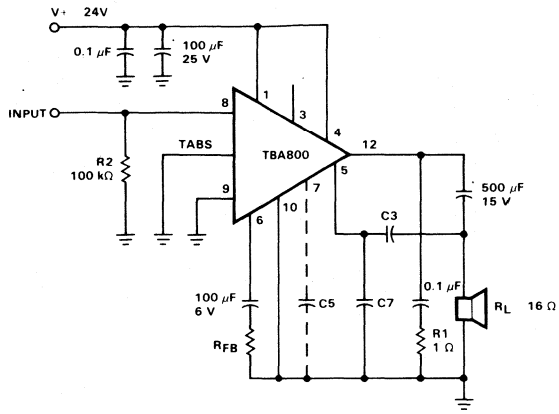
NOTE: Compared with the other circuits, this configuration uses a smaller number of external components and can be used at low supply voltages.

C3, C7 see Performance Curves

Fig. 14. Circuit with the Load Connected to the Supply Voltage

4

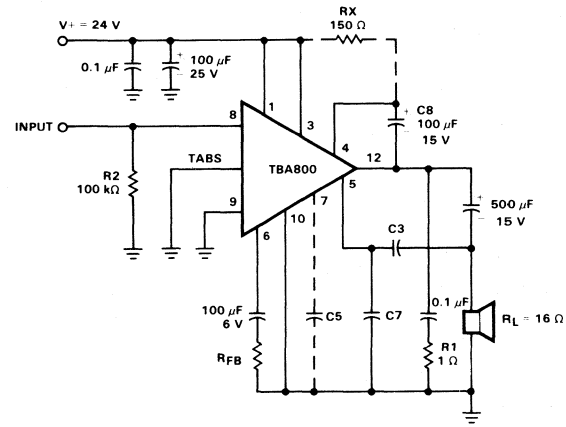
APPLICATION INFORMATION (Cont'd)



C3, C7 see Performance Curves

NOTE: This circuit is only for use at high voltages. If pin 3 is left open circuit, this automatically inserts diodes D2 – D3 (see schematic diagram) and enables a symmetrical signal to be obtained at the output. Refer to Figs. 10 and 11 for distortion and output power.

Fig. 15. Circuit with Load Connected to Ground without Bootstrap

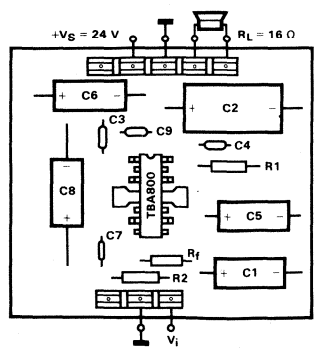


NOTE: The bootstrap capacitor C8 enables the same electrical characteristics as those of the test circuit to be achieved. For low supply voltage operation (*e.g.* 9 to 14 V) RX (150 Ω) is connected between pin 1 and pin 4.

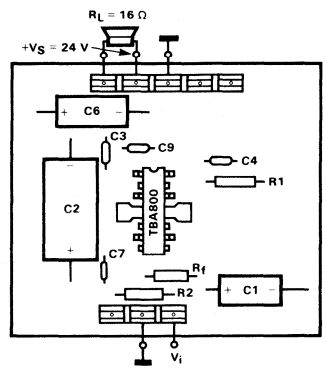
Fig. 16. Circuit with Load Connected to Ground with Bootstrap

NOTE: For the circuits of Fig. 15 and 16 an excellent supply voltage ripple rejection is obtained by connecting the capacitor C5 (10 to 100 μF – 25 V) between pin 7 and ground.

PC Board and Component Layout of the Test Circuit



PC Board Layout (Fig. 14 Circuit)



MOUNTING INSTRUCTIONS – The tabs on the TBA800 can be used to conduct away the heat generated in the integrated circuit so that the junction temperature does not exceed the permissible maximum (150°C). This may be done by connecting tabs to an external heat sink, or by soldering it to a suitable copper area of the printed circuit board (*Fig. 17a*). *Fig. 17b* shows a simple type of heat sink. Assuming an area of copper on the printed circuit board of only 2 cm², the total θ between junction to ambient is approximately 30°C/W.

For TBA800A, the desired thermal resistance is obtained attaching the hardware shown in *Fig. 17c*, to a bracket with proper dimensions. This bracket can also act as a support for the whole printed circuit board.

External heat sink or printed circuit copper area must be connected to electrical ground.

In the latter case, *Fig. 12* shows the maximum dissipated power (for T_A = 55°C) as a function of the side of two equal square copper areas having a thickness of 35 μ (1.4 mils).

Fig. 17a. Example of an area of PC board copper soldered to the tabs of the TBA800, which is used as a heat dissipator.

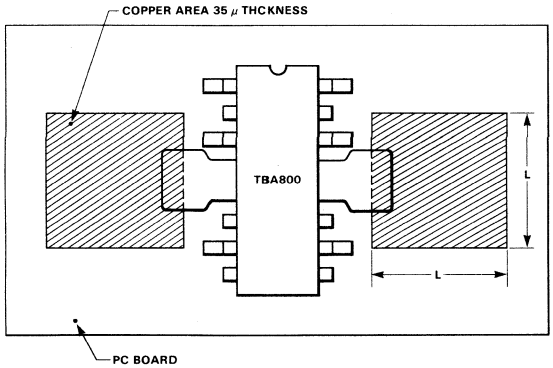


Fig. 17b. Example of TBA800 with external heat sink.

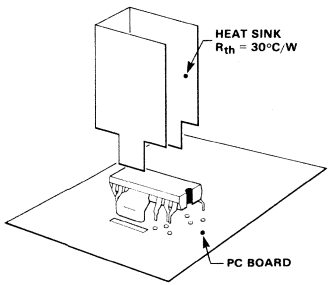
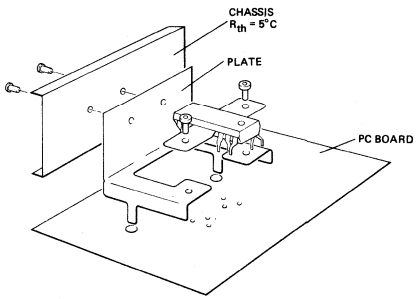


Fig. 17c. Example of TBA800A with external heat sink.



PROCEDURE TO CALCULATE AREA OF COPPER NEEDED

1) Calculate maximum power dissipation

$$P_D = 0.4 \cdot \frac{V+^2_{max}}{8\,R_L} + V+_{max}\, I+$$

where

$V+_{max}$ = maximum value of supply voltage (increase 10% if not stabilized)

R_L = load resistance

$I+$ = quiescent drain current for typical value see *Fig. 9*; maximum value at V+ = 24 V is 20 mA (for worst case design)

$T_{A\ max} = 70°C$

2) From *Fig. 12*, and knowing $T_{A(max)}$, calculate copper length ("L")

Examples:

a) V+ (not stabilized) = 24 V; $R_L = 16\ \Omega$

$$P_D = 0.4 \cdot \frac{(24 + 2.4)^2}{8 \cdot 16} + (24 + 2.4) \cdot 20 \cdot 10^{-3} = 2.6\,W$$

From *Fig. 12* L ≅ 25 mm

For geometries different from the one of *Fig. 17* note that copper areas near the tabs have better efficiency as regards power dissipation. Therefore additional safety factors must be added for worst case designs.

b) V+ (stabilized) = 12 V; $R_L = 8\ \Omega$

$$P_D = 0.4 \cdot \frac{12^2}{8 \cdot 8} + 0.02 \cdot 12 = 1\ W$$

The *Fig. 12* shows that no heat sink is required if $T_A \leqslant 55°C$.

TBA810S/TBA810AS TBA810DS/TBA810DAS

7 WATT AUDIO POWER AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The TBA810S is a monolithic integrated circuit in a 12-lead plastic power package intended for use as a low frequency class B power amplifier. It is constructed using the Fairchild Planar* epitaxial process. With a 4 Ω speaker impedance, it typically provides 7 W at 16 V, 6 W at 14.4 V, 2.5 W at 9 V, and 1 W at 6.0 V. It offers high output current capability (up to 2.5 A), high efficiency (75% at 6 W output) and very low harmonic and crossover distortion.

The TBA810AS has the same electrical characteristics as the TBA810S, but its cooling tabs are flat and provide mounting holes for heat sink attachment.

The TBA810DS is electrically the same as the TBA810S except it includes an overvoltage protection circuit (load dump circuit). This feature makes the TBA810DS ideally suitable for car radio applications.

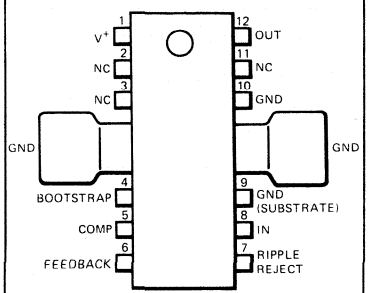
The TBA810DAS has the same electrical characteristics as the TBA810DS, but the cooling tabs are flat and provide mounting holes.

- **THERMAL SHUTDOWN**
- **OVERVOLTAGE PROTECTION (TBA810DS, TBA810DAS)**
- **WIDE SUPPLY VOLTAGE RANGE (4 V TO 20 V)**
- **HIGH CURRENT CAPABILITY (2.5 A)**
- **12-PIN POWER PACKAGE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Peak Current (Non-Repetitive)	3.5 A
Output Current (Repetitive)	2.5 A
Input Voltage	220 mVrms
Power Dissipation: at T_A = 70°C	1.0 W
at T_C = 100°C	5.0 W
Storage and Junction Temperature	−40 to 150°C
Pin Temperature (Soldering, 12 s)	230°C

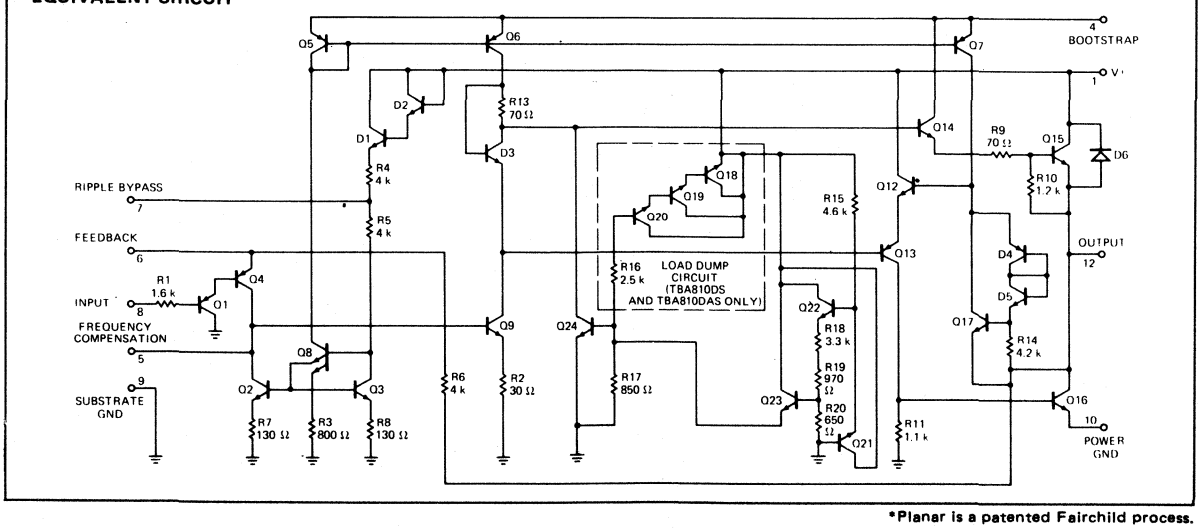
CONNECTION DIAGRAM
12-PIN POWER PACKAGE
(TOP VIEW)
PACKAGE OUTLINE 9W
PACKAGE CODES P3, P4



ORDER INFORMATION

TYPE	PART NO.
810S(P3)	TBA810S
810DS(P3)	TBA810DS
810AS(P4)	TBA810AS
810DAS (P4)	TBA810DAS

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

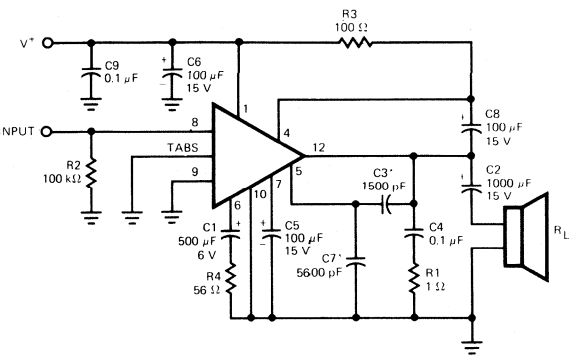
ELECTRICAL CHARACTERISTICS: Refer to the test circuit: $T_A = 25°C$

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Output Voltage (Pin 12)	V+ = 14.4 V	6.4	7.2	8.0	V
Quiescent Drain Current (Pin 1)			12	20	mA
Bias Current (Pin 8)			0.4		μA
Power Output	THD = 10%, R_L = 4.0 Ω, f = 1.0 kHz				
	V+ = 16 V		7.0		W
	V+ = 14.4 V		6.0		W
	V+ = 9.0 V		2.5		W
	V+ = 6.0 V		1.0		W
Input Sensitivity	P_{OUT} = 6 W, V+ = 14.4 V, R_L = 4.0 Ω, f = 1.0 kHz				
	R_f = 56 Ω		80		mV
	R_f = 22 Ω		35		mV
Input Resistance (Pin 8)			5.0		MΩ
Frequency Response (−3.0 dB)	V+ = 14.4 V, R_L = 4.0 Ω				
	C3 = 820 pF		40 to 20,000		Hz
	C3 = 1500 pF		40 to 10,000		Hz
Total Harmonic Distortion	P_{OUT} = 50 mW to 3 W, V+ = 14.4 V, R_L = 4.0 Ω, f = 1.0 kHz		0.3		%
Voltage Gain (Open Loop)	V+ = 14.4 V, R_L = 4.0 Ω, f = 1.0 kHz		80		dB
Voltage Gain (Closed Loop)	V+ = 14.4 V, R_L = 4.0 Ω, f = 1.0 kHz	34	37	40	dB
Input Noise Voltage	V+ = 14.4 V, R_g = 0, BW (−3.0 dB) = 20 Hz to 20,000 Hz		2.0		μV
Input Noise Current	V+ = 14.4 V, BW(−3.0 dB) = 20 Hz to 20,000 Hz		0.1		nA
Efficiency	P_{OUT} = 5 W, V+ = 14.4 V, R_L = 4.0 Ω, f = 1.0 kHz		70		%
Supply Voltage Rejection	V+ = 14.4 V, R_L = 4.0 Ω, f_{ripple} = 100 Hz		38		dB

THERMAL DATA		TBA810S/DS	TBA810AS/DAS
θ_{JC}	Thermal Resistance Junction to Case (tab)	12° C/W	10° C/W
θ_{JA}	Thermal Resistance Junction to Ambient	70° C/W**	80° C/W

**Obtained with tabs soldered to printed circuit with minimized copper area.

TEST AND APPLICATION CIRCUIT



*C3, C7 See Fig. 6

TYPICAL PERFORMANCE CURVES FOR TBA810S/TBA810AS/TBA810DS/TBA810DAS

POWER OUTPUT AS A FUNCTION OF SUPPLY VOLTAGE

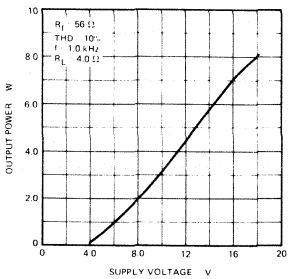


Fig. 1

MAXIMUM POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE (SINE WAVE OPERATION)

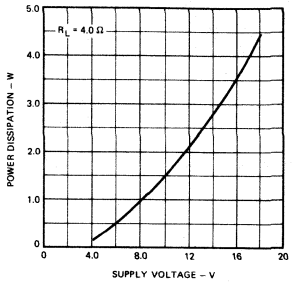


Fig. 2

TOTAL HARMONIC DISTORTION AS A FUNCTION OF POWER OUTPUT

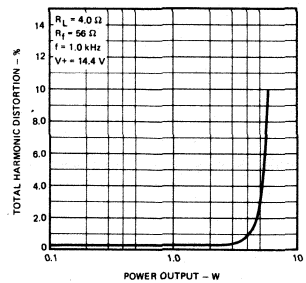


Fig. 3

TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY

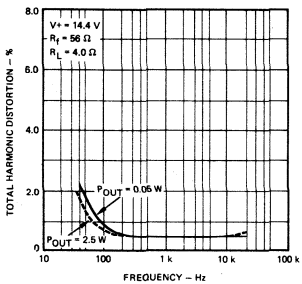


Fig. 4

TYPICAL RELATIVE VOLTAGE GAIN (CLOSED LOOP) AND TYPICAL INPUT VOLTAGE AS A FUNCTION OF FEEDBACK RESISTANCE (R_f)

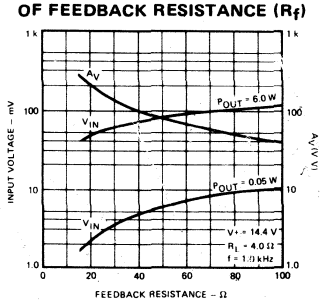


Fig. 5

TYPICAL VALUE OF C3 AS A FUNCTION OF R_f FOR VARIOUS VALUES OF BANDWIDTH

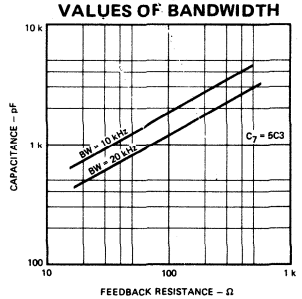


Fig. 6

TYPICAL POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF POWER OUTPUT

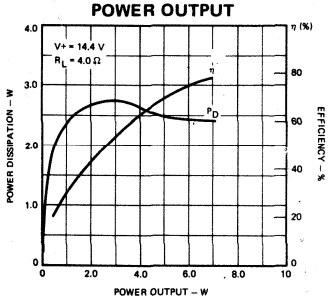


Fig. 7

TYPICAL PERFORMANCE CURVES FOR TBA810S/TBA810AS/TBA810DS/TBA810DAS (Cont'd)

TYPICAL QUIESCENT OUTPUT VOLTAGE (PIN 12) AS A FUNCTION OF SUPPLY VOLTAGE

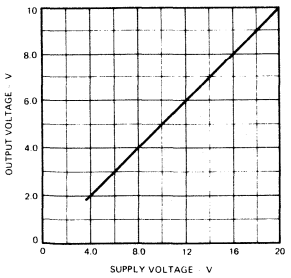


Fig. 8

TYPICAL QUIESCENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

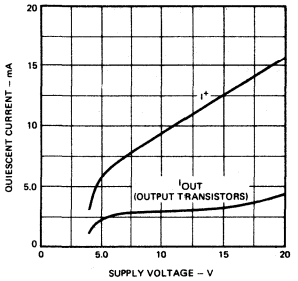


Fig. 9

TYPICAL SUPPLY VOLTAGE REJECTION AS A FUNCTION OF FEEDBACK RESISTANCE

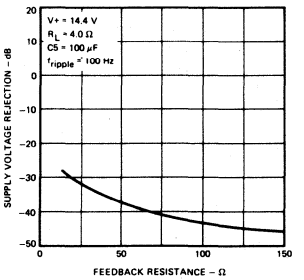


Fig. 10

TYPICAL CIRCUIT WITH LOAD CONNECTED TO THE SUPPLY VOLTAGE

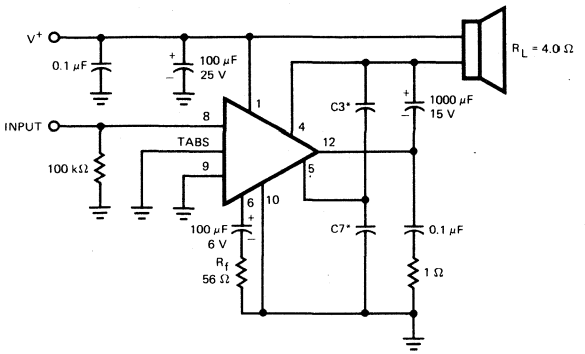


Fig. 11

TYPICAL SUPPLY VOLTAGE REJECTION AS A FUNCTION OF R_f (FIG. 11 CIRCUIT)

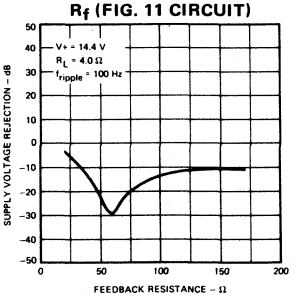


Fig. 12

*C3, C7 see Fig. 6.

MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by connecting the tabs to an external heat sink (TBA810AS/TBA810DAS, Figure 13) or by soldering them to an area of copper on the printed circuit. (TBA810S/TBA810DS, Figure 14). During soldering, the tabs temperature must not exceed 230°C and the soldering time must not be longer than 12 seconds. Figures 15a and 15b show two ways that can be used for mounting the device.

MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TBA810AS AND TBA810DAS)

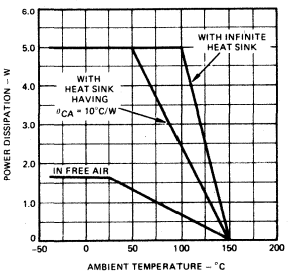
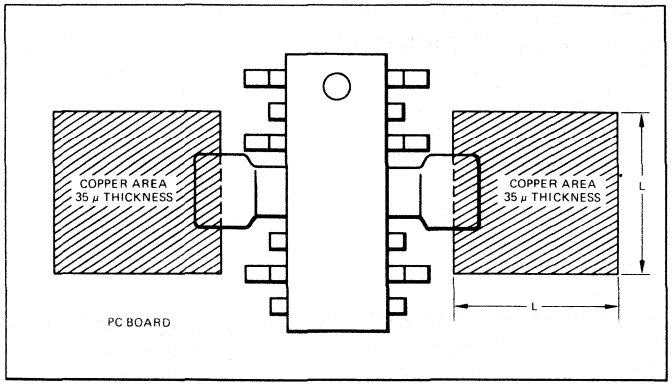


Fig. 13

MAXIMUM POWER DISSIPATION AND TOTAL THERMAL RESISTANCE AS A FUNCTION OF COPPER AREA OF PC BOARD (TBA810S AND TBA810DS)



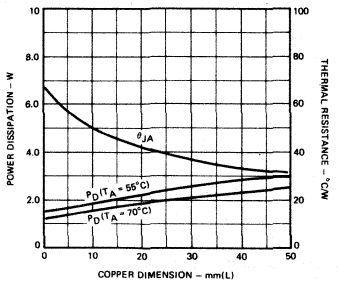


Fig. 14

4

Figure 15a shows a method of mounting the TBA810S or TBA810DS that is satisfactory both from the point of view of heat dissipation and from mechanical considerations. For the TBA810AS and the TBA810DAS, the desired thermal resistance is obtained attaching the hardware shown in Figure 15b, to a bracket with proper dimensions. This bracket can also act as a support for the whole printed circuit board.

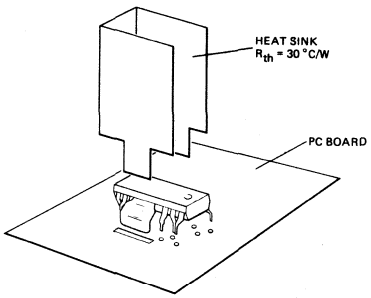


Fig. 15a

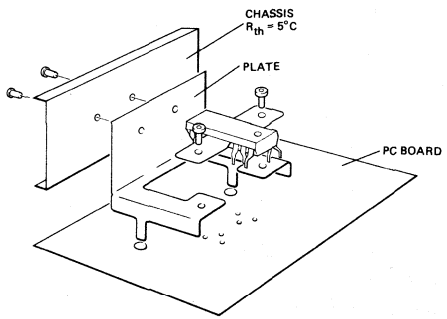


Fig. 15b

THERMAL SHUTDOWN

The on chip design of the thermal limiting circuit offers the following advantages:

1. An overload on the output (even if permanent) or an above-limit ambient temperature can be easily handled.
2. The heat sink can have a smaller factor of safety compared with that of a conventional circuit. In case of too high a junction temperature, power output, power dissipation and the supply current decrease (Figure 16) thus protecting the device.

OUTPUT POWER AND SUPPLY CURRENT AS A FUNCTION OF CASE TEMPERATURE

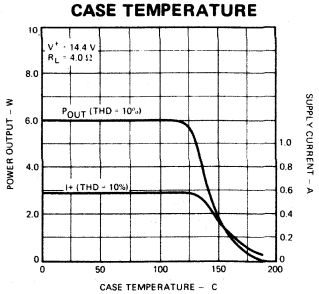


Fig. 16

TBA820 • TBA820L

2-WATT AUDIO AMPLIFIER

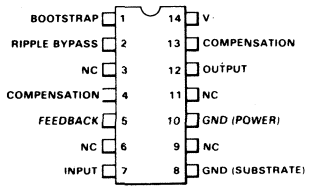
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The TBA820 is an integrated monolithic audio amplifier in a 14-pin plastic power package. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is intended for use as a low frequency class B amplifier with wide range of supply voltage (3 to 16 V).

The device is supplied in both the quad in-line (TBA820) and the standard dual in-line (TBA820L).

- ***MINIMUM WORKING VOLTAGE OF 3 V***
- **LOW QUIESCENT CURRENT**
- **LOW NUMBER OF EXTERNAL COMPONENTS**
- **GOOD RIPPLE REJECTION**
- **NO CROSS-OVER DISTORTION**
- **TYPICAL OUTPUT POWER:**
  - **–2 W AT 12 V – 8 Ω**
  - **–1.6 W AT 9 V – 4 Ω**
  - **–1.2 W AT 9 V – 8 Ω**
  - **–0.75 W AT 6 V – 4 Ω**

CONNECTION DIAGRAM
14-PIN POWER DIP
(TOP VIEW)
PACKAGE OUTLINE 9A, 9C



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	16 V
Output Peak Current	1.5 A
Power Dissipation at T_{amb} = 50°C	1.25 W
Storage and Junction Temperature	–40°C to 150°C
Pin Temperature (Soldering 10 s)	260°C

Thermal Data

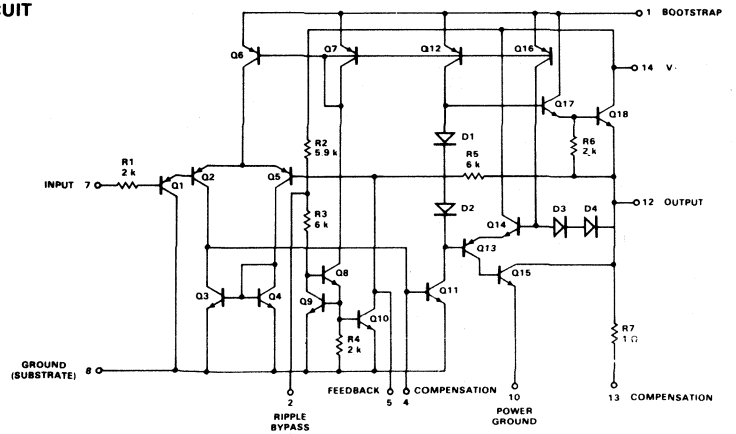
$\theta_{j\text{-amb}}$	Thermal Resistance Junction-Ambient (copper frame) max	80°C/W

ORDER INFORMATION

TYPE	PART NO.
820 (9C)	TBA820
820L (9A)*	TBA820L

*Recommended for new designs.

EQUIVALENT CIRCUIT



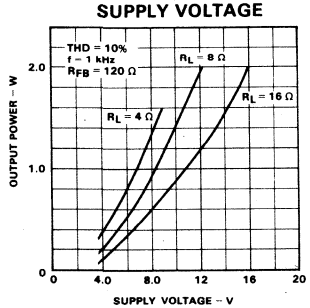
*Planar is a patented Fairchild process

ELECTRICAL CHARACTERISTICS: Power output measured at pin 12, TA = 25°C unless otherwise specified.

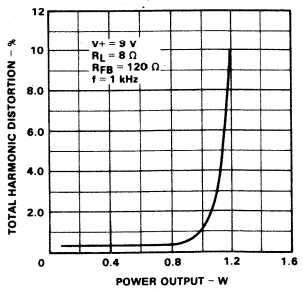
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		3		16	V
Quiescent Output Voltage (Pin 12)	V+ = 9 V	4	4.5	5	V
Quiescent Drain Current	V+ = 9 V		4	12	mA
Bias Current (Pin 7)	V+ = 9 V		0.1	0.7	μA
Power Output, Figure 1	THD = 10%, R_{FB} = 120 Ω, f = 1 kHz,				
	V+ = 12 V, R_L = 8 Ω		2		W
	V+ = 9 V, R_L = 4 Ω		1.6		W
	V+ = 9 V, R_L = 8 Ω	0.9	1.2		W
	V+ = 6 V, R_L = 4 Ω		0.75		W
	V+ = 3.5 V, R_L = 4 Ω		0.22		W
Input Sensitivity, Figure 1	P_{OUT} = 1.2 W, R_L = 8 Ω, V+ = 9 V, f = 1 kHz				
	R_{FB} = 33 Ω		16		mV
	R_{FB} = 120 Ω		60		mV
Input Sensitivity, Figure 1	P_{OUT} = 50 mW, R_L = 8 Ω, V+ = 9 V, f = 1 kHz				
	R_{FB} = 33 Ω		3.5		mV
	R_{FB} = 120 Ω		12		mV
Input Resistance			5		MΩ
Frequency Response (−3 dB) Figure 1	V+ = 9 V, R_L = 8 Ω, R_{FB} = 120 Ω C_{FB} = 680 pF		25 – 7000		Hz
	C_{FB} = 220 pF		25 – 20,000		Hz
Total Harmonic Distortion Figure 1	P_{OUT} = 500 mW, R_L = 8 Ω, V+ = 9 V, f = 1 kHz				
	R_{FB} = 33 Ω		0.8		%
	R_{FB} = 120 Ω		0.4		%
Voltage Gain (Open Loop)	V+ = 9 V, R_L = 8 Ω, f = 1 kHz		75		dB
Voltage Gain (Closed Loop)	V+ = 9 V, R_L = 8 Ω, f = 1 kHz				
	R_{FB} = 33 Ω		45		dB
	R_{FB} = 120 Ω	31	34	37	dB
Input Noise Voltage	V+ = 9 V, BW (−3.0 dB) = 25–20,000 Hz		3		μV
Input Noise Current	V+ = 9 V, BW (−3.0 dB) = 25–20,000 Hz		0.4		nA
Signal Plus Noise to Noise Ratio	V+ = 9 V, R_L = 8 Ω, R_{FB} = 120 Ω BW (−3.0 dB) = 25–20,000 Hz				
	R_1 = 100 kΩ, P_{OUT} = 1.2 W		70		dB
Supply Voltage Rejection, Figure 2	V = 9 V, R_L = 8 Ω, f (ripple) = 100 Hz, C6 = 50 μF, R_{FB} = 120 Ω		42		dB

TYPICAL PERFORMANCE CURVES

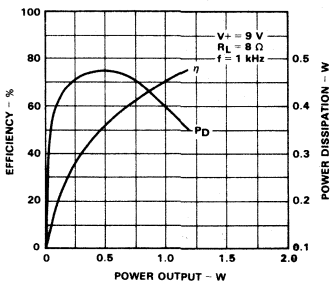
OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY

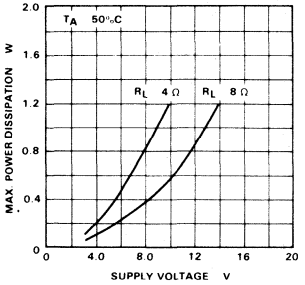


POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF POWER OUTPUT

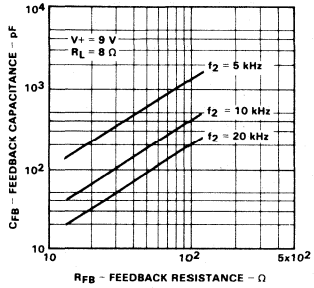


TYPICAL PERFORMANCE CURVES (Cont'd)

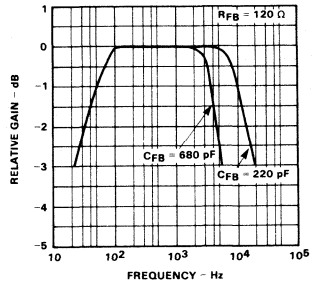
MAXIMUM POWER DISSIPATION (SINE WAVE OPERATION) AS A FUNCTION OF SUPPLY VOLTAGE



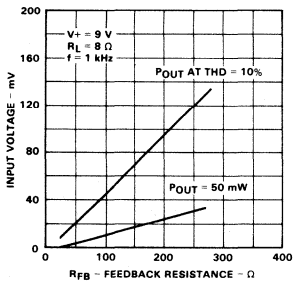
TYPICAL VALUE OF C_{FB} AS A FUNCTION OF R_{FB}



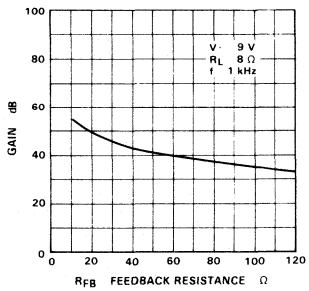
TYPICAL RELATIVE FREQUENCY RESPONSE



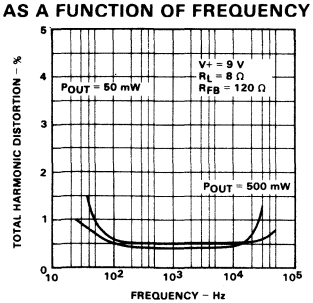
INPUT SENSITIVITY AS A FUNCTION OF R_{FB}



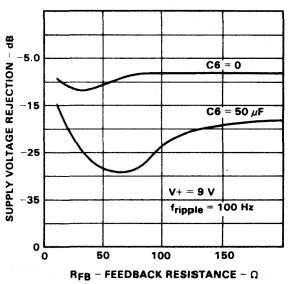
TYPICAL VOLTAGE GAIN (CLOSED LOOP) AS A FUNCTION OF R_{FB}



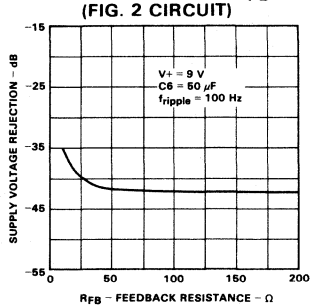
TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY



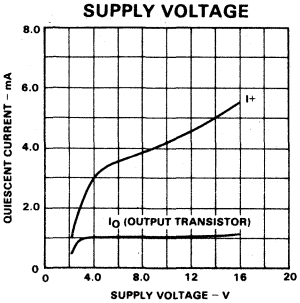
SUPPLY VOLTAGE REJECTION AS A FUNCTION OF R_{FB} FOR FIG. 1 CIRCUIT



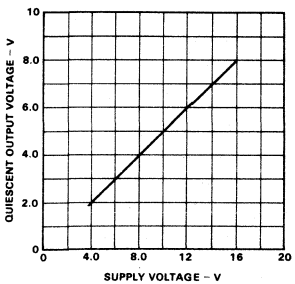
SUPPLY VOLTAGE REJECTION AS A FUNCTION OF R_{FB} (FIG. 2 CIRCUIT)



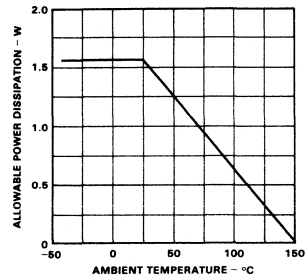
QUIESCENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



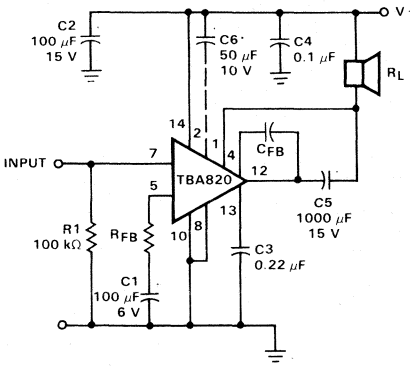
QUIESCENT OUTPUT VOLTAGE AT PIN 12 AS A FUNCTION OF SUPPLY VOLTAGE

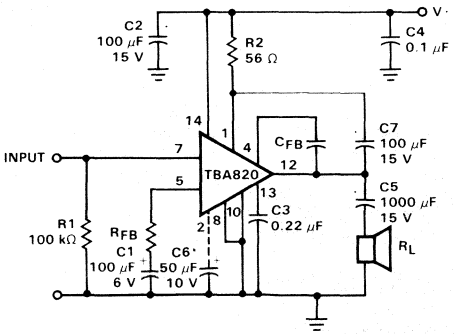


POWER RATING CHART AS A FUNCTION OF AMBIENT TEMPERATURE



TEST AND APPLICATION CIRCUITS





*Capacitor C6 must be used when high ripple rejection is desired.

Fig. 1. Circuit Diagram with Load Connected to the Supply Voltage

Fig. 2 Circuit Diagram with Load Connected to Ground

4

TBA920 · TBA920S

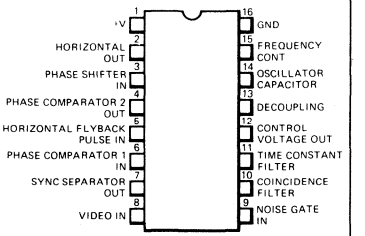
TELEVISION HORIZONTAL OSCILLATORS

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA920s are monolithic integrated circuits designed for TV receiver applications. They are constructed on a single silicon chip using the Fairchild Planar* process. They accept the composite video signal, separate sync pulses (with the added safeguard of noise gating) and provide a sync output for the vertical integrator. Also incorporated is the horizontal oscillator along with two phase comparators, one to compare flyback pulses to the oscillator and the other for sync phase comparison. The devices will interface with both SCR and transistor deflection systems.

- **SYNC SEPARATOR**
- **NOISE GATE**
- **HORIZONTAL OSCILLATOR**
- **DUAL PHASE COMPARATOR**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ABSOLUTE MAXIMUM RATINGS

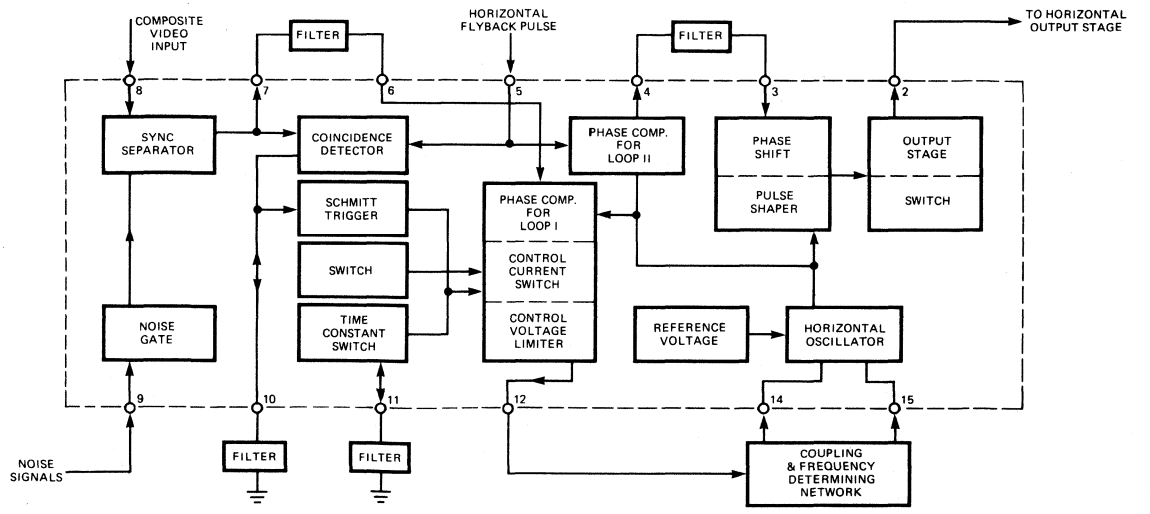
Supply Voltage	13.2 V
Total Power Dissipation (Note 1)	600 mW
Storage Temperature	−55°C to +125°C
Operating Temperature	−20°C to +60°C
Pin Temperature (Soldering, 10 s)	260°C
Voltages	
$V_1 - 16$	13.2 V
$V_3 - 16$	0 to 13.2 V
$V_8 - 16$	−12 V
$V_{10} - 16$	−0.5 to 5.0 V
Currents	
I_2 (Average Value)	−20 mA
I_2 (Peak Value)	−200 mA
I_5 (Peak Value)	10 mA
I_7 (Peak Value)	10 mA
I_8 (Peak Value)	10 mA
I_9 (Peak Value)	10 mA

ORDER INFORMATION

TYPE	PART NO.
920	TBA920
(920Q)	(TBA920Q)†
920S	TBA920S

†Not recommended for new designs.

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_{1-16} = 12V$, See Applications Circuit (CCIR Standard), unless otherwise specified.
***Note: TBA920S is identical to the TBA920 except as indicated.**

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Current Consumption	I_1	$I_2 = 0$		36		mA
Video Signal						
Input Voltage (Positive Going Sync) Peak-to-Peak Value	V_{IN} (p-p)		1.0	3.0	7.0	V
Input Current During Sync Pulse (Peak Value)	I_8			100		μA
Noise Gating (Lead 9)						
Input Voltage (Peak Value)	V_{9-16}		0.7			V
Input Current (Peak Value)	I_9		0.03		10	mA
Input Resistance	R_{9-16}			200		Ω
Flyback Pulse (Lead 5)						
Input Voltage (Peak Value)	V_{5-16}			±1.0		V
Input Current (Peak Value)	I_5		0.05	1.0		mA
Input Resistance	R_{5-16}			400		Ω
Pulse Duration	t_5	f = 15625 Hz	10			μs
Composite Sync Pulses (Positive, Lead 7)						
Output Voltage (Peak-to-Peak Value)	V_{7-16} (p-p)			10		V
Output Resistance						
at Leading Edge of Pulse (Emitter Follower)	R_{7-16}			50		Ω
at Trailing Edge	R_{7-16}			2.2		kΩ
Additional External Load Resistance	R_{7-16} (ext.)		2.0			kΩ
Driver Pulse (Lead 2)						
Output Voltage (Peak-to-Peak Value)	V_{2-16} (p-p)			10		V
Average Output Current	I_2 (AVG)				20	mA
Peak Output Current	I_2				200	mA
Output Resistance (Low Ohmic)	R_{2-16}	Note 2		2.5 or 15		Ω
Output Pulse Duration	t_2	Note 3		12 to 32		μs
Permissible Delay Between Leading Edge of Output Pulse and Flyback Pulse	t_d (tot)	$t_5 = 12$ μs		0 to 15		μs
Supply Voltage at Which Output Pulses are Obtained	V_{1-16}		4.0			V
Oscillator						
Frequency, Free Running	f_o	$R_{15-16} = 3.3$ kΩ (Note 4)		15625		Hz
Spread of Frequency at Nominal Values of Peripheral Components (TBA920)	$\frac{\Delta f_o}{f_o}$	Note 5			±5.0	%
*Spread of Frequency at Nominal Values of Peripheral Components (TBA920S)	$\frac{\Delta f_o}{f_o}$				±1.5	%
Frequency Change When Decreasing the Supply Down to Minimum 4.0 V	$\frac{\Delta f_o}{f_o}$				10	%
Frequency Control Sensitivity	$\frac{\Delta f_o}{\Delta I_{15}}$			16.5		Hz/μA
Adjustment Range of Network in Circuit on Application Information (TBA920)	$\frac{\Delta f_o}{f_o}$			±10		%
*Adjustment Range of Network in Figure 1 (TBA920S)	$\frac{\Delta f_o}{f_o}$			±5.0		%
Influence of Supply Voltage on Frequency	$\frac{\delta f_o/\delta V}{f_o/V_{nom}}$	$V_1 = 12$ V			5.0	%
Control Loop I (Between Sync Pulse and Oscillator)						
Control Voltage Range	V_{12-16}			0.8 to 5.5		V
Control Current (Peak Values)	I_{12}	$V_{10-16} > 4.5$ V; $V_{6-16} > 1.5$ V,		±2.0		mA
	I_{12}	$V_{10-16} > 2.0$ V; $V_{6-16} > 1.5$ V		±6.0		mA
Loopgain of APC System						
a. Time Coincidence Between Sync Pulse and Flyback Pulse or $V_{10-16} > 4.5$ V	$\frac{\Delta f}{\Delta t}$			1.0		kHz/μs
b. No Time Coincidence or $V_{10-16} < 2.0$ V	$\frac{\Delta f}{\Delta t}$			3.0		kHz/μs
Capture and Holding Range	Δf	Note 6		±1.0		kHz
Pull In Time for $\Delta f/f_o = \pm 3\%$	t	$\Delta f = 470$ Hz (Note 7)		20		ms
Switch Over From Large Control Sensitivity to Small Control Sensitivity After Capture	t	Note 7		20		ms

ELECTRICAL CHARACTERISTICS: (Cont'd)

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Control Loop II						
(Between Flyback Pulse and Oscillator)						
Permissible Delay Between Leading Edge of Output Pulse (Lead 2) and Leading Edge of Flyback Pulse	$t_{d\ (tot)}$			0 to 15		µs
Static Control Error	$\frac{\Delta t}{\Delta t_d}$	Note 8			0.5	%
Output Current During Flyback Pulse (Peak Value)	I_4			±0.7		mA
Overall Phase Relation						
Phase Relation Between Leading Edge of Sync Pulse and Middle of Flyback Pulse	t	Note 9		4.9		µs
Tolerance of Phase Relation (TBA920)	$\lvert\Delta t\rvert$	Note 10			1.0	µs
Tolerance of Phase Relation (TBA920S)	$\lvert\Delta t\rvert$				0.4	µs
Voltage for t_2 = 12 to 32 µs	V_{3-16}			6 to 8		V
Adjustment Sensitivity	$\frac{\Delta t_2}{\Delta V_{3-16}}$			10		µs/V
Input Current	I_3				2.0	µA
External Switch Over of Parameters						
(Loop Filter and Loop Gain) of Control Loop I						
(e.g. for Video Recorder Application) See Note 11						
Required Switch Over Voltage	V_{10-16}	R_{11-16} = 150 Ω	4.5			V
	V_{10-16}	R_{11-16} = 2.0 kΩ			2.0	V
Required Switch Over Current	I_{10}	R_{11-16} = 150 Ω V_{10-16} = 4.5 V (Note 11)		80		µA
	I_{10}	R_{11-16} = 2.0 kΩ, V_{10-16} = 2.0 V (Note 11)		120		µA

NOTES:

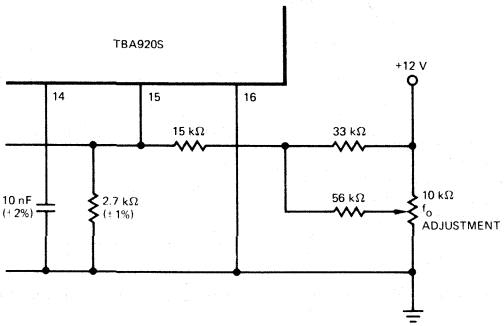
1. 800 mW permissible while tubes are heating up.
2. Depends on switch position and polarity output current. R_{2-16} = 2.5 Ω is valid for V_{2-16} = +10.5 V and a load between leads 2 and 16 (e.g. an external resistor).
3. The output pulse duration is adjusted by shifting the leading edge (V_{3-16} from 6.0 V to 8.0 V). The pulse duration is a result of delay in the line output device and the action of the second control loop in the TBA920.

   For a line output stage with BU108 high voltage transistor the resulting duration is about 22 µs, and in such a way that the line output transistor is switched on again about 8.0 µs after the middle of the line flyback pulse. This pulse duration must be taken into account when designing the driver stage and driver transformer as this way of driving the line output device differs from the usual, i.e. a driver duty cycle of about 50%.
4. The oscillator frequency can be changed for other TV standards by an appropriate value of C_{14-16}.
5. Exclusive external components tolerances.
6. Adjustable with R_{12-15}.
7. See application information circuit.
8. The control error is the remaining error in reference to the nominal phase position between leading edge of the sync pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.
9. This phase relation assumes a luminance delay line with a delay of 500 ns between the input of the sync separator and the drive to the picture tube. If the sync separator is inserted after the luminance delay line or if there is no delay line at all (black and white sets), then the phase relation is achieved at C_{5-16} = 560 pF.
10. The adjustment of the overall phase relation and consequently the leading edge of the output pulse at lead 2 occurs automatically by the control loop II or by applying a dc voltage to lead 3.
11. With sync pulses at lead 7 and 8; without RC network at lead 10.

TEST CIRCUITS

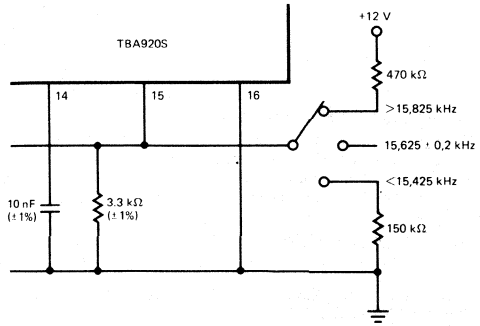
TBA920S

(See application circuit for balance of circuitry)



Frequency adjustment range. Test circuit for TBA920S.

Fig. 1

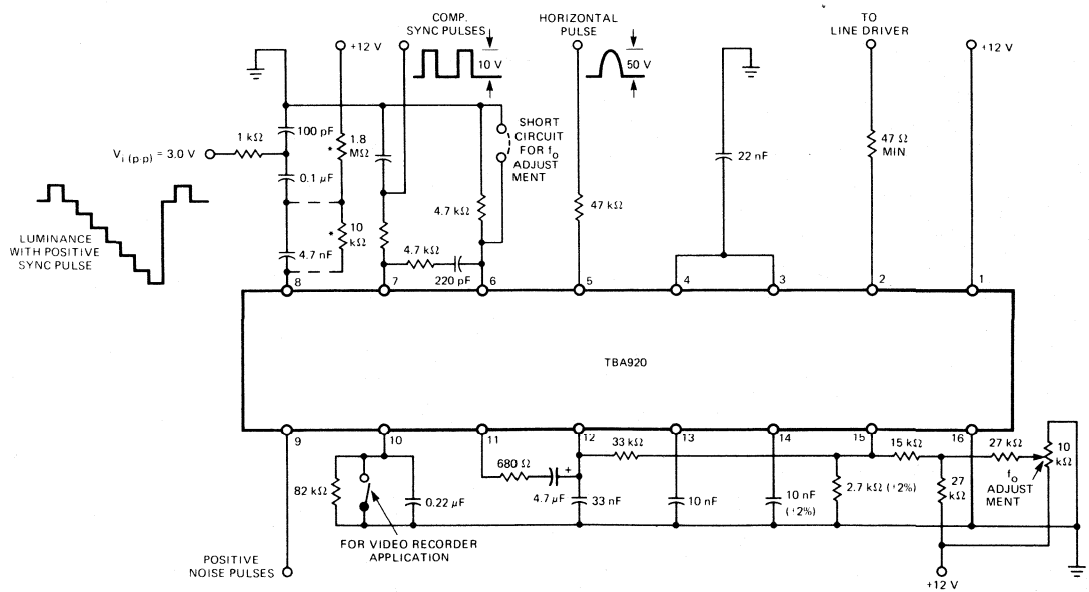


Other circuit possibilities for oscillator frequency adjustment.

Fig. 2

APPLICATION

(See Fig. 1 for TBA920S network)



*To bias input direct to base.

TBA970

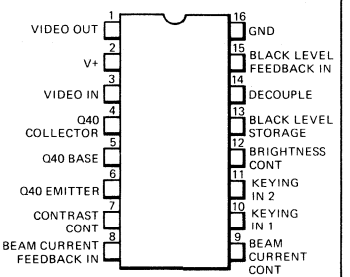
TELEVISION VIDEO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA970 is a monolithic video amplifier for television receivers. It is constructed using the Fairchild Planar* epitaxial process. The circuitry includes a video preamplifier, dc contrast control utilizing a linear potentiometer which can be ganged to the chroma gain control, beam current limiting via contrast. Beam current limiting could be obtained with either positive or negative control voltage. Black level control is achieved by a clamped feedback circuit combined with the brightness control. Emitter follower output could be used to directly drive the video output stage. A separate NPN transistor (Q40) is provided on the chip.

- **DC CONTRAST CONTROL**
- **DC BRIGHTNESS CONTROL**
- **BLACK LEVEL CLAMPING**
- **BEAM CURRENT LIMITING**
- **LOW IMPEDANCE OUTPUT**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

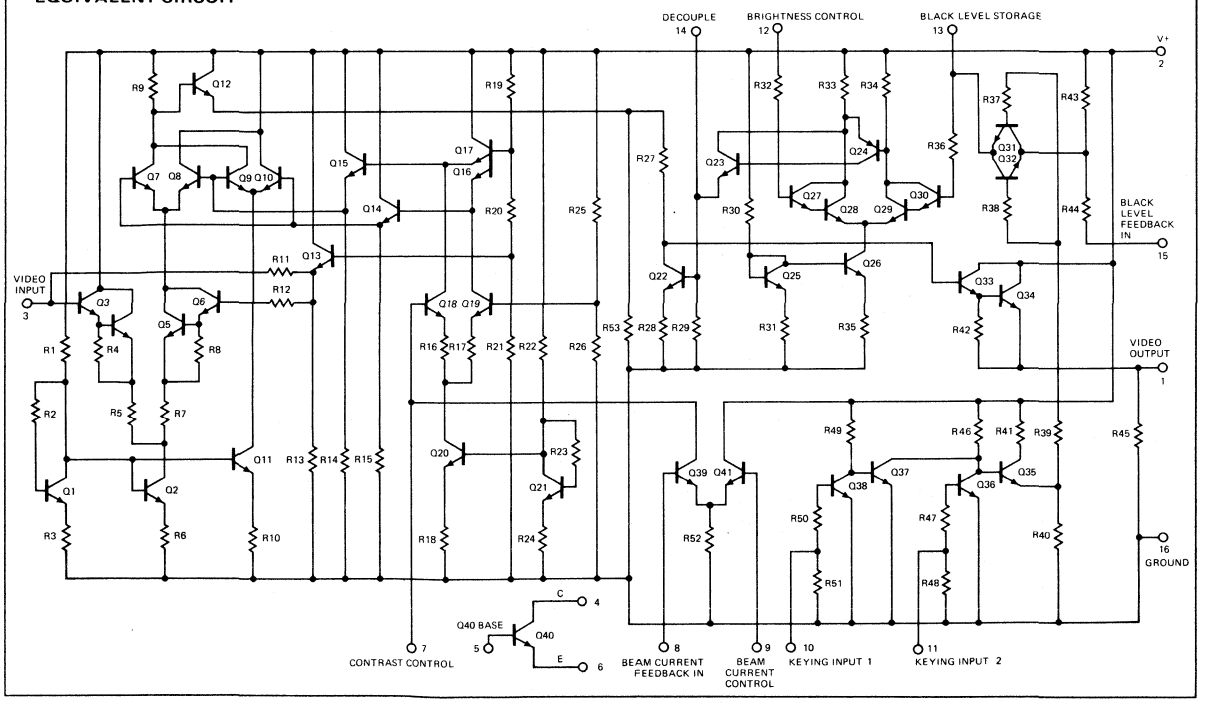
TYPE	PART NO.
970	TBA970
(970Q)	(TBA970Q)†

†Not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15.5 V
Internal Power Dissipation	750 mW
Collector Current Q40	10 mA
Power Dissipation Q40	20 mW
V_{CEO} Q40	13.2 V
V_{CES} Q40	15.5 V
Operating Temperature Range	−20°C to +45°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



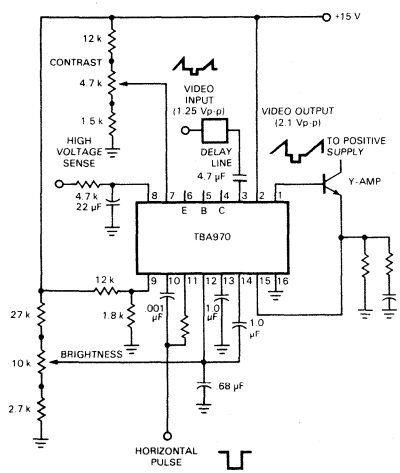
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, V+ = 15 V, See Test Circuit, unless otherwise specified

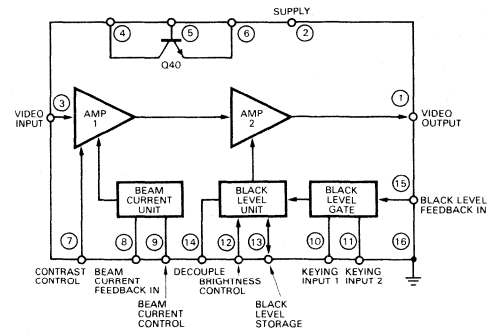
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_2)	(Note 1)		27	36	mA
Peak-to-Peak Input Voltage (V_3 p/p)	(Note 2)			1.6	Vp-p
Input Resistance (R_3)			12		kΩ
Voltage Gain			2.4		
3.0 dB Bandwidth			6.0		MHz
6.0 dB Bandwidth			9.0		MHz
Linearity of Black-to-White Video Output Signal		0.9			
Low Black Level Voltage (V_{15})				0.2	V
High Black Level Voltage (V_{15})		3.0			V
Contrast Control Range	$1.5\ V \leq V_7 \leq 4.5\ V$	36			dB
Input Resistance for Brightness Control (R12)			200		kΩ
Change of Black Level (ΔV_{15})	(Note 3)			20	mV
DC Voltage for Beam Current Limiting Inputs (V_8, V_9)	(Note 4)		2.0		V
Separate Transistor Q40 Gain	$I_C = I_4 = 1.0$ mA	40			

NOTES:
1. No input signal and at minimum brightness.
2. With negative going synchronizing pulse.
3. With constant brightness setting, due to change of picture content, contrast control setting and change in ambient temperature ($\Delta T_A = 20°C$); black level clamping with $t_c = 1\ \mu s$, $I_{10} \geq 0.25$ mA, $V_{11} \leq 0.3$ V.
4. Beam current limiting occurs at $V_8 \geq V_9$.

TEST CIRCUIT



BLOCK DIAGRAM



TBA990

PAL TV CHROMA DEMODULATOR

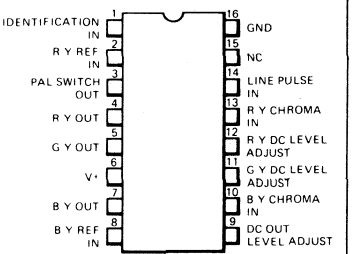
FAIRCHILD LINEAR INTEGRATED CIRCUIT

ENERAL DESCRIPTION – The TBA990 is an integrated color demodulator circuit for color elevision receivers incorporating two active synchronous demodulators for the R-Y and B-Y chromiance signals, a matrix (producing the G-Y color difference signal), PAL phase switch and flip-flop. is suitable for dc coupled drive to the picture tube. When associated with the matrix integrated rcuit (TBA530) it provides RGB output signals.

pecial attention has been given in the design to minimizing dc level drift with temperature and irect interface with TBA530, TBA540 and TBA560. It is constructed on a single silicon chip using ie Fairchild Planar* process.

DOUBLE BALANCED SYNCHRONOUS DEMODULATOR
INTERNAL DECODING MATRIX
INTERNAL PAL SWITCH
PROVISION FOR OUTPUT DC LEVEL MATCHING
MINIMIZED DC LEVEL DRIFT WITH TEMPERATURE
SIMULTANEOUS DC ADJUSTMENT ON CHROMA OUTPUTS

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

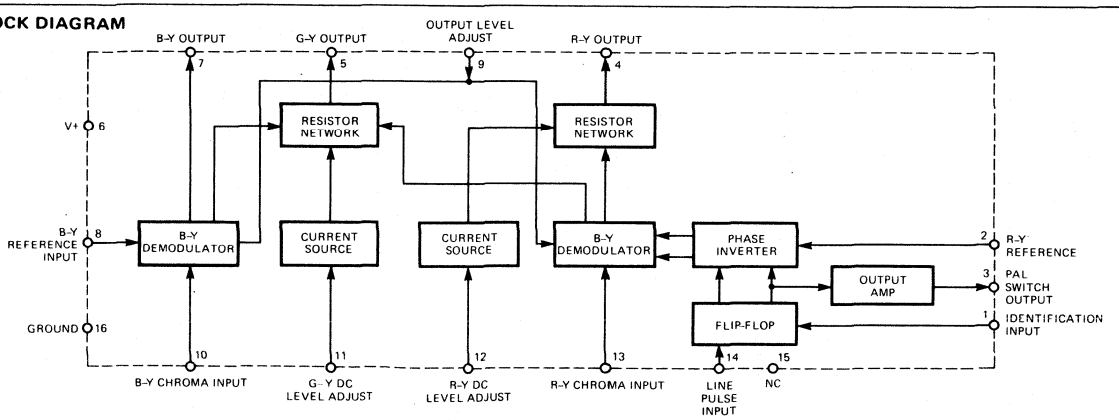
TYPE	PART NO.
990	TBA990
990Q	TBA990Q†

†Not recommended for new designs

BSOLUTE MAXIMUM RATINGS

Supply Voltage	13.2 V
Internal Power Dissipation	300 mW
Operating Ambient Temperature	−20°C to +60°C
Storage Temperature	−55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

BLOCK DIAGRAM



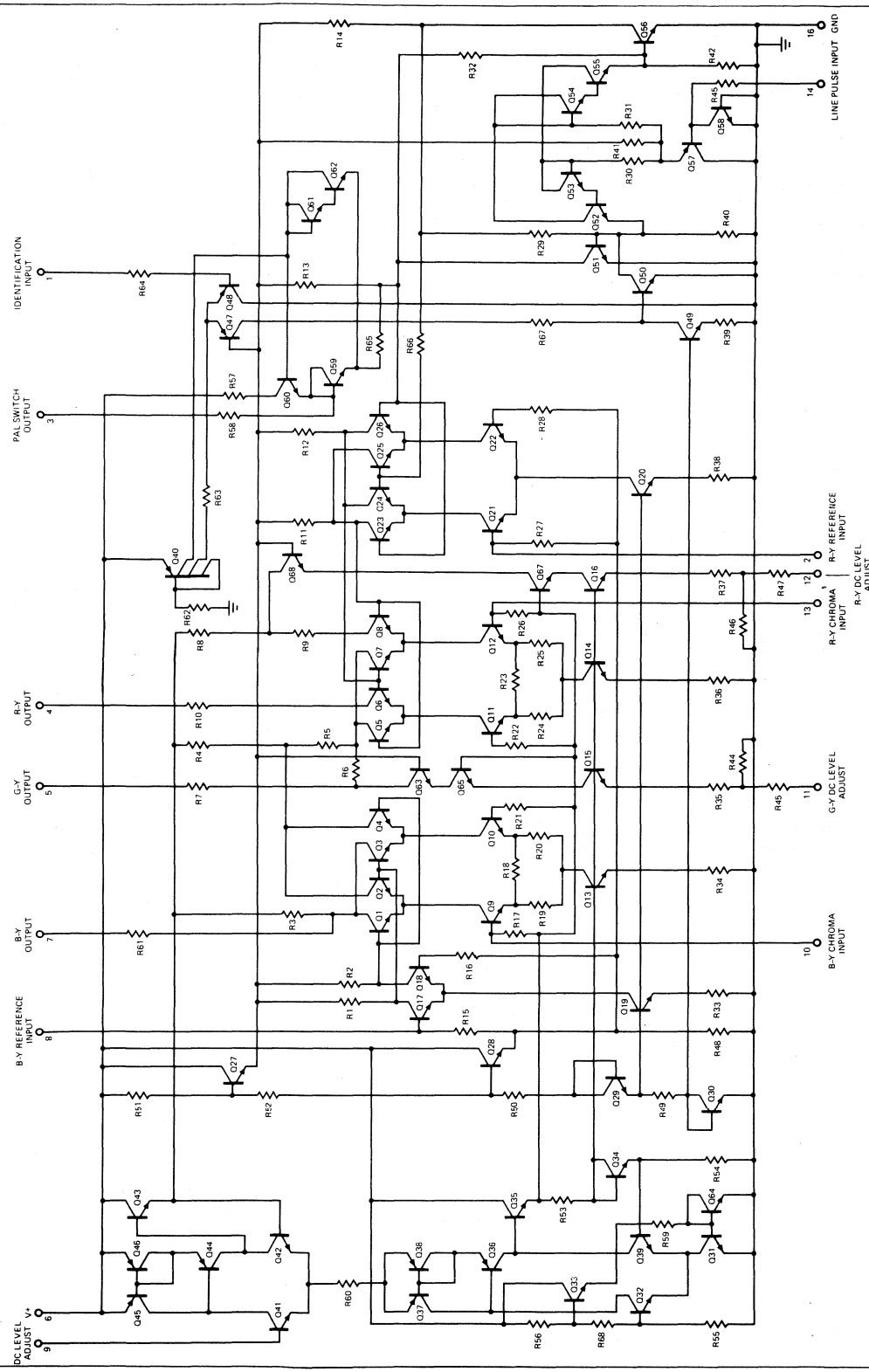
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_+ = 12V$, See Test Circuit, unless otherwise specified.

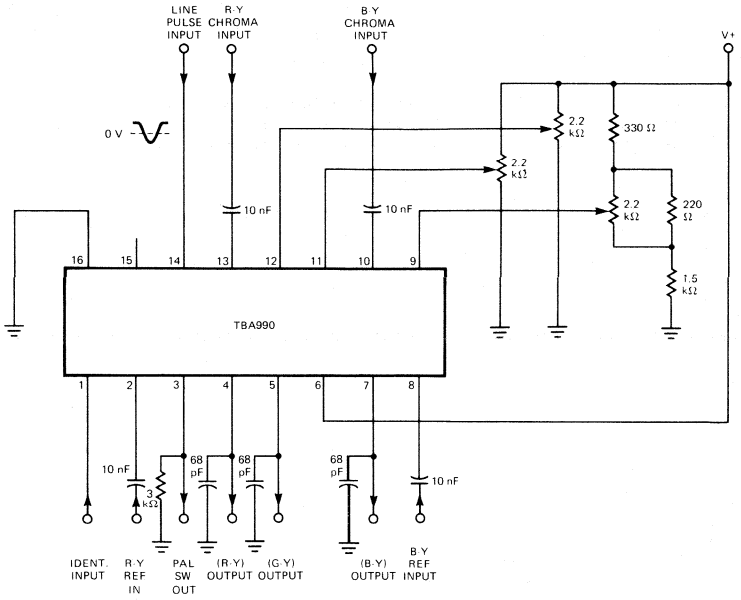
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_6)			17		mA
Color Difference Gain					
R-Y Channel ($A_{V4/13}$)	$V_{10} = V_{13} = 50$ mV pk-pk		3.8		V/V
B-Y Channel ($A_{V7/10}$)	f = 4.4 MHz		6.8		V/V
G-Y Channel	(Note 3)		(Note 1)		
Maximum Color Difference Output Voltage (Notes 2, 3)					
R-Y Output ($V_{4\ pk\text{-}pk}$)	(Notes 2, 3)	1.6			$V_{pk\text{-}pk}$
B-Y Output ($V_{7\ pk\text{-}pk}$)		2.0			$V_{pk\text{-}pk}$
G-Y Output ($V_{5\ pk\text{-}pk}$)		0.9			$V_{pk\text{-}pk}$
Color Difference DC Output Voltage					
R-Y Output (V_4)			7.5		V
B-Y Output (V_7)			7.5		V
G-Y Output (V_5)			7.5		V
Input Resistance of Chroma Inputs (R10, R13)	$V_{10} = V_{13} = 20$ mV rms (Sinusoidal) f = 4.4 MHz	800			Ω
Input Capacitance of Chroma Inputs (C10, C13)				10	pF
Output Resistance at Color Difference Terminals (R4, R5, R7)			3.0		kΩ
Input Resistance of Reference Inputs (R2, R8)			5.0		kΩ
Peak-to-Peak PAL Switch Output Voltage ($V_{3\ pk\text{-}pk}$)	(Note 4)		3.5		$V_{pk\text{-}pk}$
Activation Threshold Voltage (V_1)	Identification Circuit is Active	6.5			V
Deactivation Threshold Voltage (V_1)	Identification Circuit is Inactive			5.5	V
Identification Input Current (i_1)		−100			μA
Output Voltage Drift ($\Delta T_A = 40°C$)					
DC Output Voltage (V_4)	$V_{11} = V_{12} = 6$ V	−50		+50	mV
DC Output Voltage (V_7)		−50		+50	mV
DC Output Voltage (V_5)		−50		+50	mV
Relative DC Output Voltage Change between Channels		−20		+20	mV

NOTES:
1. G-Y output is typically equal to −0.51 (R-Y) −0.19 (B-Y).
2. Increase V_{10} and V_{13} until gain is equal to 0.7 of small signal gain.
3. Reference input ($V_{2\ pk\text{-}pk}$ and $V_{8\ pk\text{-}pk}$) range is 0.5 V to 2.0 V. (typically 1.0 V).
4. f_o = 0.5 x line pulse frequency; V_{14} = 2.0 to 5.0 $V_{pk\text{-}pk}$ (See application information).

EQUIVALENT CIRCUIT – TBA990



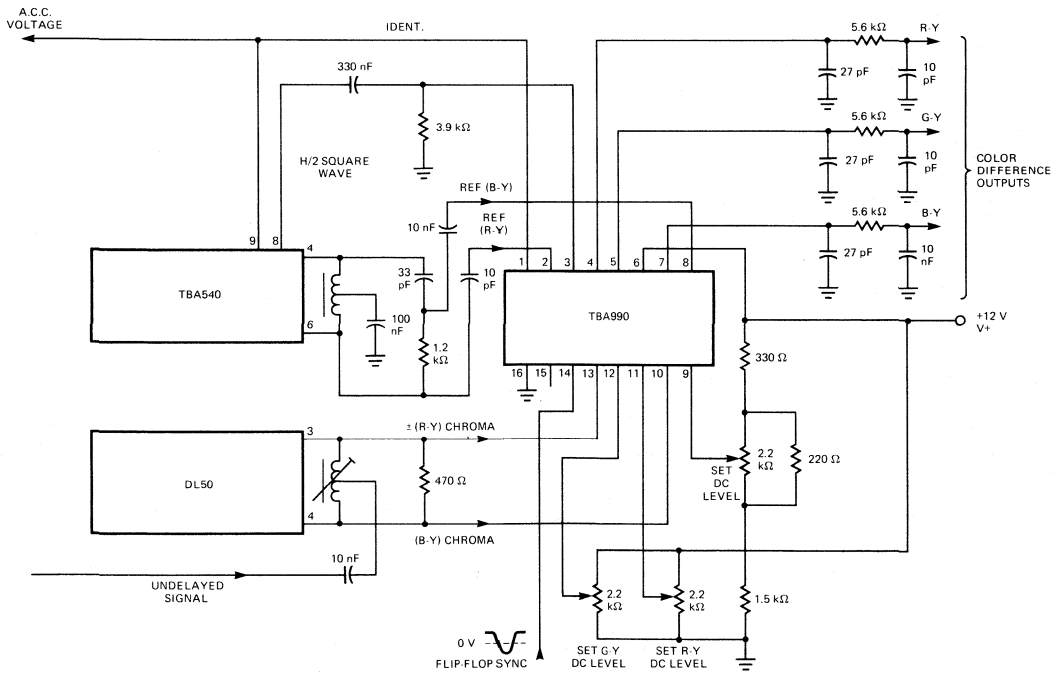
TEST CIRCUIT



$V_{11} = V_{12} = 6.0$ V

$V_9 = 9.5$ V

APPLICATION INFORMATION



APPLICATION INFORMATION (Cont'd)

The function is quoted against the corresponding lead number.

IDENTIFICATION BIAS

1. The PAL flip-flop is stopped, for identification purposes, when the voltage on pin 1 increases above 6 V. This threshold is internally generated and has a proportional behavior with the 12 V supply voltage. The threshold level of 6 V is chosen to match the output characteristic of the TBA540 and has sufficiently high safety margin above the zero chroma signal level of 4 V to eliminate spurious identifying.

R-Y SUBCARRIER REFERENCE INPUT

2. A 1 V pk-pk signal is required via a dc blocking capacitor. Under no circumstances should this signal be less than 0.5 V pk-pk. The input resistance at this pin is typically 5 kΩ.

PAL SQUARE WAVE CIRCUIT

3. The amplitude is 3.5 V pk-pk from an emitter follower.

R-Y SIGNAL OUTPUT (G-Y at pin 5 and B-Y at pin 7)

4. These outputs require no external dc loads except that direct connection must be made via the low pass filter to the appropriate pins on the RGB matrix TBA530.

   The signals produced are in the following ratios:

   $V_{B-Y} = 1.78\ V_{R-Y}$

   (a) $V_{G-Y} = 0.85\ V_{R-Y}$

   (b) $V_{G-Y} = 0.17\ V_{R-Y}$

   Condition (a) refers to (B-Y) + (R-Y) addition in the G-Y matrix.

   Condition (b) refers to the phase reversed (R-Y) input signal where (G-Y) is obtained by subtraction.

   The dc levels should each be adjusted, starting with the (B-Y), to +7.5 V at nominal supply voltage. However, in a complete circuit using the TBA530 matrix and feedback integrated circuit these dc levels will be adjusted to give the correct setting of the picture tube drive black levels. The changes in dc level with supply voltage are approximately linear and track together.

   The unwanted products of demodulation occurring in the color difference outputs are chiefly 8.86 MHz and harmonics together with a small amount of 4.43 MHz due to possible unbalance in the demodulators. To avoid possible troubles in the receiver because of the radiation of these demodulation products from the RGB drive circuits, filters must be employed in each of the color-difference outputs from the TBA990. The roll-off should begin at about 1.5 MHz and attention should be given to the parallel resonance of the inductors to ensure that no serious attenuation will occur at less than 1.5 MHz. Also, some advantage may be secured by designing the inductor so that the dip due to its self-resonance occurs at about 4.43 MHz.

G-Y SIGNAL OUTPUT

5. See pin 4.

POSITIVE SUPPLY

6. The maximum allowable voltage on this pin is 13.2 V.

B-Y SIGNAL OUTPUT

7. See pin 4.

B-Y SUBCARRIER REFERENCE INPUT

8. The requirements here are identical with those for pin 2.

DC LEVEL SETTING FOR B-Y OUTPUT SIGNAL

9. See test circuit diagram, and also pin 4.

CHROMINANCE B-Y INPUT SIGNAL

10. An input signal of approximately 360 mV pk-pk (color bars) is required at this pin. The input impedance is greater than 800 Ω and the input capacitance is less than 10 pF.

DC LEVEL SETTING FOR G-Y OUTPUT SIGNAL

11. See test circuit diagram, and also pin 5.

DC LEVEL SETTING FOR R-Y OUTPUT SIGNAL

12. See test circuit diagram, and also pin 4.

CHROMINANCE R-Y INPUT SIGNAL

13. An input signal of approximately 500 mV pk-pk (color bars) is required at this pin. The input imedpance is the same as for pin 10.

LINE PULSE INPUT (flip-flop synchronizing)

14. A waveform derived from the line timebase can be used for synchronizing providing that its amplitude lies between 2 V and 5 V pk-pk. The trigger point occurs where the negative going edge crosses approximately +0.6 V.

NOT CONNECTED

15. This pin should not be used for external connections.

GROUND

16. See pin 16.

TDA1170 • TDA1270

TV VERTICAL DEFLECTION SYSTEMS

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TDA1170 and TDA1270 are monolithic integrated circuits designed for use in TV vertical deflection systems. They are manufactured using the Fairchild Planar* process.

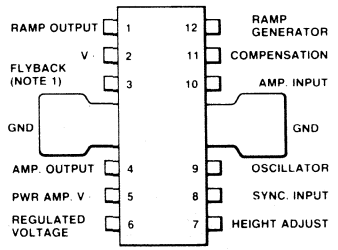
Both devices are supplied in the 12-pin plastic power package with the heat sink fins bent for insertion into the printed circuit board.

The TDA1170 is designed primarily for large and small screen black and white TV receivers and industrial TV monitors. The TDA1270 is designed primarily for driving complementary vertical deflection output stages in color TV receivers and industrial monitors.

- **VERTICAL OSCILLATOR**
- **VOLTAGE RAMP GENERATOR**
- **HIGH GAIN POWER AMPLIFIER**
- **FLYBACK GENERATOR (TDA1170)**

CONNECTION DIAGRAM
12-PIN POWER PACKAGE
(TOP VIEW)

PACKAGE OUTLINE 9W
PACKAGE CODE P3



ORDER INFORMATION

TYPE	PART NO.
1170 (P3)	TDA1170
1270 (P3)	TDA1270

NOTE:
Pin 3 is not used for the TDA1270 but is internally connected and must be left open.

*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS

	TDA1170	TDA1270	UNITS
Supply Voltage (Pin 2)	27	40	V
Supply Voltage (Pin 5)	–	40	V
Flyback Voltage (Pin 4 – Pin 5)	58	–	V
Voltage at Pin 4	–	41	V
Sync Input Voltage (Pin 8)	±12	±12	V
Power Amplifier Input Voltage	−0.5 to +10	−0.5 to +10	V
Output Peak Current (Non-Repetitive $t \leq 2$ ms)	2.0	2.0	A
Output Peak Current, f = 50 Hz, $t \leq 10\ \mu s$	2.5	2.5	A
Output Peak Current, f = 50 Hz, $t > 10\ \mu s$	1.5	1.5	A
Power Dissipation, T_{tab} = 90°C	5.0	5.0	W
Power Dissipation, T_A = 80°C (free air)	1.0	1.0	W
Storage Temperature Range	−40 to +150	−40 to +150	°C
Pin Temperature (Soldering 10 s)	260	260	°C

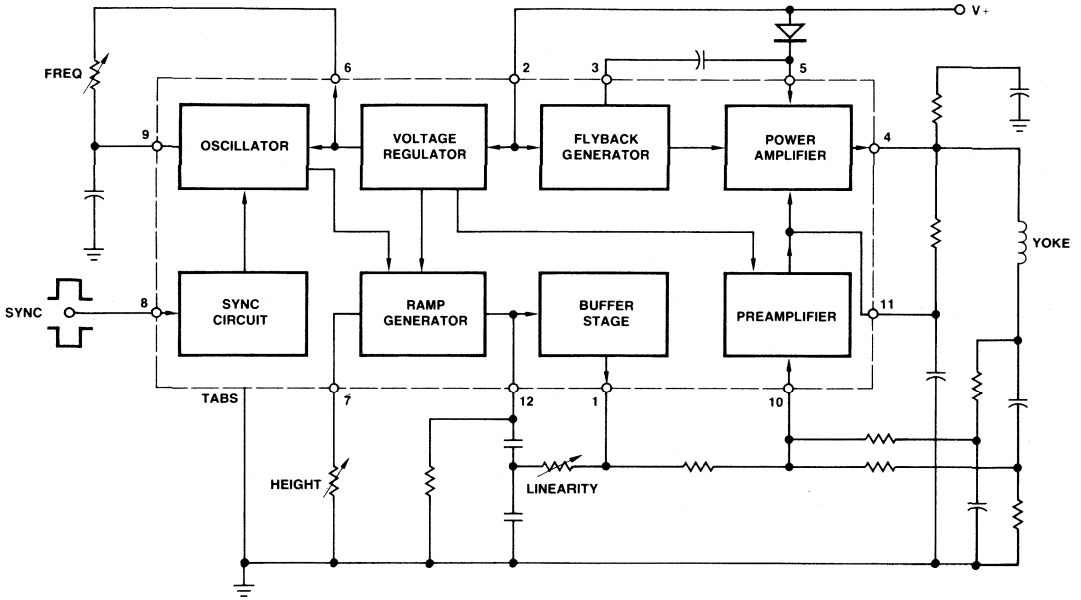
THERMAL DATA

$\theta_{J\text{-}C}$ Thermal Resistance Junction to Tab (max)	12°C/W
$\theta_{J\text{-}A}$ Thermal Resistance Junction to Ambient (max)	70°C/W†

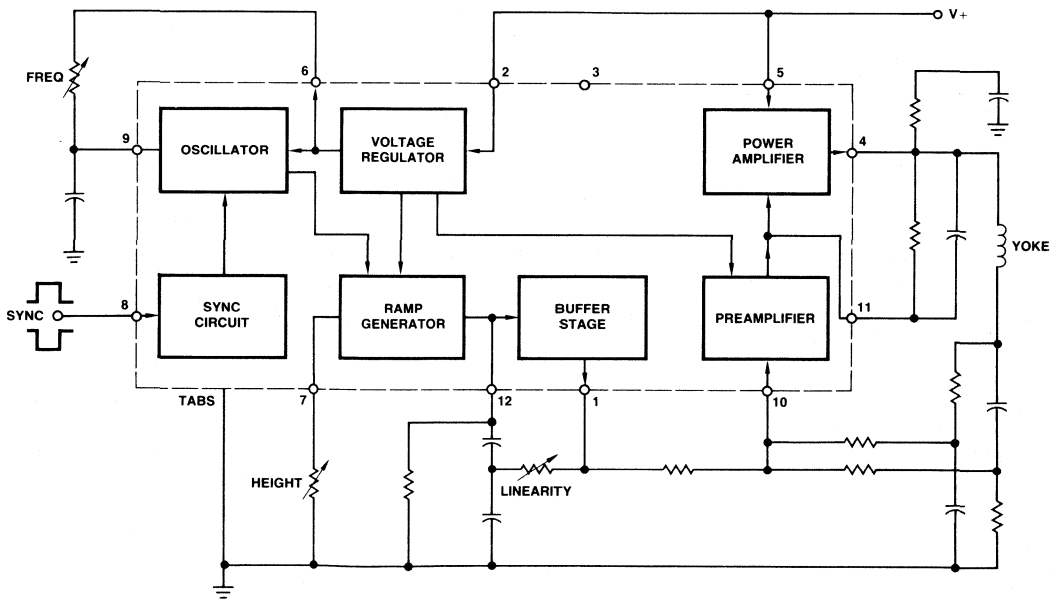
†Obtained with tabs soldered to printed circuit with minimized area.

BLOCK DIAGRAMS

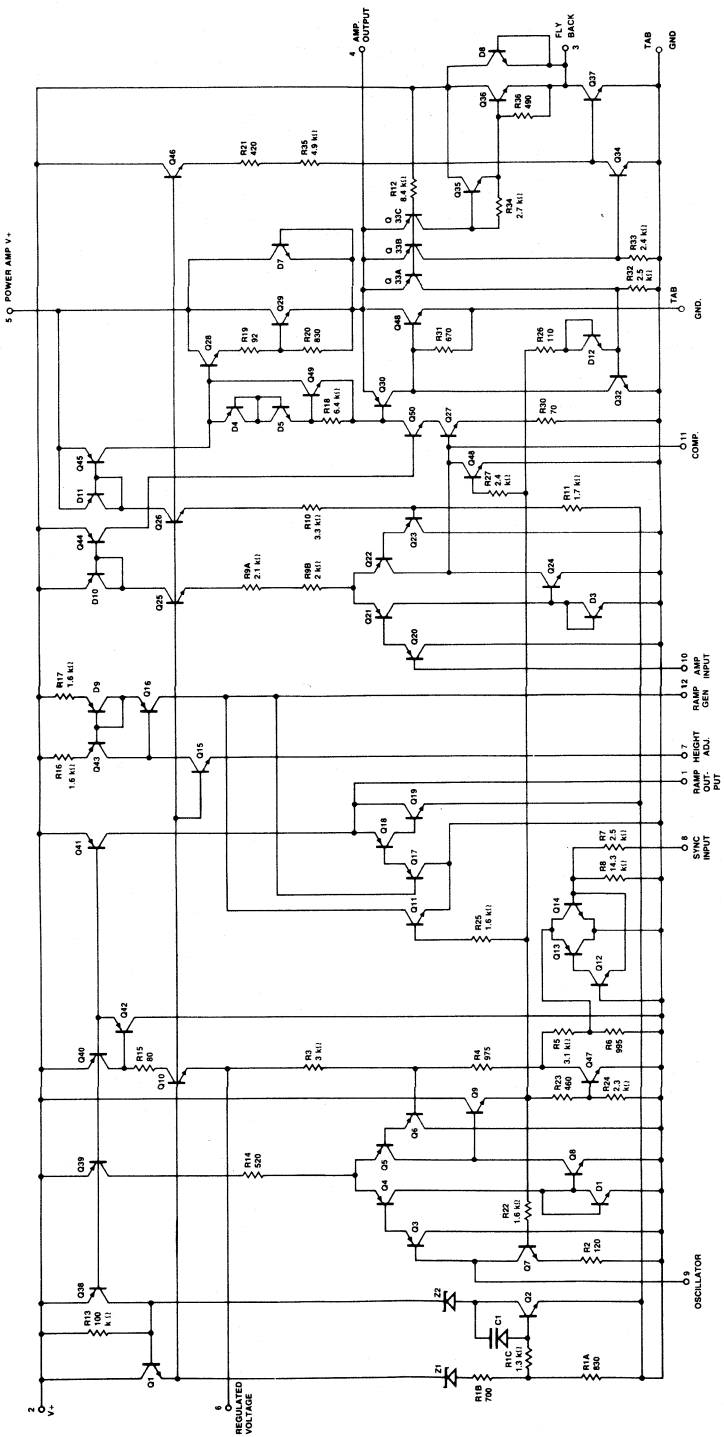
TDA1170



TDA1270

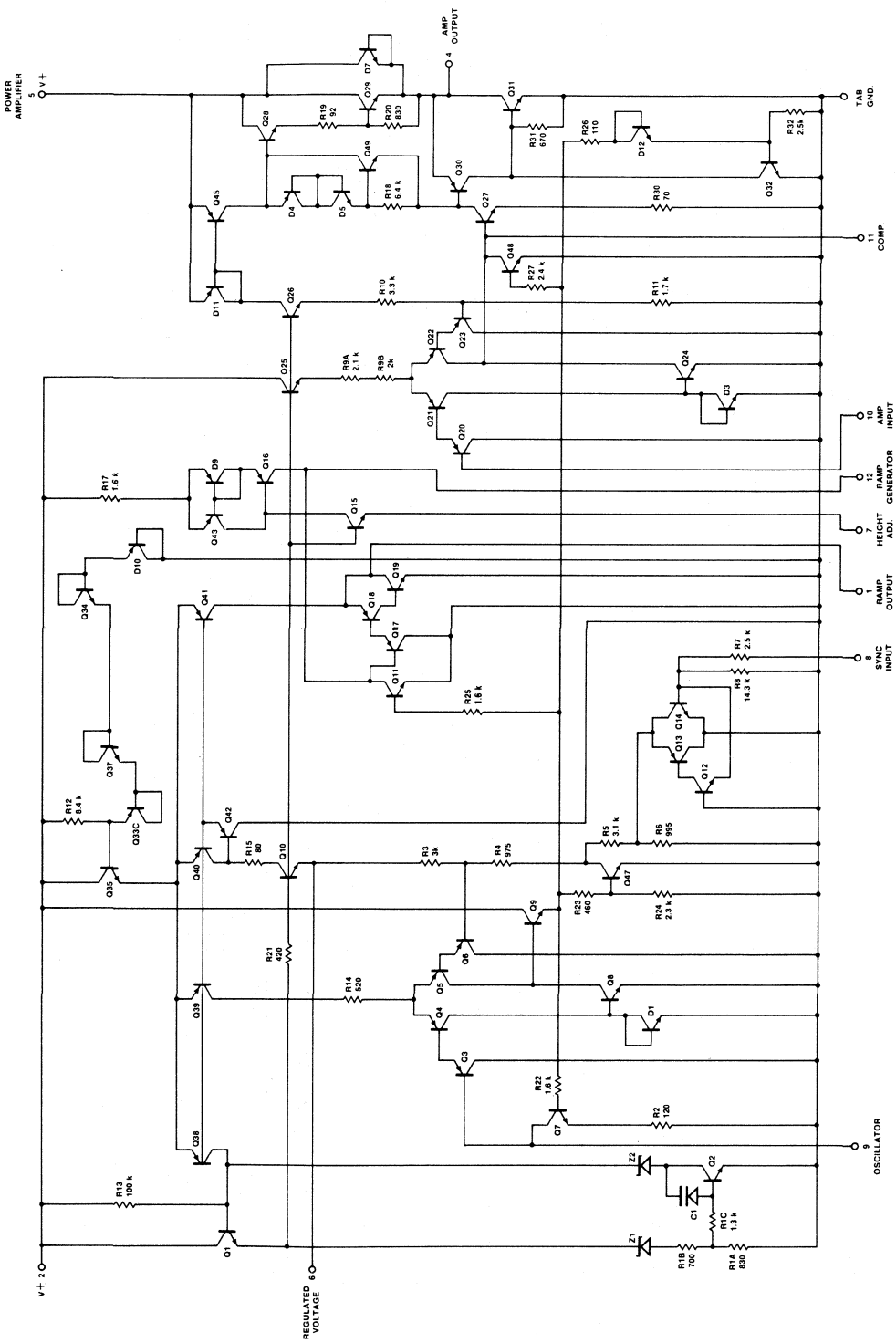


EQUIVALENT CIRCUIT



TDA1170

EQUIVALENT CIRCUIT



TDA1270

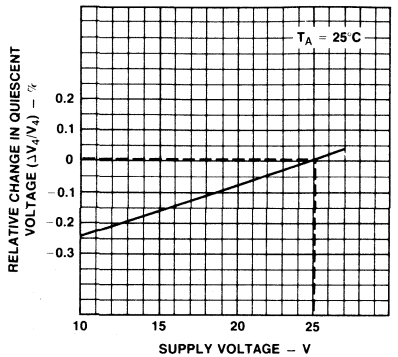
ELECTRICAL CHARACTERISTICS: (Refer to test circuits) $T_A = 25°C$; V+ = 25 V (TDA1170); V+ = 32 V (TDA1270) unless otherwise noted.

DC CHARACTERISTICS (Test Circuits – Figures 1a, 1b).

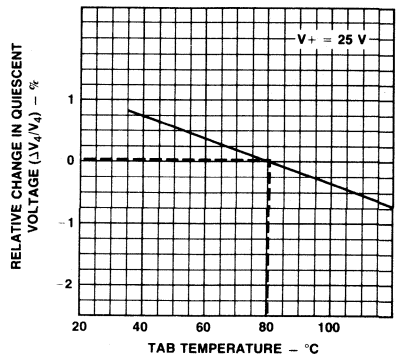
CHARACTERISTICS	CONDITIONS	TDA1170			TDA1270			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Bias Current	V_9 = 1 V		0.2	1.0		0.2	1.0	μA
Amplifier Input Bias Current	V_{10} = 1 V		0.15	1.0		0.15	1.0	μA
Ramp Generator Bias Current			0.05	0.5		0.05	0.5	μA
Supply Voltage		10			10			V
Quiescent Output Voltage	R2 = 10 kΩ V+ = 25 V, R1 = 30 kΩ V+ = 10 V, R1 = 10 kΩ	8.0 4.0	8.8 4.4	9.6 4.8				V V
Quiescent Output Voltage	R2 = 10 kΩ V+ = 32 V, R1 = 30 kΩ V+ = 10 V, R1 = 10 kΩ				8.0 4.0	8.8 4.4	9.6 4.8	V V
Regulated Voltage V_6, V_7		6.0	6.5	7.0	6.0	6.5	7.0	V
$\frac{\Delta V_6}{\Delta V+}$ $\frac{\Delta V_7}{\Delta V+}$ Line regulation	V+ = 10 to 27 V		1.5					mV/V
$\frac{\Delta V_6}{\Delta V+}$ $\frac{\Delta V_7}{\Delta V+}$ Line regulation	V+ = 10 to 40 V					1.5		mV/V
AC CHARACTERISTICS (Test Circuits – Figures 2a, 2b)								
Supply Current	I_Y = 0.5 A					70		mA
	I_Y = 1A		140					mA
Peak to Peak Yoke Current (Pin 4)				1.6			1.0	A
Flyback Voltage	I_Y = 1 A		51					V
Peak Sync. Input Voltage (Positive or Negative)		1.0			1.0			Vpk
Peak to Peak Oscillator Sawtooth Voltage			2.4			2.4		Vpk–pk
Sync. Input Resistance	V_8 = 1 V		3.5			3.5		kΩ
Flyback Time	I_Y = 1 A		0.6	0.8				
	I_Y = 0.5 A					0.7		ms
Pull-in Range (Below 50 Hz)			7.0			7.0		Hz
Oscillator Frequency Drift with Supply Voltage	V+ = 10 to 40 V V+ = 10 to 27 V		 0.01			0.01		$\frac{Hz}{V}$
Oscillator Frequency Drift with Tab Temperature	T_{tab} = 40 to 120°C		0.015			0.015		$\frac{Hz}{°C}$

TYPICAL PERFORMANCE CURVES – TDA1170

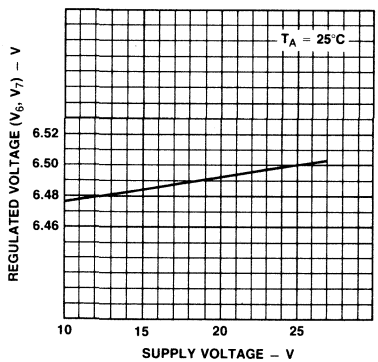
RELATIVE CHANGE IN QUIESCENT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



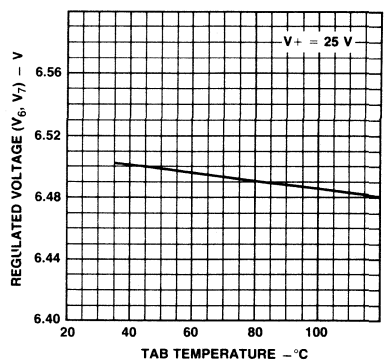
RELATIVE CHANGE IN QUIESCENT VOLTAGE AS A FUNCTION OF TAB TEMPERATURE



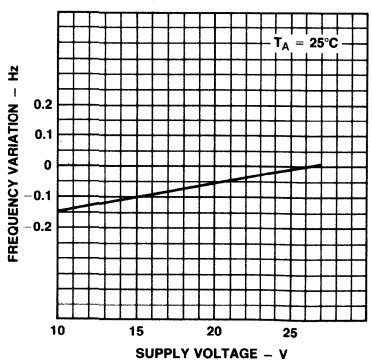
REGULATED VOLTAGE (V_6, V_7) AS A FUNCTION OF SUPPLY VOLTAGE



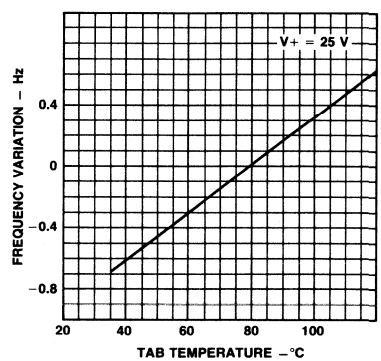
REGULATED VOLTAGE (V_6, V_7) AS A FUNCTION OF TAB TEMPERATURE



FREQUENCY VARIATION OF UNSYNCHRONIZED OSCILLATOR AS A FUNCTION OF SUPPLY VOLTAGE

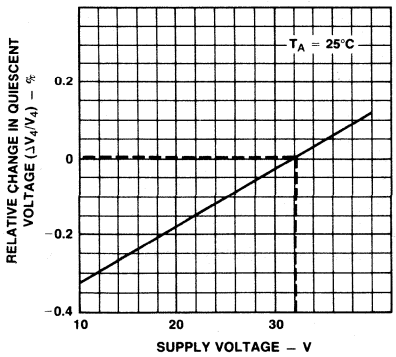


FREQUENCY VARIATION OF UNSYNCHRONIZED OSCILLATOR AS A FUNCTION OF TAB TEMPERATURE

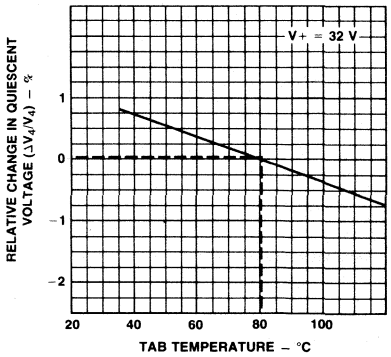


TYPICAL PERFORMANCE CURVES – TDA1270

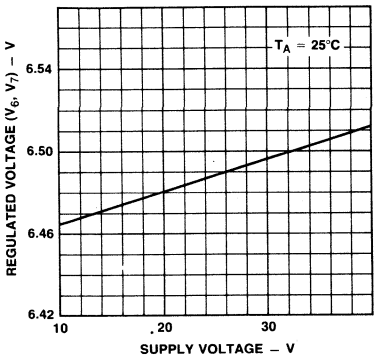
RELATIVE CHANGE IN QUIESCENT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



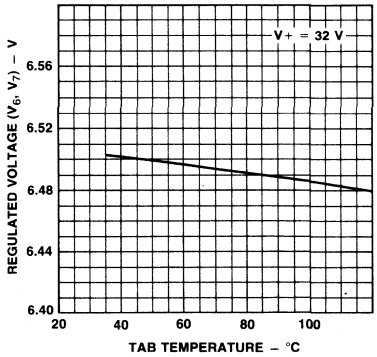
RELATIVE CHANGE IN QUIESCENT VOLTAGE AS A FUNCTION OF TAB TEMPERATURE



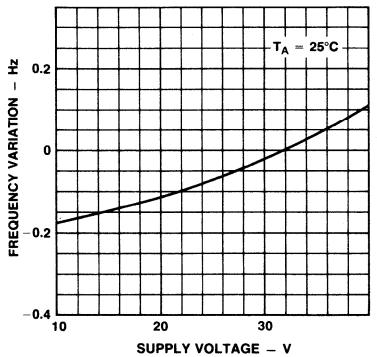
REGULATED VOLTAGE (V_6, V_7) AS A FUNCTION OF SUPPLY VOLTAGE



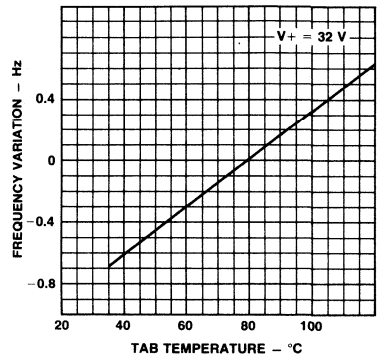
REGULATED VOLTAGE (V_6, V_7) AS A FUNCTION OF TAB TEMPERATURE



FREQUENCY VARIATION OF UNSYNCHRONIZED OSCILLATOR AS A FUNCTION OF SUPPLY VOLTAGE



FREQUENCY VARIATION OF UNSYNCHRONIZED OSCILLATOR AS A FUNCTION OF TAB TEMPERATURE



4

APPLICATION INFORMATION (TDA1170)

The vertical oscillator is directly synchronized by the sync pulses (positive or negative); therefore its free running frequency must be lower than the sync frequency. The use of current feedback causes the yoke current to be independent of yoke resistance variations due to thermal effects. Therefore no thermistor is required in series with the yoke. The flyback generator applies a voltage, about twice the supply voltage, to the yoke. This produces a short flyback time together with a high useful power to dissipated power ratio.

$$t_{fly} \cong \frac{2\,L_Y I_Y}{3V+}$$

where: L_Y = Yoke inductance (mH)
$V+$ = Supply Voltage (V)
I_Y = Peak to peak yoke current (A)

The supply current is : $I+ \cong \frac{I_Y}{8} + 0.02$

As can be seen, the supply current is independent of V+ and depends only on the yoke characteristics. The minimum value of V+ necessary for the required output current results in the maximum efficiency. The quiescent output voltage (pin 4) is fixed by the voltage feedback net network R7, R8, and R9 (Fig. 2a) according to:

$$V_4 = V_{10}\,\frac{R7 + R8 + R9}{R7}$$

The voltage on the inverting input of the amplifier (V_{10}) is $V_{10} \cong 2$ V. Typical application circuits are shown in Figures 3 and 4. A printed circuit board layout is shown in Figure 5.

TEST CIRCUITS

STATIC TEST CIRCUIT FOR MEASUREMENT OF $-I_9$, $-I_{12}$, AND V_4

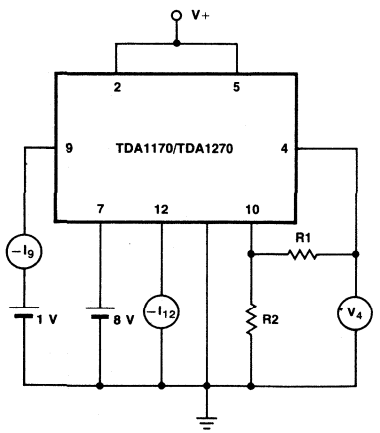


Fig. 1a

STATIC TEST CIRCUIT FOR MEASUREMENT OF $-I_{10}$, V_6, V_7, $\Delta V_6/\Delta V+$ AND $\Delta V_7/\Delta V+$

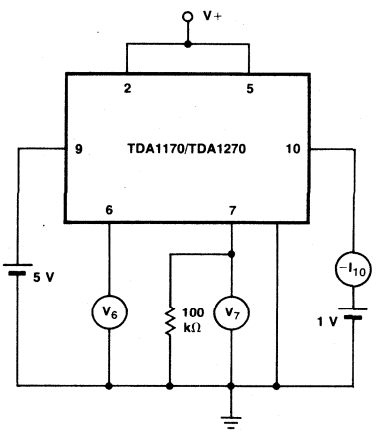


Fig. 1b

DYNAMIC TEST CIRCUIT FOR TDA1170

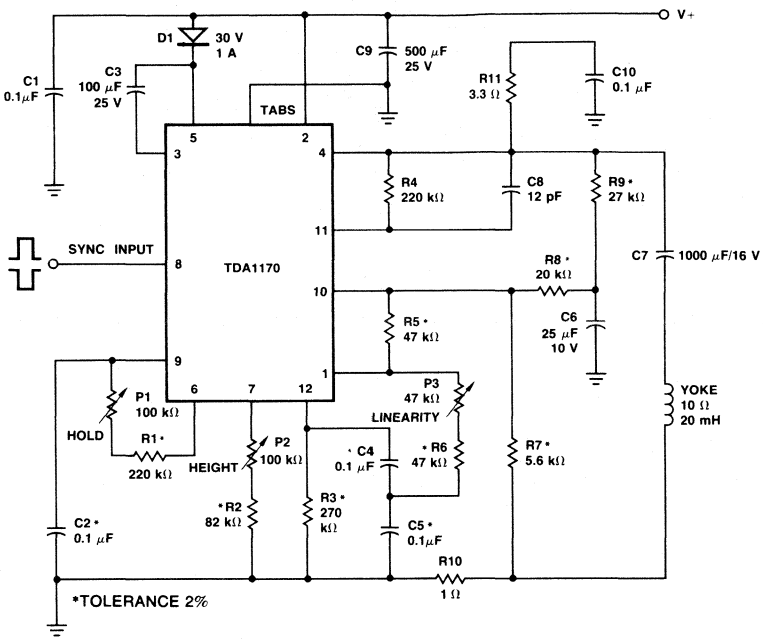


Fig. 2a

DYNAMIC TEST CIRCUIT FOR TDA1270.

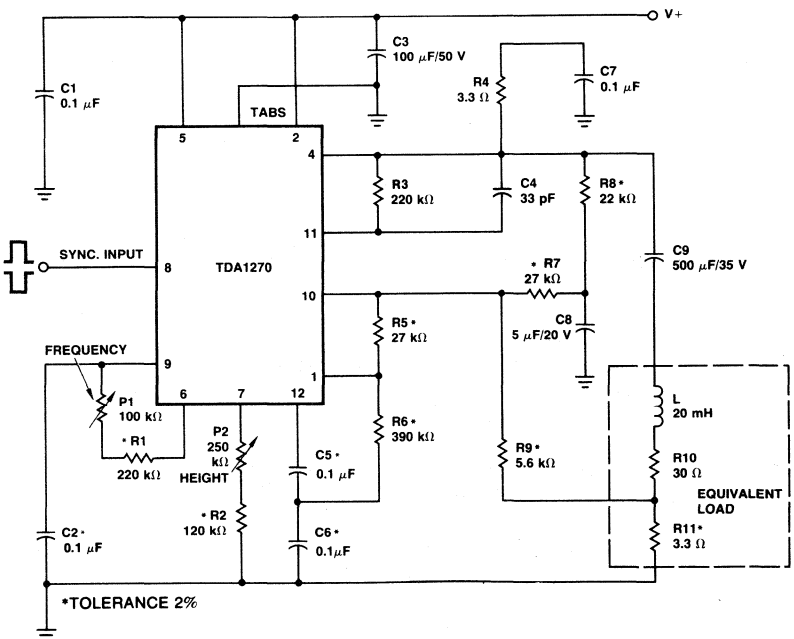


Fig. 2b

TYPICAL APPLICATION CIRCUIT FOR B & W 24" 110° TV SETS

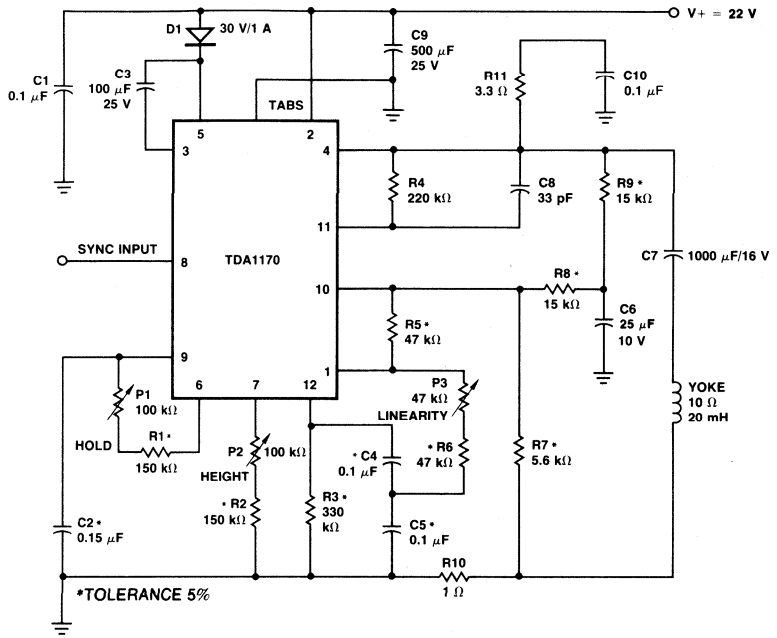


Fig. 3

Typical performance of circuit in Fig. 3 ($V+ = 22$ V; $I_Y = 1$ A; $R_Y = 10\ \Omega$; $L_Y = 20$ mH)

$I+$	Supply current	140	mA
t_{fly}	Flyback time	0.75	ms
I_Y	Maximum scanning current (peak to peak)	1.2	A
$V+$	Operating supply voltage	20 to 24	V
P_D	TDA1170 power dissipation	2.2	W

For safe working up to $T_A = 50°C$ a heatsink of $\theta = 40°C/W$ is required and each tab of the TDA1170 must be soldered to 1 cm^2 copper area of the printed circuit board.

TYPICAL APPLICATION CIRCUIT FOR B & W SMALL SCREEN TV SETS.

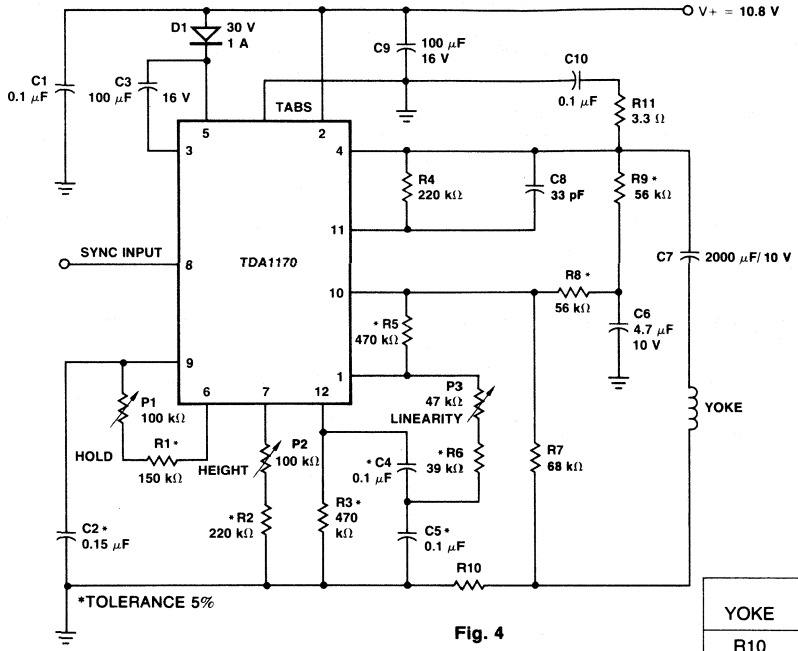


Fig. 4

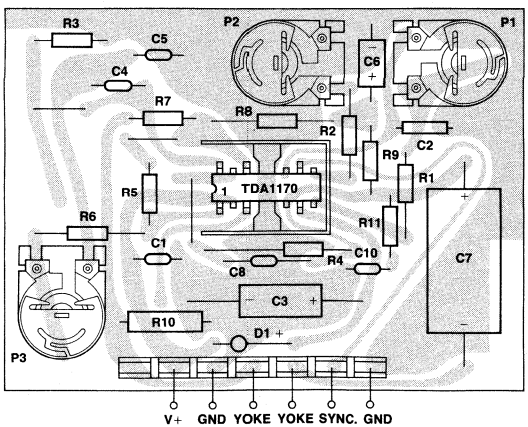
	7.5	4.7	mH
YOKE	4	2.5	Ω
R10	0.5	0.33	Ω

Typical performance of circuit in Fig. 4 ($V+ = 10.8$ V; $I_Y = 1$ A; $R_Y = 4\ \Omega$; $L_Y = 7.5$ mH)

$I+$	Supply current	150	mA
t_{fly}	Flyback time	0.7	ms
I_Y	Maximum scanning current (peak to peak)	1.15	A
$V+$	Operating supply voltage	10.8	V
P_D	TDA1170 power dissipation	1.3	W

For safe working up to $T_A = 50°C$ a heatsink of $\theta = 30°C/W$ is required and each tab of the TDA1170 must be soldered to 1 cm^2 copper area of the printed circuit board.

PC BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 3 AND FIG. 4 (1:1 SCALE)



C9 is not mounted on the PC board.

Fig. 5

APPLICATIONS INFORMATION (TDA1270)

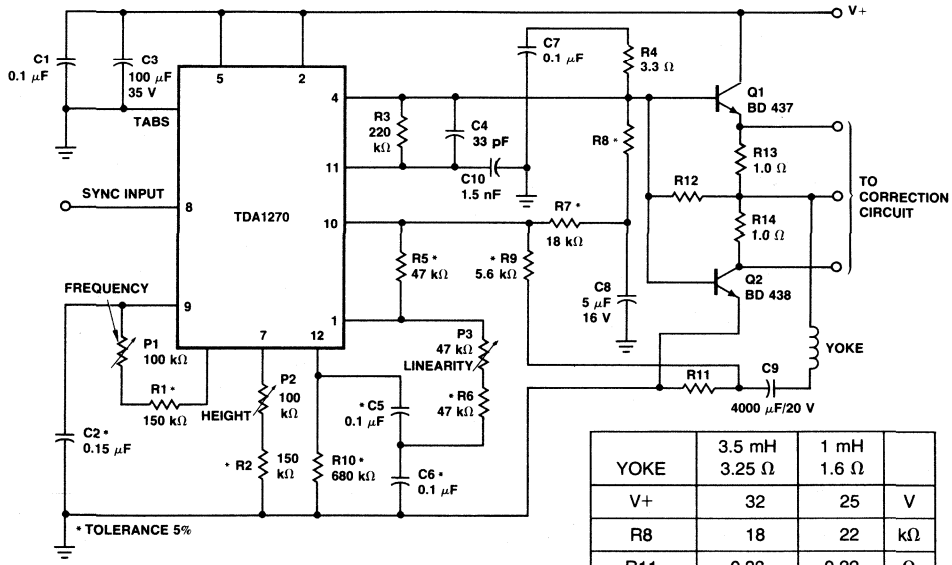
The high current capability of the TDA1270 allows low current gain transistors to be used in driving low impedance yokes. The oscillator is directly synchronized by the sync pulses; therefore its free frequency must be lower than the sync. frequency. The sync. input (pin 8) can be driven by positive or negative pulses.

The quiescent output voltage (V_4) is fixed by the voltage feedback network, R7, R8, and R9 (Fig. 6) according to:

$$V_4 = V_{10} \frac{R7 + R8 + R9}{R9}$$

The voltage on the inverting input of the amplifier, V_{10}, is $V_{10} \cong 2$ V. Typical application circuits are shown in Fig. 6, 8, 10. Printed circuit board layouts are shown in Fig. 7 and 9.

TYPICAL APPLICATION CIRCUIT FOR LARGE SCREEN COLOR TV SETS



YOKE	3.5 mH 3.25 Ω	1 mH 1.6 Ω	
V+	32	25	V
R8	18	22	kΩ
R11	0.33	0.22	Ω
R12	10	5.6	Ω

Fig. 6

		YOKE	
		3.5 mH 3.25 Ω	1 mH 1.6 Ω
I_+	Supply Current	0.5 A	0.8 A
t_{fly}	Flyback Time	0.7 ms	0.6 ms
I_Y	Maximum Scanning Current (Peak to Peak)	4 A	7.5 A
V_+	Operating Supply Voltage	28 to 36 V	23 to 27 V
P_T	TDA1270 Power Dissipation	1.5 W	2.0 W
P_T	Output Transistors Power Dissipation	11 W	13 W
$\theta_{tab\text{-}amb}$	Heatsink θ Required for TDA1270	35°C/W	30°C/W
$\theta_{case\text{-}amb}$	θ of Output Transistors Heatsink (Total)	6°C/W	5°C/W

Stable continous operation is ensured up to an ambient temperature of 55°C

PC BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 6 (1:1 SCALE)

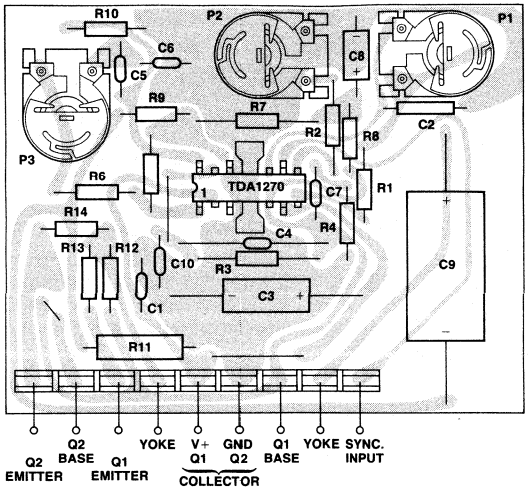


Fig. 7

TYPICAL APPLICATION CIRCUIT FOR 12" TO 17" (110°, 20 mm NECK) B & W TV SET.

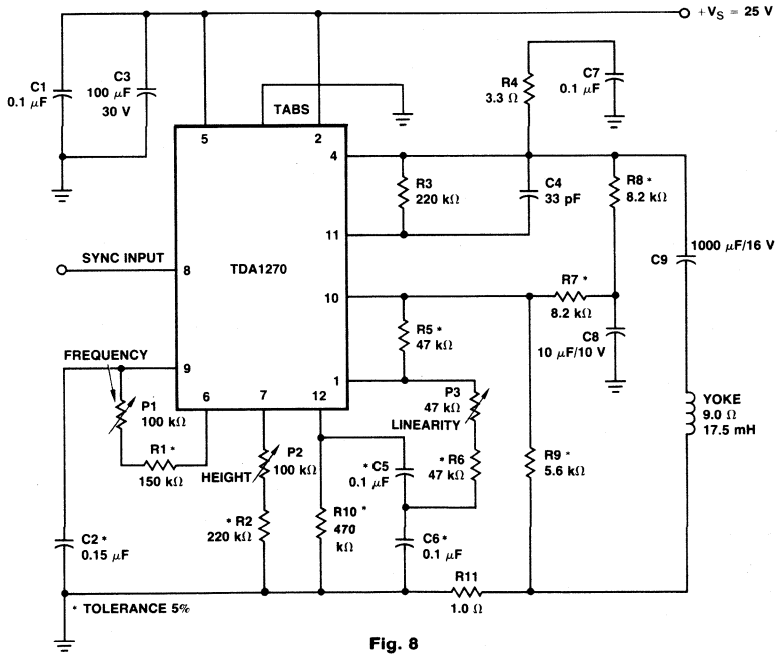


Fig. 8

Typical Performance of Circuit in Fig. 8

I_+	Supply Current	110	mA
t_{fly}	Flyback Time	0.8	ms
I_Y	Maximum Scanning Current (Peak to Peak)	0.9	A
V+	Operating Supply Voltage	23 to 27	V
P_T	TDA1270 Power Dissipation	2.4	W

For safe working up to $T_A = 50°C$ a heatsink of $\theta = 30°C/W$ is required and each tab of the TDA1270 must be soldered to 1 cm^2 copper area of the printed circuit board.

PC BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 8 (1:1 SCALE)

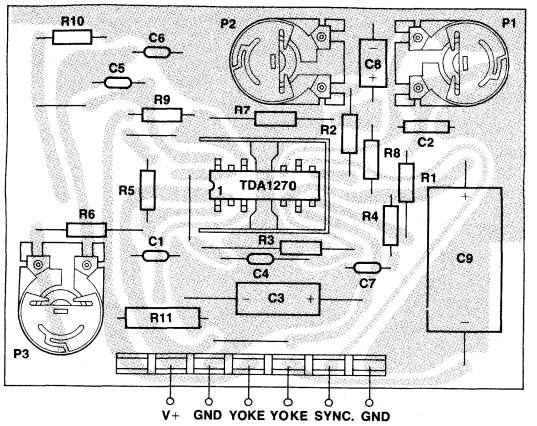
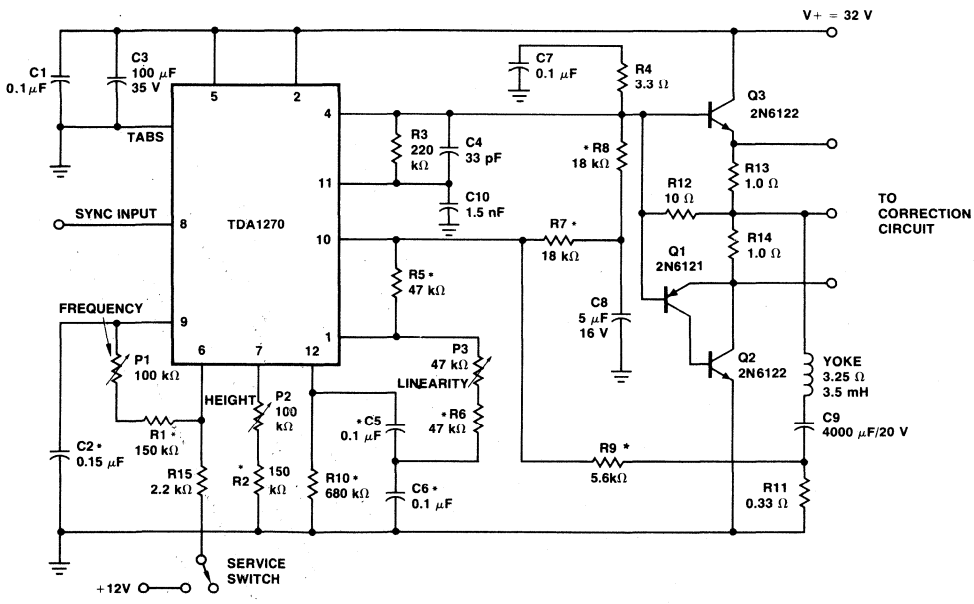


Fig. 9

Fig. 10 shows an output stage employing two NPN power transistors and a service switch that stops the vertical deflection during covergence adjustment.

VERTICAL DEFLECTION CIRCUIT EMPLOYING TWO NPN POWER OUTPUT TRANSISTORS.



• TOLERANCE 5%

Fig. 10

MOUNTING INSTRUCTIONS

The junction to ambient thermal resistance of the TDA1170 and TDA1270 can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (Fig. 12) or to an external heatsink (Fig. 13).

The diagram of Fig. 14 shows the maximum dissipable power P_D and the θ_{J-A} as a function of the side "L" to two equal square copper areas having a thickness of 35 μ (1.4 mil). During soldering, the tab temperature must not exceed 250°C and the soldering time must not be longer than 10 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

EXAMPLE OF P.C. BOARD COPPER AREA USED AS HEATSINK

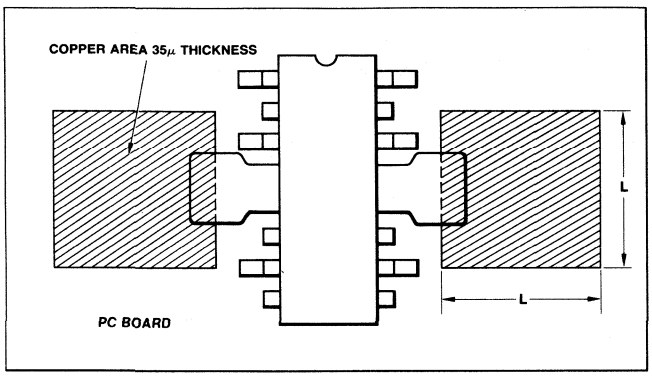


Fig. 12

EXAMPLE OF CIRCUIT WITH ETERNAL HEATSINK

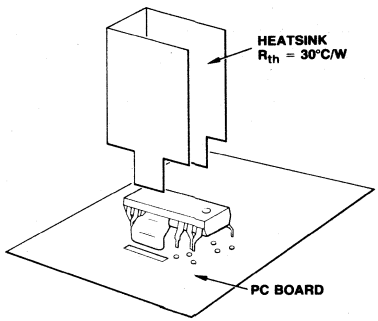


Fig. 13

MAXIMUM POWER DISSIPATION AND THERMAL RESISTANCE AS A FUNCTION OF COPPER LENGTH (L)

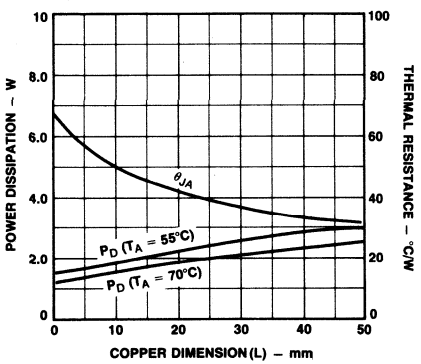


Fig. 14

MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

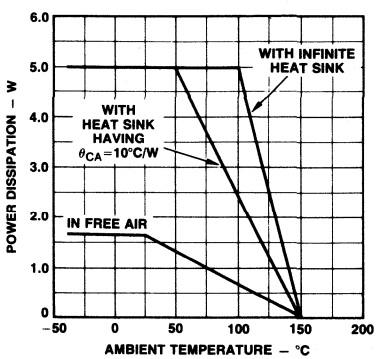


Fig. 15

TDA1190 • TDA1190Z

ONE CHIP TV SOUND SYSTEM

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The TDA1190 and TDA1190Z are silicon monolithic integrated circuits in 12-pin plastic power packages. They perform all the functions needed for TV sound systems, including IF limiter-amplifier, FM detector, AF preamplifier and power output stage. The TDA1190 is specified for 5.5 MHz (PAL) sound systems and the TDA1190Z is specified for 4.5 MHz (NTSC) sound systems. They are constructed using the Fairchild Planar* epitaxial process.

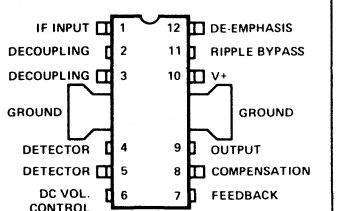
They provide an output power of 4.2 W into a 16 Ω load at V+ = 24 V, or 1.5 W into an 8.0 Ω load at V+ = 12 V. This performance, together with the FM-IF section characteristics of high sensitivity, high AM rejection and low distortion, enables them to be used in almost every type of television receiver. No external shielding is needed.

The basic differences between the TDA1190 and TDA1190Z are:

The TDA1190Z is designed for a larger volume control potentiometer (22 kΩ vs 2.2 kΩ). The TDA1190 includes one of the gain adjust resistors on the chip, while in the TDA1190Z both are required in the external circuitry.

- **DC VOLUME CONTROL**
- **ACTIVE LOW PASS FILTER**
- **OUTPUT POWER 4.2 W (24 V – 16 Ω)**
- **HIGH SENSITIVITY**
- **EXCELLENT AM REJECTION**

CONNECTION DIAGRAM
12-PIN POWER PACKAGE
(TOP VIEW)
PACKAGE OUTLINE 9W
PACKAGE CODE P3



ORDER INFORMATION

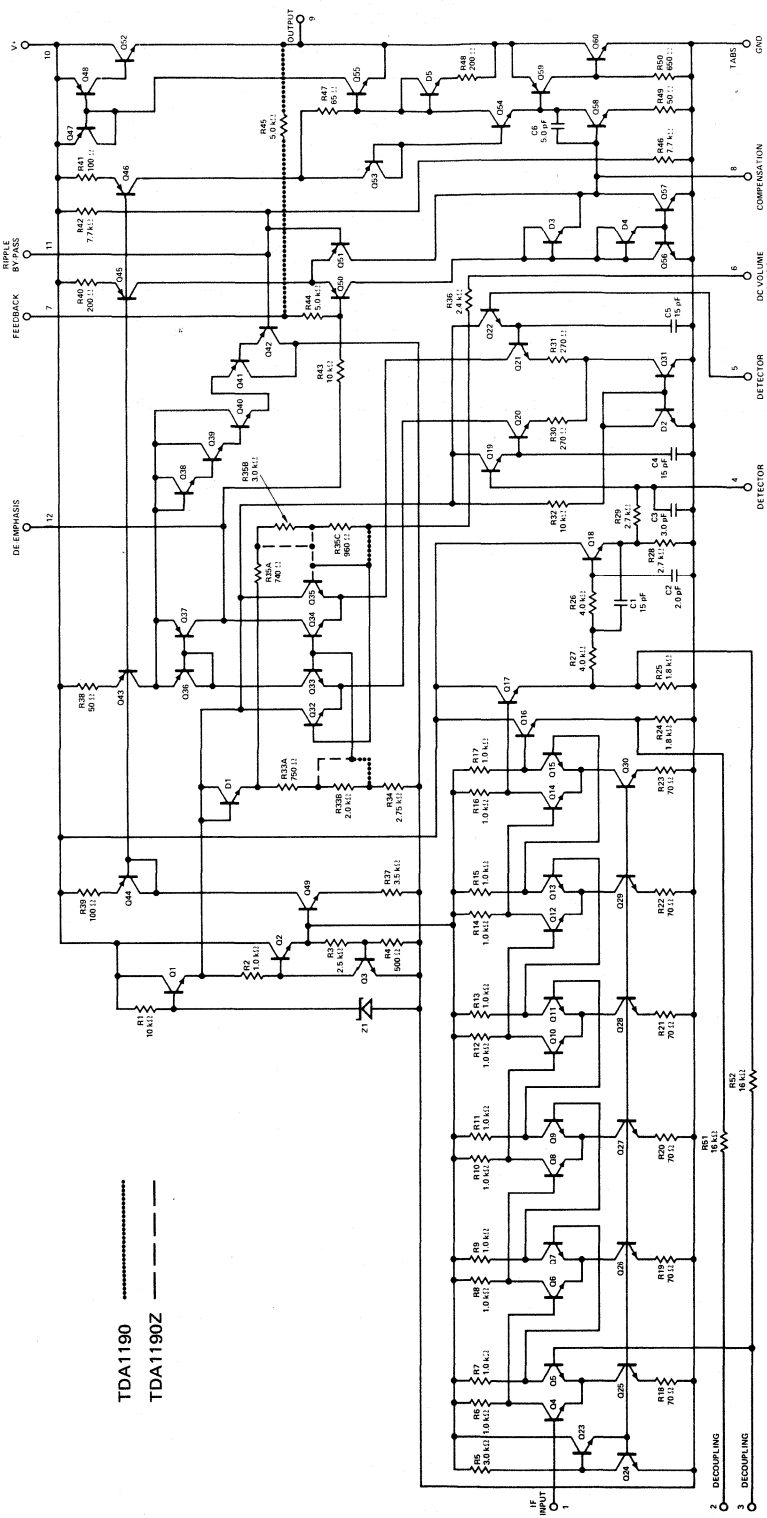
TYPE	PART NO.
1190	TDA1190
1190Z	TDA1190Z

ABSOLUTE MAXIMUM RATINGS

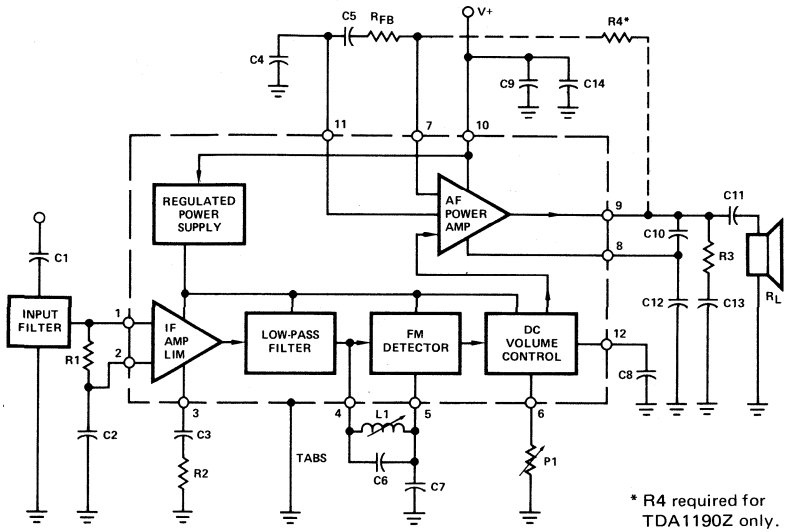
Supply Voltage	28 V
Input Signal Voltage	1.0 V
Output Peak Current (Non-repetitive)	2.0 A
Output Peak Current (Repetitive)	1.5 A
Power Dissipation: at T_{tab} = 90°C	5.0 W
at T_A = 80°C (Free Air)	1.0 W
Storage and Junction Temperature	−40°C to +150°C
Pin Temperature (Soldering, 10 s)	260°C

*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



BLOCK DIAGRAM



TDA1190

ELECTRICAL CHARACTERISTICS: See Test Circuits

$V+ = 24$ V, $T_A = 25°C$ unless otherwise specified.

CHARACTERISTICS	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (Pin 10)			9.0		28	V
Quiescent Output Voltage (Pin 9)	V+ = 24 V		11	12	13	V
	V+ = 12 V		5.5	6.0	6.5	V
Quiescent Drain Current	P1 = 2.2 kΩ	V+ = 24 V		22	35	mA
		V+ = 12 V		19	31	mA
Output Power	THD = 10%, f_o = 5.5 MHz,	V+ = 24 V, R_L = 16 Ω	3.0	4.2		W
	f_m = 1.0 kHz, Δf = ±25 kHz	V+ = 12 V, R_L = 8.0 Ω		1.5		W
Output Power	THD = 2%, f_o = 5.5 MHz,	V+ = 24 V, R_L = 16 Ω		3.4		W
	f_m = 1.0 kHz, Δf = ±25 kHz	V+ = 12 V, R_L = 8.0 Ω		1.4		W
Input Limiting Voltage (−3.0 dB) at Pin 1	f_o = 5.5 MHz, f_m = 1.0 kHz, Δf = ±7.5 kHz, P1 = 0			30		μV
Distortion	P_o = 50 mW, f_o = 5.5 MHz,	V+ = 24 V, R_L = 16 Ω		0.55		%
	f_m = 1.0 kHz, Δf = ±7.5 kHz	V+ = 12 V, R_L = 8.0 Ω		0.65		%
Frequency Response of Audio Amplifier (−3.0 dB)	R_L = 16 Ω, C10 = 200 pF,	R_{FB} = 18 Ω		50 to 12,000		Hz
	C12 = 1000 pF, P1 = 220 pF,	R_{FB} = 10 Ω		50 to 9,100		Hz
Recovered Audio Voltage (Pin 12)	V_{IN} ≥ 1.0 mV, f_o = 5.5 MHz, f_m = 1.0 kHz, Δf = ±7.5 kHz, P1 = 0			60		mV
Amplitude Modulation Rejection	V_{IN} ≥ 1.0 mV, f_o = 5.5 MHz, f_m = 1.0 kHz, Δf = ±50 kHz, m = 0.3			55		dB
Signal and Noise to Noise Ratio	V_{IN} ≥ 1.0 mV, V_o = 4.0 V, f_o = 5.5 MHz, f_m = 1.0 kHz, Δf = ±50 kHz			70		dB
Feedback Resistance (Between Pins 7 and 9)	Internal Resistor		3.5	5.0	6.5	kΩ
Input Resistance (Pin 1)	V_{IN} = 1.0 mV, f_o = 5.5 MHz			30		kΩ
Input Capacitance (Pin 1)				5.0		pF
Supply Voltage Rejection Ratio	R_L = 4.0 Ω, f_{ripple} = 100 Hz, P1 = 2.2 kΩ			46		dB
DC Volume Control Attenuation	P1 = 2.2 kΩ			90		dB

TDA1190Z

ELECTRICAL CHARACTERISTICS: See Test Circuits

$V+ = 24$ V, $T_A = 25°C$ unless otherwise specified.

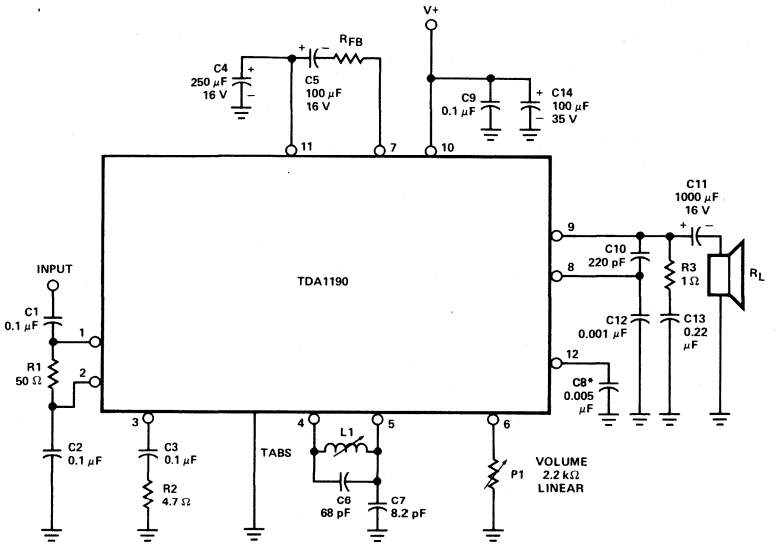
CHARACTERISTICS	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (Pin 10)			9.0		28	V
Quiescent Output Voltage (Pin 9)	$V+ = 24$ V		11	12	13	V
	$V+ = 12$ V		5.1	6.0	6.9	V
Quiescent Drain Current	P1 = 22 kΩ	$V+ = 24$ V	11	22	35	mA
		$V+ = 12$ V		19		mA
Output Power	THD = 10%, $f_o = 4.5$ MHz,	$V+ = 24$ V, $R_L = 16$ Ω		4.2		W
	$f_m = 400$ Hz, $\Delta f = \pm 25$ kHz	$V+ = 12$ V, $R_L = 8.0$ Ω		1.5		W
Output Power	THD = 2%, $f_o = 4.5$ MHz,	$V+ = 24$ V, $R_L = 16$ Ω		3.5		W
	$f_m = 400$ Hz, $\Delta f = \pm 25$ kHz	$V+ = 12$ V, $R_L = 8.0$ Ω		1.4		W
Input Limiting Voltage (−3.0 dB) at Pin 1	$f_o = 4.5$ MHz, $f_m = 400$ Hz, $\Delta f = \pm 7.5$ kHz, P1 = 0			40	100	μV
Distortion	$P_o = 50$ mW, $f_o = 4.5$ MHz,	$V+ = 24$ V, $R_L = 16$ Ω		0.75		%
	$f_m = 400$ Hz, $\Delta f = \pm 7.5$ kHz	$V+ = 12$ V, $R_L = 8.0$ Ω		1.0		%
Frequency Response of Audio Amplifier (−3.0 dB)	$R_L = 16$ Ω, C10 = 120 pF,	$R_{FB} = 82$ Ω		70 to 12,000		Hz
	C12 = 470 pF, P1 = 22 kΩ	$R_{FB} = 47$ Ω		70 to 7,000		Hz
Recovered Audio Voltage (Pin 12)	$V_{IN} \geq 1.0$ mV, $f_o = 4.5$ MHz, $f_m = 400$ Hz, $\Delta f = \pm 7.5$ kHz, P1 = 0			120		mV
Amplitude Modulation Rejection	$V_{IN} \geq 1.0$ mV, $f_o = 4.5$ MHz, $f_m = 400$ Hz, $\Delta f = \pm 25$ kHz, m = 0.3			55		dB
Signal and Noise to Noise Ratio	$V_{IN} \geq 1.0$ mV, $V_o = 4.0$ V, $f_o = 4.5$ MHz, $f_m = 400$ Hz, $\Delta f = \pm 25$ kHz		50	65		dB
Feedback Resistance (Between Pins 7 and 9)	External Resistor			22		kΩ
Input Resistance (Pin 1)	$V_{IN} = 1.0$ mV, $f_o = 4.5$ MHz			30		kΩ
Input Capacitance (Pin 1)				5.0		pF
Supply Voltage Rejection Ratio	$R_L = 4.0$ Ω, $f_{ripple} = 100$ Hz, P1 = 22 kΩ			46		dB
DC Volume Control Attenuation	P1 = 12 kΩ			90		dB

PACKAGE THERMAL RESISTANCE

θ_{j-tab}	Thermal resistance junction-tab	max	12	°C/W
θ_{j-amb}	Thermal resistance junction-ambient	max	70*	°C/W

*With tabs soldered to printed circuit with minimized copper area.

TEST CIRCUIT – TDA1190

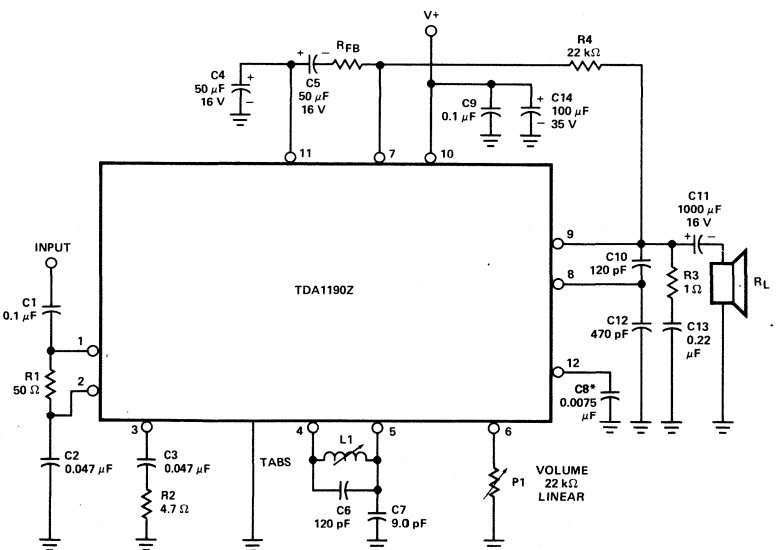


*RC = 50 µs

L1 = 12 µH
Qu = 80
f_o = 5.5 MHz

V+	12	24	V
R_L	8	16	Ω
R_{FB}	18	10	Ω

TEST CIRCUIT – TDA1190Z



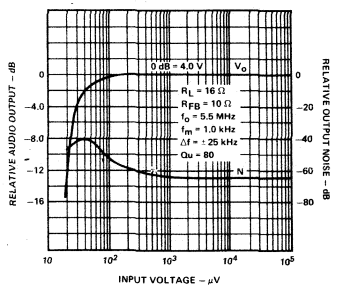
*RC = 75 µs

L1 = 10 µH
Qu = 60
f_o = 4.5 MHz

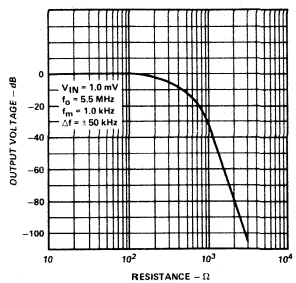
V+	12	24	V
R_L	8	16	Ω
R_{FB}	82	47	Ω

TYPICAL PERFORMANCE CURVES FOR TDA1190

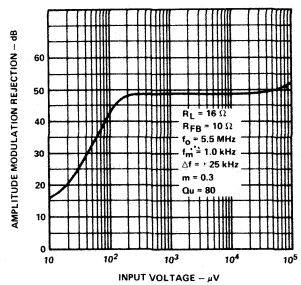
RELATIVE AUDIO OUTPUT VOLTAGE AND OUTPUT NOISE AS A FUNCTION OF INPUT VOLTAGE



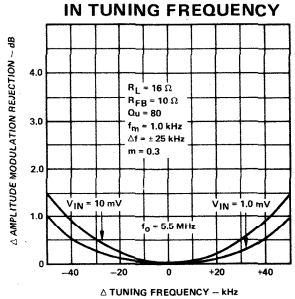
OUTPUT VOLTAGE ATTENUATION AS A FUNCTION OF dc VOLUME CONTROL RESISTANCE



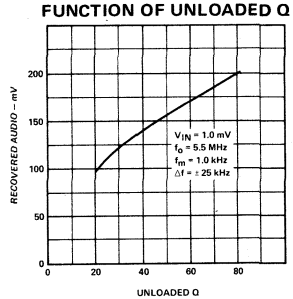
AMPLITUDE MODULATION REJECTION AS A FUNCTION OF INPUT VOLTAGE



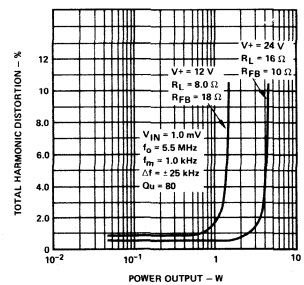
ΔAMR AS A FUNCTION OF CHANGE IN TUNING FREQUENCY



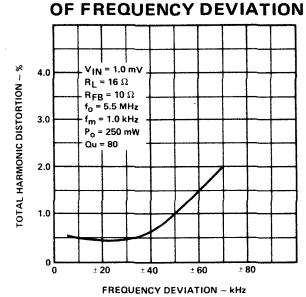
RECOVERED AUDIO AS A FUNCTION OF UNLOADED Q



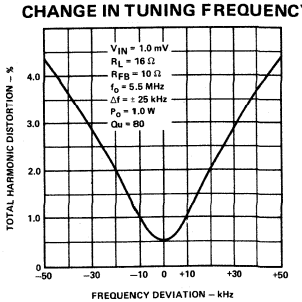
TOTAL HARMONIC DISTORTION AS A FUNCTION OF POWER OUTPUT



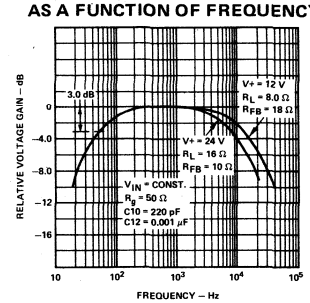
TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY DEVIATION



TOTAL HARMONIC DISTORTION AS A FUNCTION OF CHANGE IN TUNING FREQUENCY

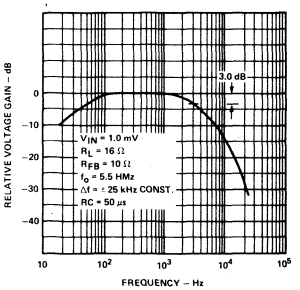


RELATIVE AUDIO AMPLIFIER VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

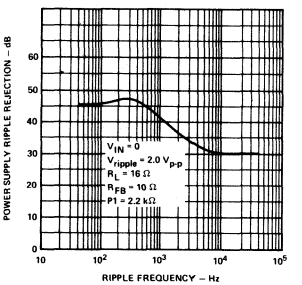


TYPICAL PERFORMANCE CURVES FOR TDA1190 (Cont'd)

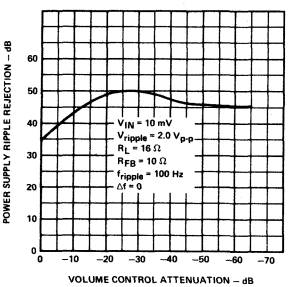
RELATIVE OVERALL VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



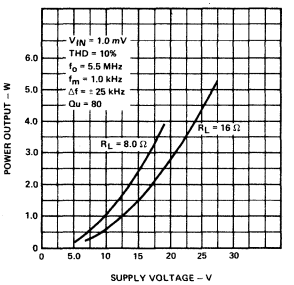
POWER SUPPLY RIPPLE REJECTION AS A FUNCTION OF RIPPLE FREQUENCY



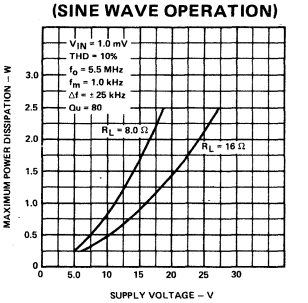
POWER SUPPLY RIPPLE REJECTION AS A FUNCTION OF VOLUME CONTROL ATTENUATION



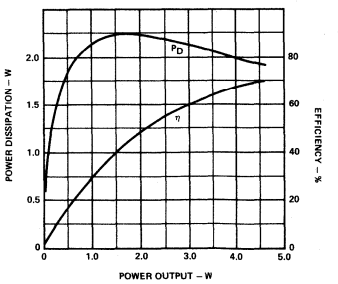
POWER OUTPUT AS A FUNCTION OF SUPPLY VOLTAGE



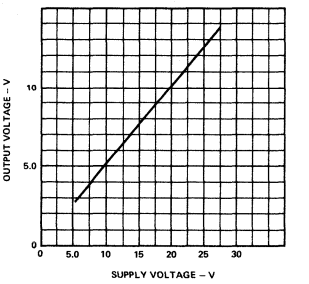
MAXIMUM POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE (SINE WAVE OPERATION)



POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF POWER OUTPUT

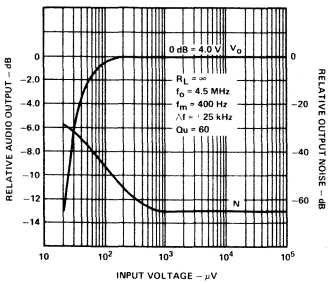


QUIESCENT OUTPUT VOLTAGE (PIN 9) AS A FUNCTION OF SUPPLY VOLTAGE

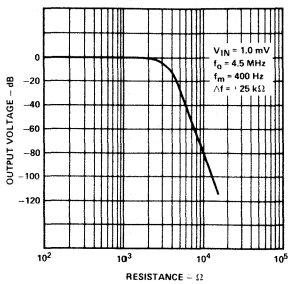


TYPICAL PERFORMANCE CURVES FOR TDA1190Z

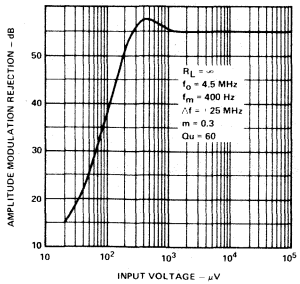
RELATIVE AUDIO OUTPUT VOLTAGE AND OUTPUT NOISE AS A FUNCTION OF INPUT VOLTAGE



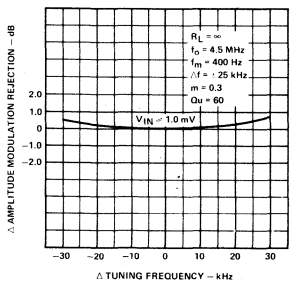
OUTPUT VOLTAGE ATTENUATION AS A FUNCTION OF dc VOLUME CONTROL RESISTANCE



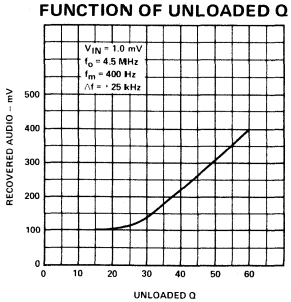
AMR AS A FUNCTION OF INPUT VOLTAGE



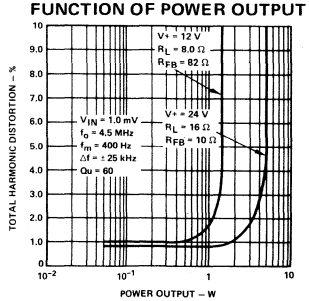
Δ AMR AS A FUNCTION OF CHANGE IN TUNING FREQUENCY



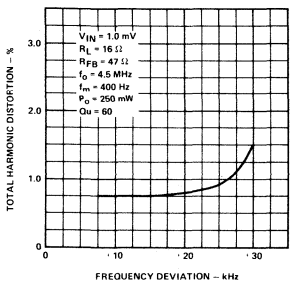
RECOVERED AUDIO AS A FUNCTION OF UNLOADED Q



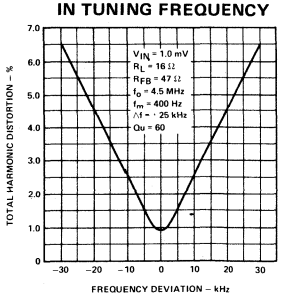
TOTAL HARMONIC DISTORTION AS A FUNCTION OF POWER OUTPUT



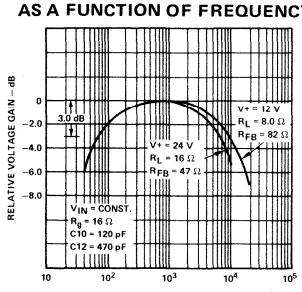
TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY DEVIATION



TOTAL HARMONIC DISTORTION AS A FUNCTION OF CHANGE IN TUNING FREQUENCY

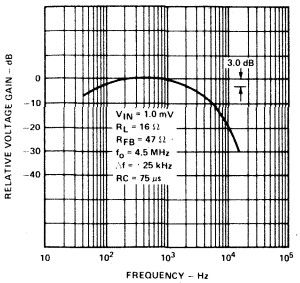


RELATIVE AUDIO AMPLIFIER VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

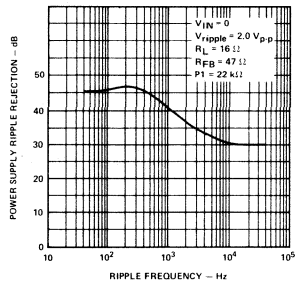


TYPICAL PERFORMANCE CURVES FOR TDA1190Z (Cont'd)

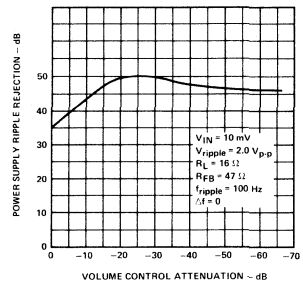
RELATIVE OVERALL VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



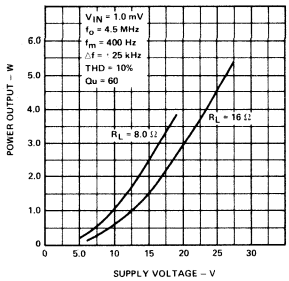
POWER SUPPLY RIPPLE REJECTION AS A FUNCTION OF RIPPLE FREQUENCY



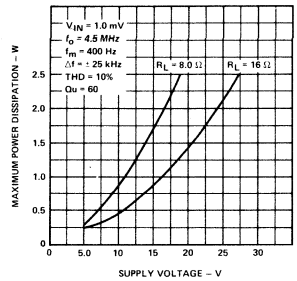
POWER SUPPLY RIPPLE REJECTION AS A FUNCTION OF VOLUME CONTROL ATTENUATION



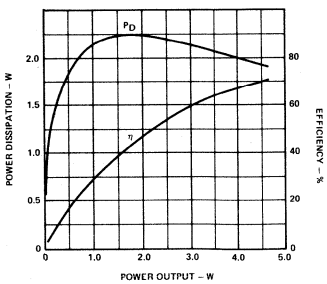
POWER OUTPUT AS A FUNCTION OF SUPPLY VOLTAGE



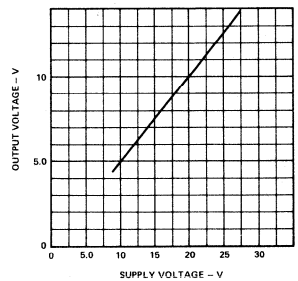
MAXIMUM POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE (SINE WAVE OPERATION)



POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF POWER OUTPUT



QUIESCENT OUTPUT VOLTAGE (PIN 9) AS A FUNCTION OF SUPPLY VOLTAGE

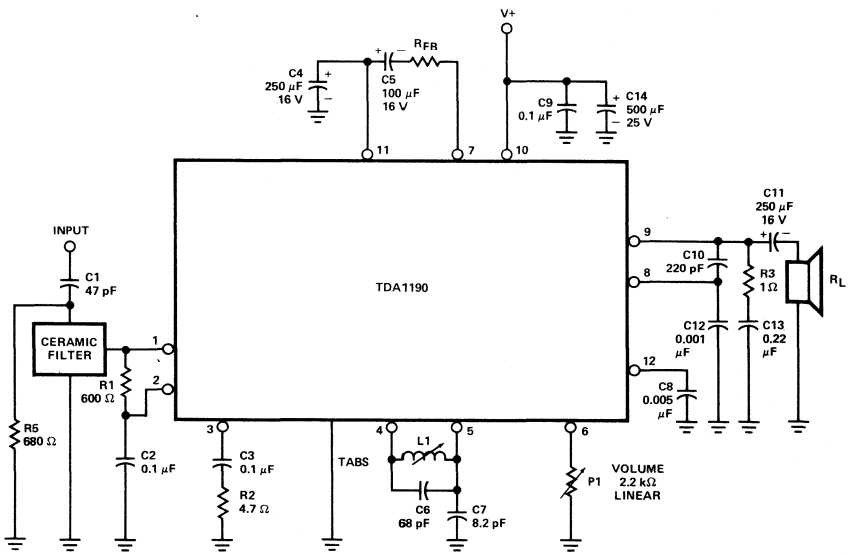


APPLICATIONS INFORMATION

The electrical characteristics of the TDA1190 and TDA1190Z remain almost constant over the frequency range 4.5 to 6.0 MHz, and therefore can be used in all television standards (FM mod.). They have a high input impedance to operate with a ceramic filter or with a tuned circuit that provides the necessary input selectivity.

The value of the resistors connected to pin 7 determines the AC gain of the audio frequency amplifier. With the TDA1190 (Figure 1), only one resistor (R_{FB}), is required to adjust the gain. The second resistor is included on the chip (typically 5.0 kΩ between pins 7 and 9). In the TDA1190Z (Figure 2), two resistors are required to adjust the gain (R4 and R_{FB}). This arrangement provides more accurate adjustment of gain.

TYPICAL APPLICATIONS CIRCUIT – TDA1190



L1 = 12 µH
Qu = 80
f_o = 5.5 MHz

V+	12	24	V
R_L	8	16	Ω
R_{FB}	18	10	Ω

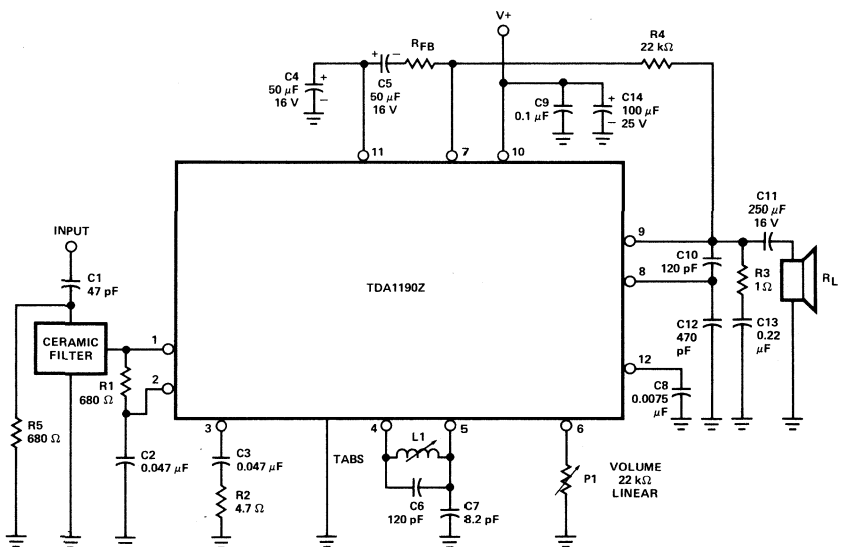
Fig. 1

APPLICATIONS INFORMATION (Cont'd)

The desired gain should be selected in relation to the frequency deviation at which the AF amplifier's output stage starts clipping. The capacitance connected between pins 9 and 8 determines the upper cut-off frequency of the audio band. If larger bandwidth is required, C10/C12 must be reduced keeping the C12/C10 ratio as shown in figure 1 or figure 2. The capacitance connected between pin 12 and ground, together with the internal resistor of 10 kΩ, forms the de-emphasis network. The Boucherot cell eliminates the high frequency oscillations caused by the inductive load and the wires connecting the loudspeaker. (R3, C13).

The TDA1190Z is also designed to operate with a larger volume control resistance than the TDA1190 for those systems where this is desired. The typical volume control resistance for the TDA1190Z is 22 kΩ and for the TDA1190 it is 2.2 kΩ.

TYPICAL APPLICATIONS CIRCUIT – TDA1190Z



L1 = 10 μH
Qu = 60
f_o = 4.5 MHz

V+	12	24	V
R_L	8	16	Ω
R_{FB}	82	47	Ω

Fig. 2

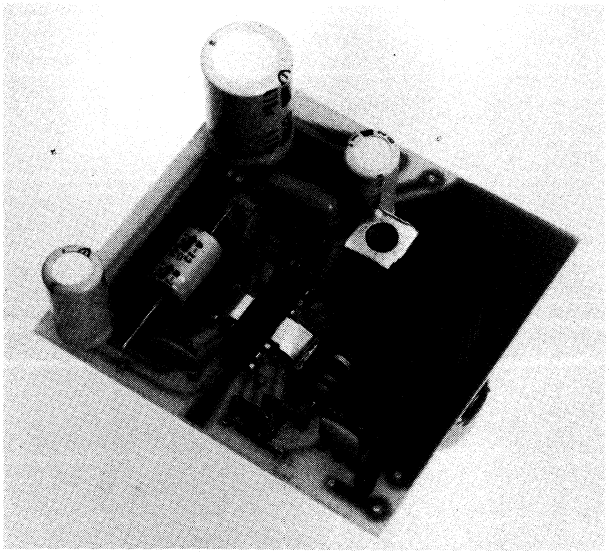
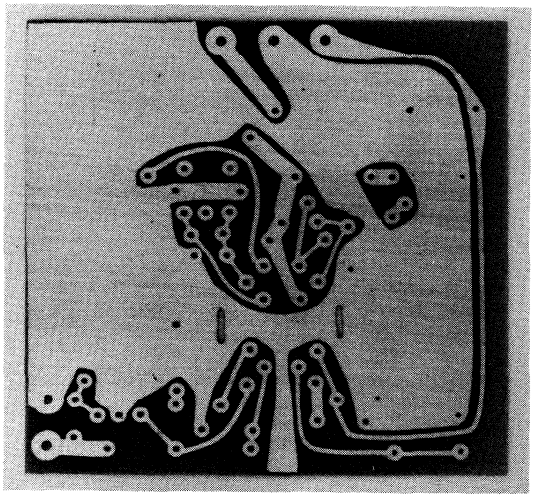
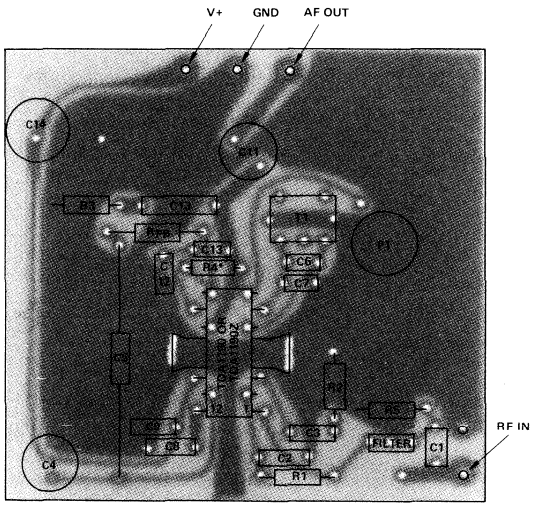


Fig. 3



P. C. BOARD
COPPER SIDE

Fig. 4



*TDA1190 and TDA1190Z components.
R4 is required only for TDA1190Z.

COMPONENTS LOCATION
(TOP VIEW)

Fig. 5

MOUNTING INSTRUCTION

The $\theta_{j\text{-amb}}$ of the TDA1190 and TDA1190Z can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (Fig. 6 or to an external heatsink (Fig. 7). Figure 8 shows the maximum allowable power P_D and the $\theta_{j\text{-amb}}$ as a function of the side "L" of the two equal square copper areas having a thickness of 35 μ (1.4 mils). During soldering the tab temperature must not exceed 260°C and the soldering time must not be longer than 10 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

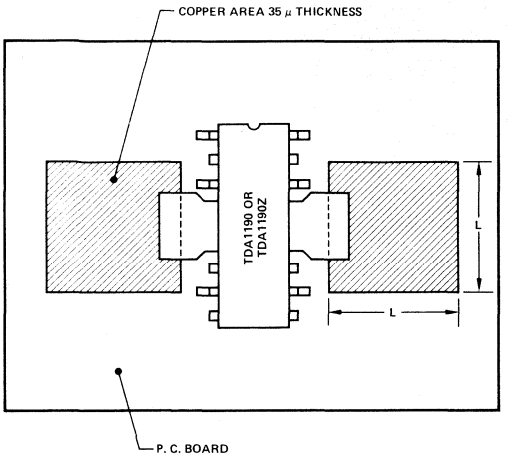


Fig. 6

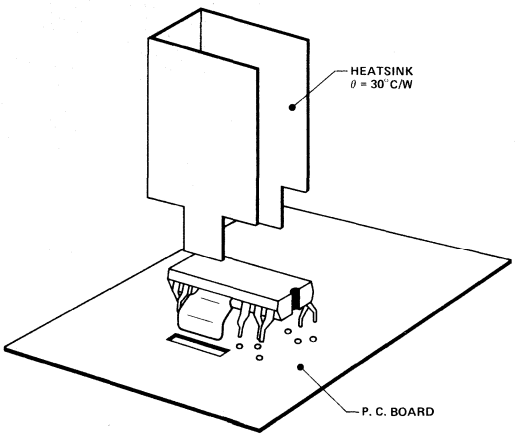


Fig. 7

MAXIMUM ALLOWABLE DISSIPATION AND $\theta_{j\text{-amb}}$ AS A FUNCTION OF COPPER LENGTH (SEE FIG. 6)

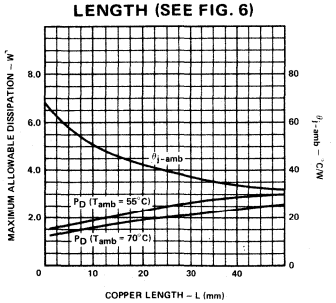


Fig. 8

MAXIMUM ALLOWABLE DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

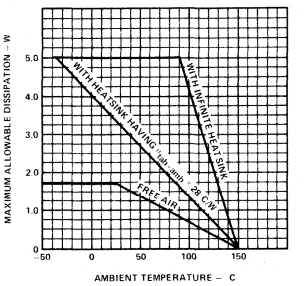


Fig. 9

TDA2002 • TDA2002A

8 WATT AUDIO POWER AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

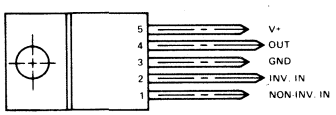
GENERAL DESCRIPTION – The TDA2002 and TDA2002A are monolithic integrated circuits designed for class B audio power amplifier applications using low impedance loads (down to 1.6 Ω). They are constructed using the Fairchild Planar* epitaxial process. The devices typically provide 8 W at 14.4 V, 2 Ω and 6.5 W at 16 V, 4 Ω.

The TDA2002 and TDA2002A are provided in a 5-pin power package, with two pin configurations (H and V) for ease in mounting either horizontally or vertically in the PC board.

The TDA2002A is the same electrically as the TDA2002 except it does not include the overvoltage (Load dump) protection circuit.

- **THERMAL SHUT DOWN**
- **SHORT CIRCUIT PROTECTION (AC)**
- **OVERVOLTAGE PROTECTION (TDA2002)**
- **LOW EXTERNAL COMPONENTS**
- **HIGH CURRENT CAPABILITY (3.5 A)**
- **MINIMUM SPACE REQUIREMENT**
- **WIDE SUPPLY VOLTAGE RANGE (8 V to 18 V)**

CONNECTION DIAGRAM
5-PIN POWER PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GO
PACKAGE CODE H, V



ORDER INFORMATION

TYPE	PART NO.
2002H	TDA2002H
2002V	TDA2002V
2002AH	TDA2002AH
2002AV	TDA2002AV

* Planar is a patented Fairchild Process.

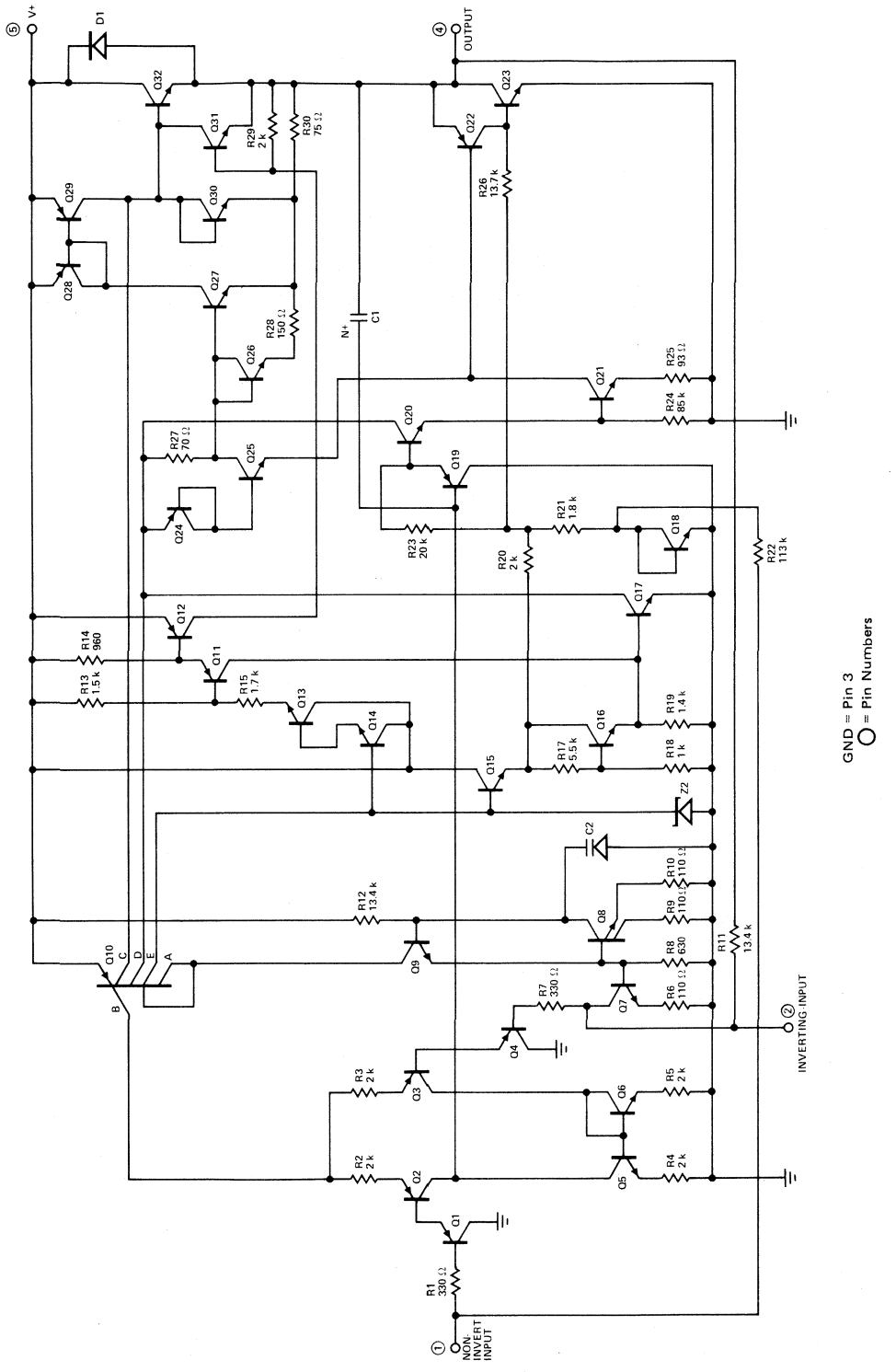
ABSOLUTE MAXIMUM RATINGS

	TDA2002	TDA2002A
Peak Supply Voltage (50 ms)	40 V	---
Supply Voltage	28 V	28 V
Operating Supply Voltage	18 V	18 V
Output Current (Repetitive)	3.5 A	3.5 A
Output Current (Non-Repetitive)	4.5 A	4.5 A
Power Dissipation: at $T_C = 90^\circ C$	15 W	15 W
Storage Temperature	-40 to $150^\circ C$	-40 to $150^\circ C$
Pin Temperature (Soldering, 10 s)	$260^\circ C$	$260^\circ C$

THERMAL DATA

θ_{JC} *Thermal resistance junction to case (max)* $4^\circ C/W$

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS: V+ = 14.4 V, T_A + 25°C, unless otherwise specified; see test circuit

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Output Voltage (Pin 4)		6.4	7.2	8.0	V
Quiescent Drain Current (Pin 5)			45	80	mA
Power Output	THD = 10% A_V = 100 f = 1 kHz				
	V+ = 16 V R_L = 4 Ω		6.5		W
	V+ = 16 V R_L = 2 Ω		10		W
	V+ = 14.4 V R_L = 4 Ω	4.8	5.2		W
	V+ = 14.4 V R_L = 2 Ω	7	8		W
Input Saturation Voltage (rms)		600			mV
Input Sensitivity	A_V = 100 f = 1 kHz				
	P_{OUT} = .5 W R_L = 4 Ω		15		mV
	P_{OUT} = .5 W R_L = 2 Ω		11		mV
	P_{OUT} = 5.2 W R_L = 4 Ω		55		mV
	P_{OUT} = 8 W R_L = 2 Ω		50		mV
Frequency Response (–3 dB)	R_L = 4 Ω C_{FB} = 39 nF R_{FB} = 39 Ω See Figs 15, 19		40–15000		Hz
Total Harmonic Distortion	A_V = 100 f = 1 kHz				
	P_{OUT} = 0.05-3.5 W (R_L = 4 Ω)		0.2		%
	P_{OUT} = 0.05-5 W (R_L = 2 Ω)		0.2		%
Input Resistance (Pin 1)	f = 1 kHz	70	150		kΩ
Voltage Gain					
(open loop)	f = 1 kHz R_L = 4 Ω		80		dB
(closed loop)		39.5	40	40.5	dB
Input Noise Voltage	BW (–3dB) = 40–15000 Hz Note 1		4		μV
Input Noise Current			60		pA
Efficiency	A_V = 100 f = 1 kHz				
	P_{OUT} = 5.2 W R_L = 4 Ω		68		%
	P_{OUT} = 8 W R_L = 4 Ω		58		%
Supply Voltage Rejection Ratio	AV = 100 R_L = 4 Ω R_g = 10 kΩ f_{ripple} = 100 Hz V_{ripple} = 0.5 V	30	35		dB

Note 1: Bandwidth (–3 dB) of test equipment = 10-25000 Hz

TYPICAL PERFORMANCE CURVES

QUIESCENT OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

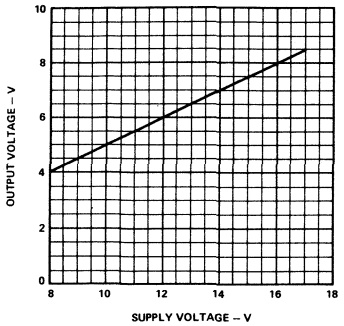


Fig. 1

QUIESCENT DRAIN CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

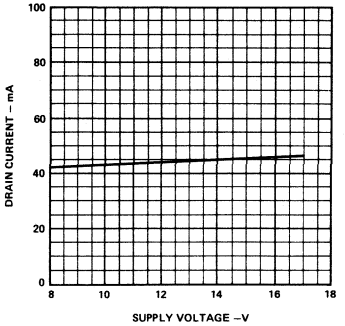


Fig. 2

OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE

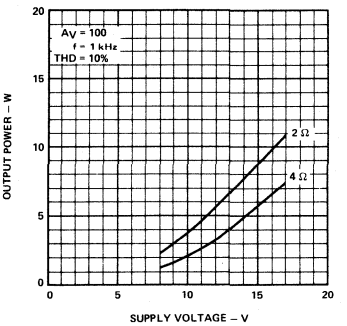


Fig. 3

OUTPUT POWER AS A FUNCTION OF LOAD RESISTANCE (RL)

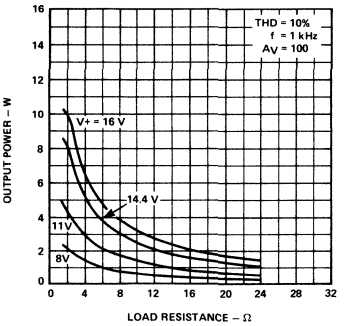


Fig. 4

INPUT VOLTAGE AS A FUNCTION OF VOLTAGE GAIN (R_L = 4 Ω)

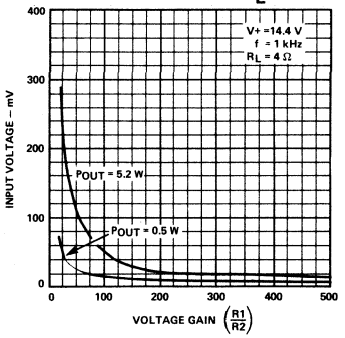


Fig. 5

INPUT VOLTAGE AS A FUNCTION OF VOLTAGE GAIN (R_L = 2 Ω)

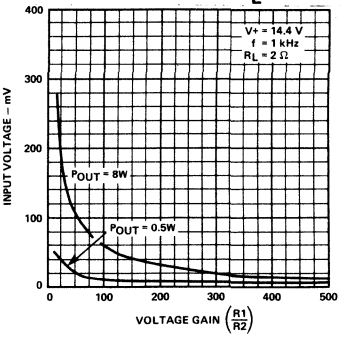


Fig. 6

TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER

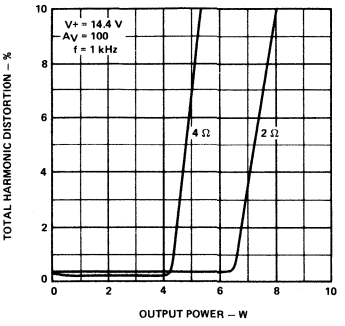


Fig. 7

TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY (R_L = 2 Ω; R_L = 4 Ω)

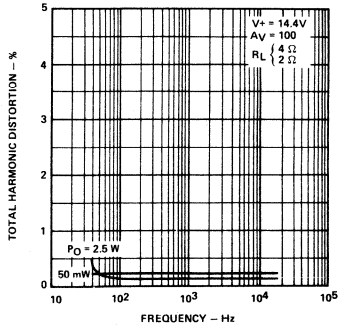


Fig. 8

SUPPLY VOLTAGE REJECTION AS A FUNCTION OF VOLTAGE GAIN

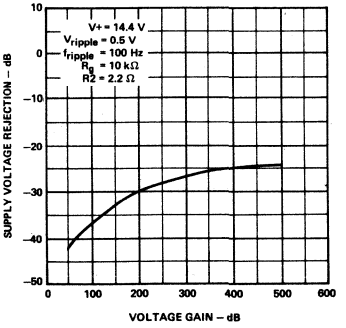


Fig. 9

TYPICAL PERFORMANCE CURVES (Cont'd)

SUPPLY VOLTAGE REJECTION AS A FUNCTION OF FREQUENCY

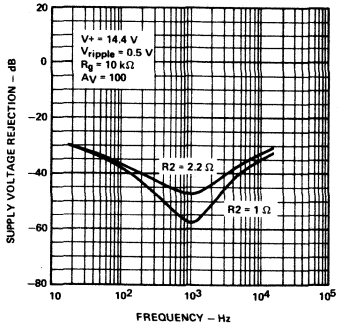


Fig. 10

POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF OUTPUT POWER (R_L = 4 Ω)

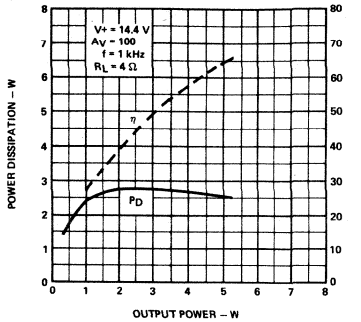


Fig. 11

POWER DISSIPATION AND EFFIECIENCY AS A FUNCTION OF OUTPUT POWER (R_L = 2 Ω)

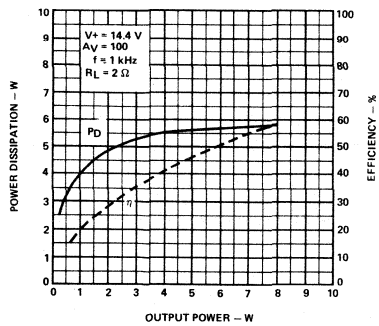


Fig. 12

MAXIMUM POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE (SINE WAVE OPERATION)

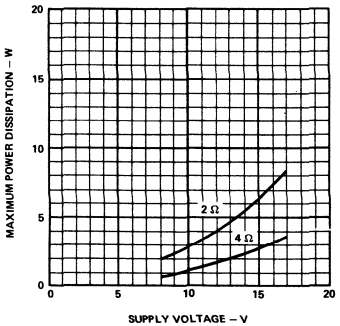


Fig. 13

MAXIMUM ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

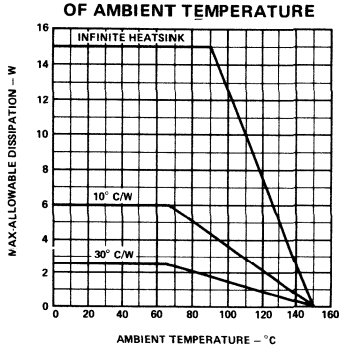


Fig. 14

CAPACITOR (CFB) AS A FUNCTION OF GAIN (VARIOUS BANDWIDTHS)

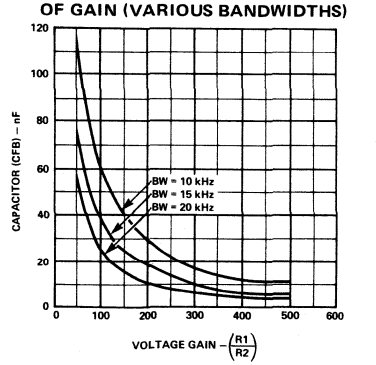


Fig. 15

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

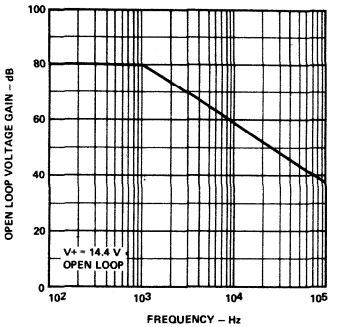


Fig. 16

OUTPUT POWER AND DRAIN CURRENT AS A FUNCTION OF CASE TEMPERATURE (R_L = 4 Ω)

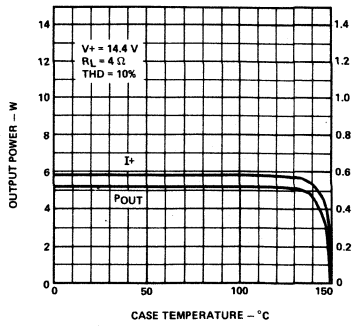


Fig. 17

OUTPUT POWER AND DRAIN CURRENT AS A FUNCTION OF CASE TEMPERATURE (R_L = 2 Ω)

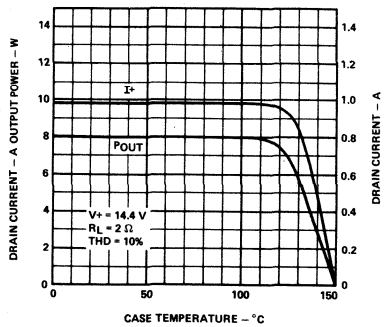


Fig. 18

DESIGN CONSIDERATIONS

The board layout of the TDA2002 and TDA2002A is critical to assure good stability. The layout shown in Figure 20 is recommended. If a different layout is used, it is important that the ground points of inputs 1 and 2 be well decoupled from the ground of the output. Pin lengths should be as short as possible.

The component values shown on the applications schematics are recommended. However, other values may be used, and Table 1 is intended to serve as a guide for the designer on the effect of changing component values.

No electrical insulation is needed between the package tab and the heat sink, if the heat sink is electrically isolated or is at ground potential.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
C1	10 μF	Input DC decoupling		Noise at switch-on, switch-off
C2	470 μF	Ripple rejection		Degradation of PSRR
C3	0.1 μF	Supply bypassing		Danger of oscillation
C4	1000 μF	Output coupling to load		Higher low frequency cutoff
C5	0.1 μF	Frequency stability		Danger of oscillation at high frequencies with inductive loads
CF_B	$\simeq \frac{1}{2\pi B R1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
R1	$(A_V - 1) \cdot R2$	Closed loop gain determination		Increase of drain current
R2	2.2 Ω	Closed loop gain and PSRR determination	Degradation of PSRR	
R3	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_{FB}	$\cong$ 20 R2	Upper frequency cutoff	Poor high frequency attenuation	Danger of oscillation

TABLE 1

APPLICATIONS INFORMATION:

Several typical applications of the TDA2002 and TDA2002A are shown in this section, together with printed circuit board layouts.

Figures 19 and 20 show a typical circuit with CFB, RFB shown dashed. CFB and RFB may be used to adjust the bandwidth after the gain has been set by the ratio R1/R2. (See Figure 15).

Figures 23 and 24 show a typical 15 watt bridge circuit utilizing two devices. A potentiometer (P1) is included to balance the offset voltages between the two devices.

TYPICAL APPLICATION CIRCUIT

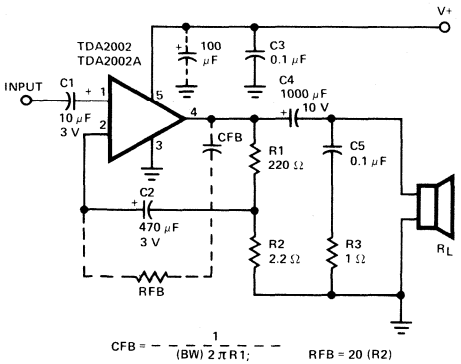


Fig. 19

P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 19 (1:1 SCALE)

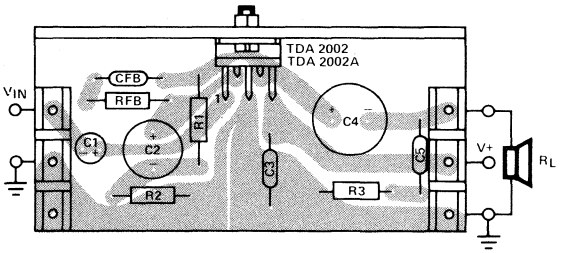


Fig. 20

LOW COST APPLICATION CIRCUIT

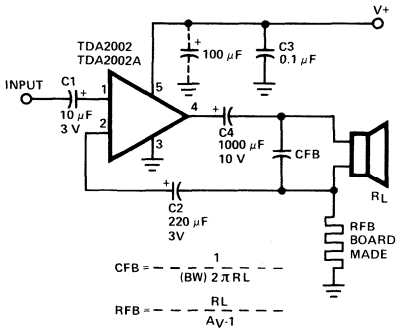


Fig. 21

P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 21 (1:1 SCALE)

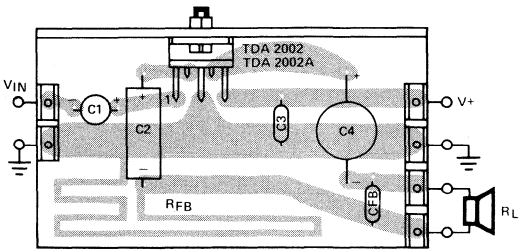


Fig. 22

15 WATT BRIDGE CIRCUIT

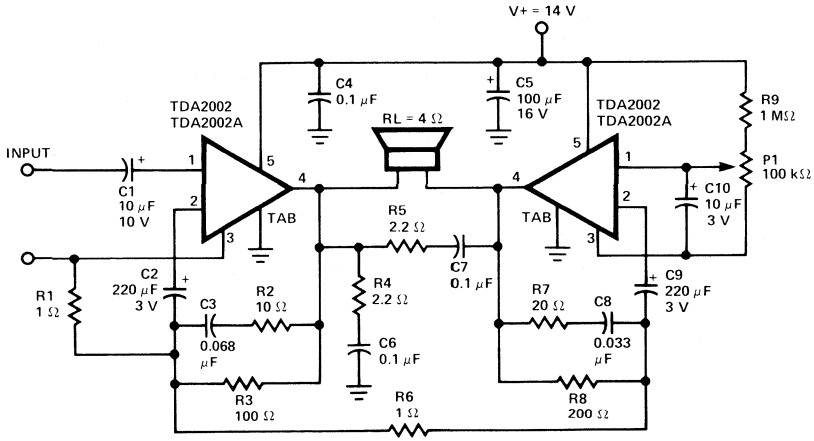


Fig. 23

P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 23 (1:1 SCALE)

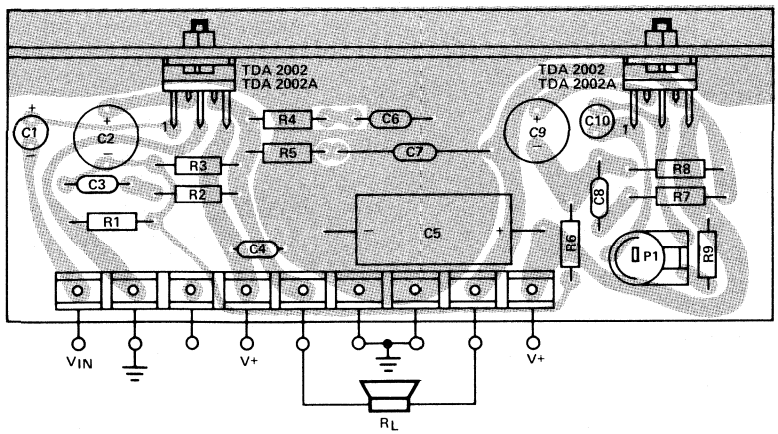


Fig. 24

THERMAL SHUTDOWN

Both the TDA2002 and TDA2002A have been designed with a thermal shutdown feature. Typical curves of output power and supply current as a function of case temperature are shown in Figures 17 and 18. The thermal overload circuit reduces the drive to the output stage when the junction temperature exceeds the design threshold. The result is a reduced supply current and power output consistent with maintaining the junction temperature at the design limit.

The thermal overload feature offers several important advantages to the circuit designer:

1. The device can withstand excessive ambient temperatures (below 150° C) and temporary or permanent overloads on the output.
2. The safety margin on the heat sink design may be reduced because the device will not be damaged by excessive junction temperature (below 150° C). The only result of this increased junction temperature will be a reduction in output power and supply current.

OVERVOLTAGE (LOAD DUMP) PROTECTION

The TDA2002 has been designed with a built-in circuit which enables this device to withstand a series of voltage spikes (see Figure 25). The load dump feature starts at about 18 V, so the operating voltage must not exceed 18 V.

This feature is particularly important in automobile applications, and the pulse train shown in Figure 25 is intended to simulate the voltage spikes which often occur on the supply line in automotive applications.

If the supply voltage peaks exceed 40 V, then an LC network must be inserted between the supply and Pin 5 to assure that the pulses at Pin 5 will not exceed the limits shown in Figure 25. A typical LC network is shown in Figure 26. With this network a train of pulses up to 120 V and 2 ms wide can be applied from the supply line.

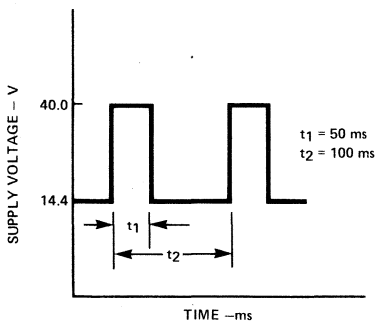


Fig. 25

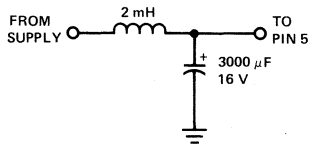
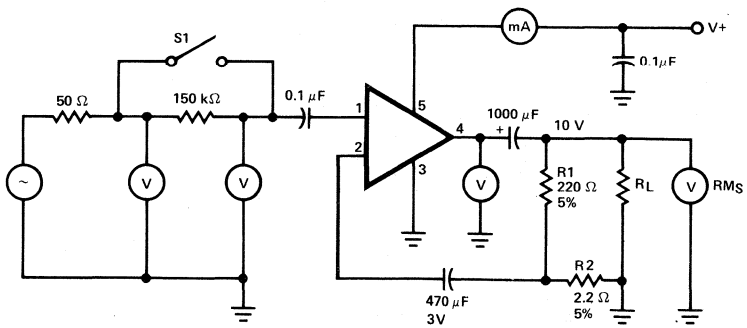


Fig. 26

TEST CIRCUIT



TDA2510

CHROMINANCE COMBINATION

FAIRCHILD LINEAR INTEGRATED CIRCUITS

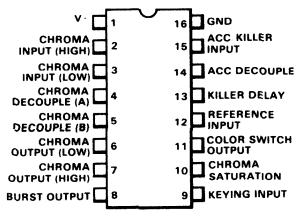
GENERAL DESCRIPTION – The TDA2510 is a monolithic integrated circuit designed for the chrominance function of a color television receiver. It is designed to interface directly with the TDA2521, using a minimum number of external components. The TDA2510 is constructed on a single silicon chip using the Fairchild Planar* epitaxial process.

- **CHROMA AMPLIFIER WITH ACC**
- **CONTROL VOLTAGE AMPLIFIER**
- **BURST SEPARATOR**
- **COLOR KILLER AND COLOR KILLER VOLTAGE DETECTOR**
- **LINEAR ELECTRONIC POTENTIOMETER FOR SATURATION CONTROL**
- **SCHMITT TRIGGER FOR COLOR KILLER**
- **CHROMA DELAY LINE DRIVER STAGE**
- **COLOR BURST OUTPUT STAGE**

ABSOLUTE MAXIMUM RATINGS

Supply voltage	15 V
Collector voltage of chroma output transistor (pin 7) (P_D = 100 mW max)	20 V
Collector current of chroma output transistor (pin 7)	20 mA
Collector current of color killer output transistor (pin 11)	10 mA
Power dissipation	500 mW
Operating temperature range	−25°C to +60°C
Storage temperature range	−55°C to +125°C
Pin Temperature (Soldering 10 s)	260°C

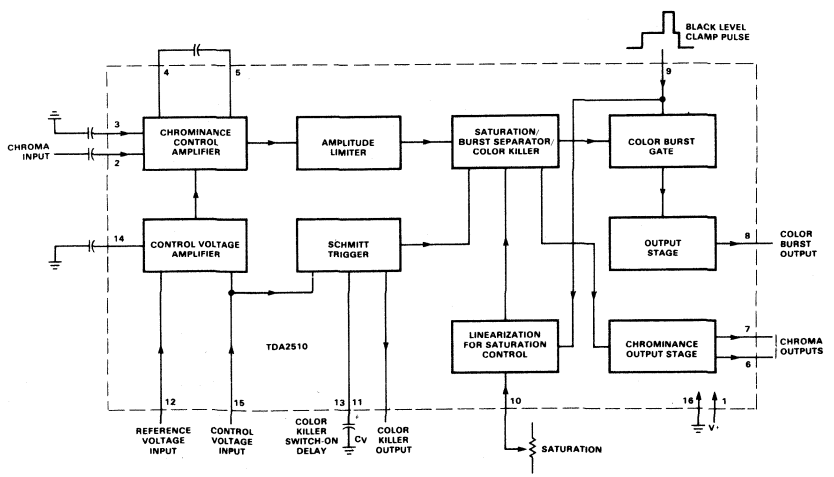
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



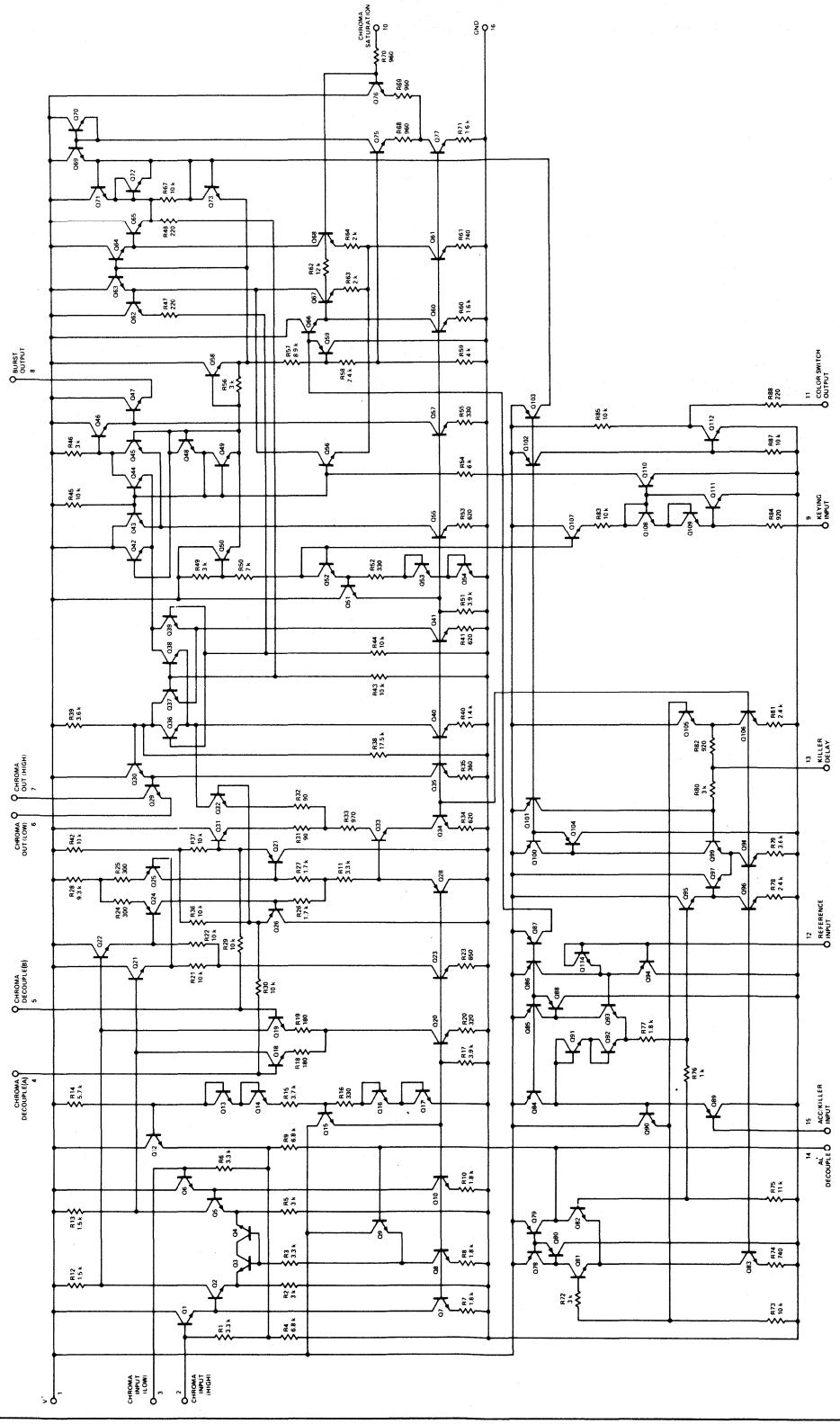
ORDER INFORMATION

TYPE	PART NO.
2510	TDA2510

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

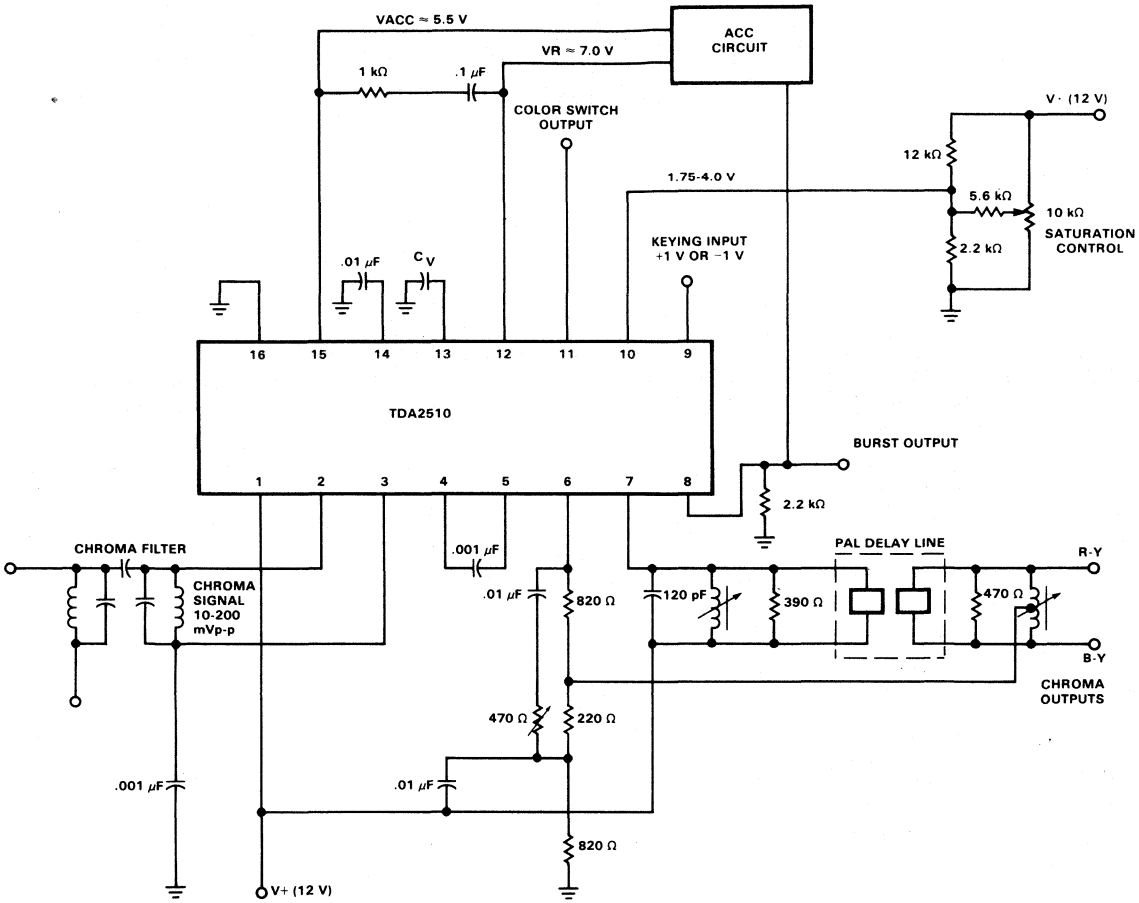

CHROMA SATURATION
10
GND
16
BURST OUTPUT
8
11
COLOR SWITCH OUTPUT
9
KEYING INPUT
13
KILLER DELAY
12
REFERENCE INPUT
14
ACC DECOUPLE
15
ACC KILLER INPUT
CHROMA DECOUPLE (R)
4
CHROMA DECOUPLE (B)
5
CHROMA OUT (LOW)
6
CHROMA OUT (HIGH)
7
V'
1
CHROMA INPUT (LOW)
3
CHROMA INPUT (HIGH)
2

ELECTRICAL CHARACTERISTICS: T_A = 25°C, V+ = 12 V, see test circuit unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Chroma Input (pin 2)					
V_{IN} (Symmetrical or Asymmetrical) Color bars (V_2 p-p)			100		mVp-p
Input Voltage Range (V_2 p-p)	Note 1	−20		+6.0	dB
Input Impedance (Z_2)		2.0			kΩ
Burst Output (Emitter Follower) (pin 8)					
DC Voltage at Burst Output (V_8)			9.0		V
Burst Output (V_8 p-p)	Note 1		0.5		Vp-p
Burst Output Limiting Level			1.5		Vp-p
Chroma Output (without Burst) (pin 6)					
DC Voltage at Chroma Output (V_6)			7.0		V
Chroma Output (Color Bars) at nominal Saturation and Maximum contrast (V_6 p-p)	Note 2		0.5		Vp-p
Signal Plus Noise to Noise Ratio	Note 3	50			dB
Saturation Control Range		−50		+6.0	dB
Phase Angle compared to Burst Output at Nominal Saturation		−5.0		5.0	degrees
Phase angle Shift during Saturation Control Range +6 to −10 dB		−5.0		5.0	degrees
Inputs for Control Voltage and Color Killer (pin 12, 15)	V_{REF} =				
Control Voltage (V_{15})	V_{12} = 7 V		5.5		V
Input Voltage (Color On) V_{15}	V_{12} = 7 V			5.7	V
Input Voltage (Color Off) V_{15}	V_{12} = 7 V	6.0			V
Signal Suppression (Color Off)	V_{12} = 7 V	50			dB
Control Input Impedance (Z_{15})		500			kΩ
Saturation Control Input (pin 10)					
Voltage Range for Linear Control (V_{10})		1.75		4.0	V
Threshold Voltage for > 50 dB suppression	*Note 4*	1.6	1.75		V
Input Impedance (Z_{10})			10		kΩ
Color Kill Switch Output (pin 11)					
Output Voltage (Color On) V_{11}			V+		V
Output Voltage (Color Off) V_{11}				0.5	V
Internal Resistance			10		kΩ
Burst Gating and Blanking Pulse (pin 9)					
Burst Gating and Blanking Pulse (positive or negative) (± V_9)		±1.0		±4.0	V
Input Impedance (Z_9)			1.0		kΩ
Color Killer Delay (pin 13)					
Delay Time as a Function of C_V			24		ms/μF

NOTES:
1. Burst output kept constant by ACC circuit at approximately 0.5 Vpp.
2. Nominal saturation is defined as maximum saturation − 6 dB, chroma/burst input ratio is approximately 2.
3. Signal plus noise to noise is calculated as V_{IN} (p-p)/6 (V_{noise} (rms)) for a standard color bar signal.
4. Saturation increases with increasing V_{10}.

APPLICATIONS AND TEST CIRCUIT



TDA2521

PAL TV CHROMA DEMODULATOR COMBINATION

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TDA2521 is a monolithic integrated circuit designed as a synchronous demodulator for PAL color television receivers. It includes an 8.8 MHz oscillator and divider, to generate two 4.4 MHz reference signals, and provides color difference outputs.

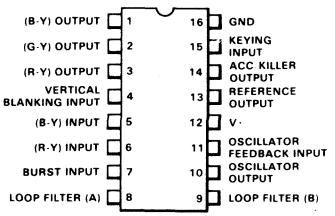
The TDA2521 is intended to interface directly with the TDA2510 with a minimum of external components and is constructed on a single silicon chip using the Fairchild Planar* epitaxial process.

- **8.8 MHz CHROMA SUBCARRIER OSCILLATOR AND DIVIDER TO GENERATE TWO 4.4 MHz REFERENCE SIGNALS**
- **KEYED PHASE COMPARATOR FOR OPTIMUM NOISE PERFORMANCE**
- **CHROMA CONTROL AND REFERENCE VOLTAGE**
- **COLOR KILLER AND IDENTIFICATION SIGNALS**
- **B-Y AND R-Y SYNCHRONOUS DEMODULATORS AND G-Y MATRIX**
- **TEMPERATURE COMPENSATED EMITTER FOLLOWER OUTPUTS**
- **PAL FLIP-FLOP AND SWITCH**
- **ON-CHIP CAPACITORS TO REDUCE CARRIER RESIDUE**
- **COLOR KILLED IN DEMODULATORS DURING FLYBACK**
- **VERTICAL BLANKING IN THE OUTPUT STAGES**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	14 V
Internal Power Dissipation	600 mW
Operating Temperature Range	−20°C to +60°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature (Soldering 10 s)	260°C

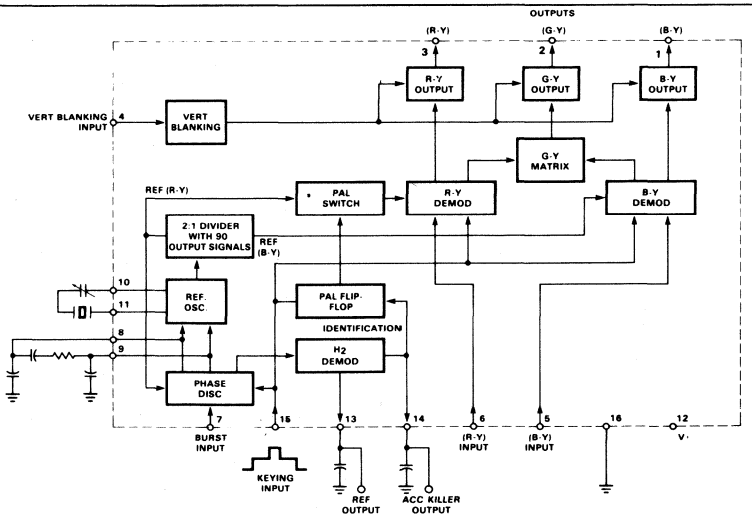
CONNECTION DIAGRAM
16-Pin DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

TYPE	PART NO.
2521	TDA2521

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

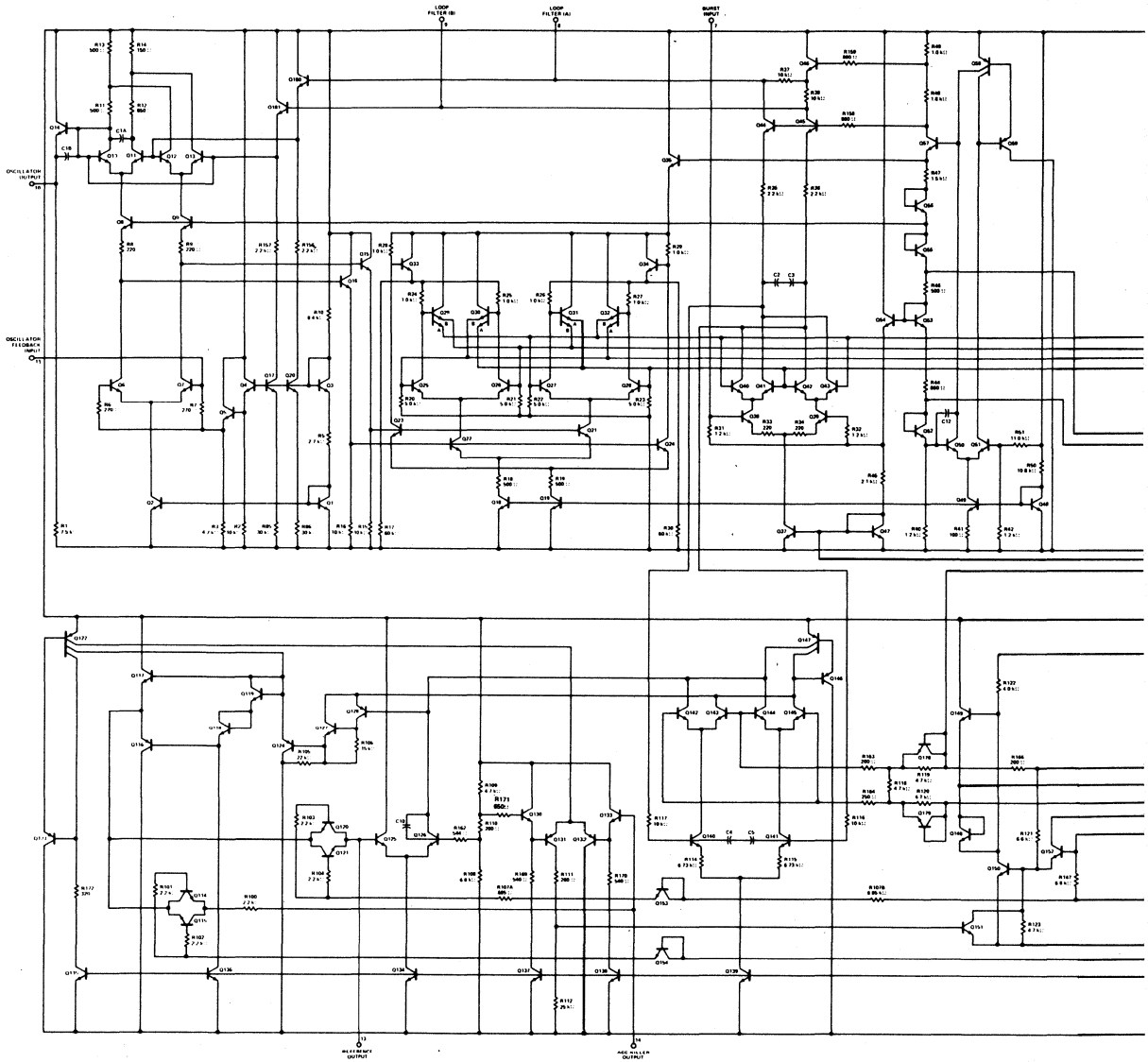
ELECTRICAL CHARACTERISTICS: V+ = 12 V, T_A = 25°C, unless otherwise specified

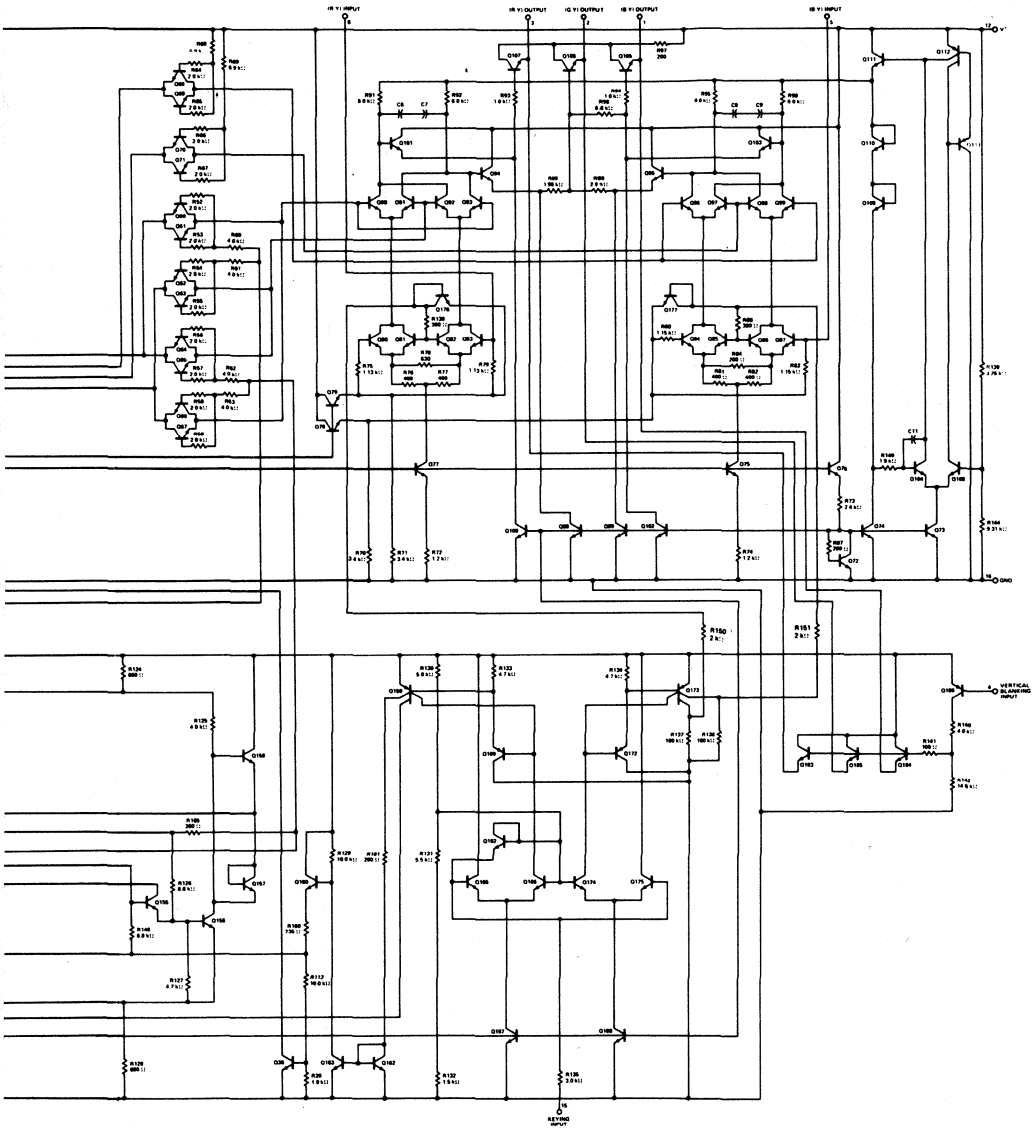
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_{12})			40		mA
DEMODULATOR SECTION (Pins 1, 2, 3)					
Ratio of Demodulated Signals					
B-Y/R-Y	$V_5 = V_6 = 50\ mV_{pk\text{-}pk}$		1.78		
G-Y Channel			Note 1		
Color Difference DC Output Voltage					
R-Y Output (V_3)			5.6		V
G-Y Output (V_2)			5.6		V
B-Y Output (V_1)			5.6		V
Color Difference Output Voltage					
R-Y Output ($V_{3pk\text{-}pk}$)		2.4			$V_{pk\text{-}pk}$
G-Y Output ($V_{2pk\text{-}pk}$)	Note 2	1.35			$V_{pk\text{-}pk}$
B-Y Output ($V_{1pk\text{-}pk}$)		3.0			$V_{pk\text{-}pk}$
H/2 Ripple Voltage at R-Y Output ($V_{3pk\text{-}pk}$)				10	mV
Input Resistance of Chroma Inputs (R5, R6)		800			Ω
Input Capacitance of Chroma Inputs (C5, C6)				10	pF
Output Resistance of Color Difference Terminals (R1, R2, R3)			250		Ω
REFERENCE SECTION					
Burst Signal Required on Pin 7 ($V_{7pk\text{-}pk}$)			0.5		$V_{pk\text{-}pk}$
Static Phase Error for ±400 Hz Deviation between f Burst and f Osc.			±5		degrees
Holding Range using a Typical Crystal			±500		Hz
DC Control Output Voltage (V_{14})					
Without Burst Signal			7.0		V
With 0.5 $V_{pk\text{-}pk}$ Burst Signal			5.5		V
ACC Reference Output Voltage (V_{13})			7.0		V
Keying Pulse Levels from Horizontal Combination TDA2590 (V_{15})					
Burst Keying (ON)				6.5	V
Burst Keying (OFF)		7.5			V
Blanking (ON)				6.5	V
Blanking (OFF)		7.5			V
Vertical Blanking (Pin 4)					
V_4 (ON)				V+ −2	V
V_4 (OFF)			V+		
Oscillator Input Resistance (R11)			270		Ω
Oscillator Output Resistance (R10)			200		Ω

NOTES:
1. G-Y output is typically equal to −0.51 (R-Y) − 0.19 (B-Y)
2. Increase V_{IN} = V_5 = V_6 until gain is equal to 0.7 of small signal gain.

4

EQUIVALENT CIRCUIT




IR Y1 INPUT
IR Y1 OUTPUT
IG Y1 OUTPUT
IB Y1 OUTPUT
IB Y1 INPUT
V+
GND
VERTICAL BLANKING INPUT
KEYING INPUT

TDA2522

PAL TV CHROMA DEMODULATOR COMBINATION

FAIRCHILD LINEAR INTEGRATED CIRCUIT

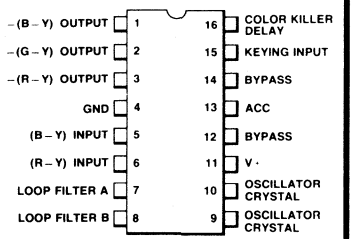
GENERAL DESCRIPTION – The TDA2522 is a monolithic integrated circuit designed as a synchronous demodulator for PAL color television receivers. It includes an 8.8 MHz oscillator and divider to generate two 4.4 MHz reference signals and provides color difference outputs.

The TDA2522 is intended to interface directly with the TDA2560 with a minimum of external components. The TDA2530 may be added if RGB drive is required. The TDA2522 is constructed using the Fairchild Planar* process.

- **8.8 MHz CHROMA SUBCARRIER OSCILLATOR AND DIVIDER TO GENERATE TWO 4.4 MHz REFERENCE SIGNALS**
- **KEYED BURST PHASE COMPARATOR FOR OPTIMUM NOISE PERFORMANCE**
- **ACC DETECTOR AND AMPLIFIER**
- **COLOR KILLER**
- **B – Y AND R – Y SYNCHRONOUS DEMODULATORS AND G – Y MATRIX**
- **TEMPERATURE COMPENSATED EMITTER FOLLOWER OUTPUTS**
- **PAL SWITCH AND FLIP-FLOP WITH INTERNAL IDENTIFICATION**
- **ON-CHIP CAPACITORS TO REDUCE CARRIER RESIDUE**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE 9B



ABSOLUTE MAXIMUM RATINGS

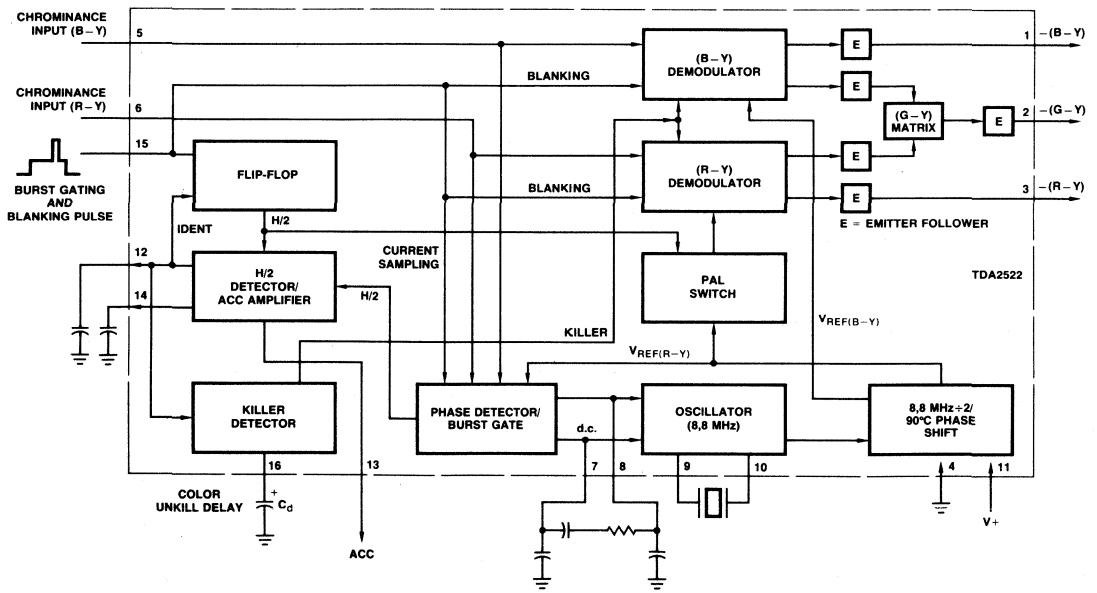
Supply Voltage	14 V
Internal Power Dissipation	600 mW
Operating Temperature Range	–20°C to +60°C
Storage Temperature Range	–20°C to +125°C
Pin Temperature (Soldering 10 s)	260°C

ORDER INFORMATION

TYPE	PART NO.
2522	TDA2522

*Planar is a patented Fairchild process.

BLOCK DIAGRAM



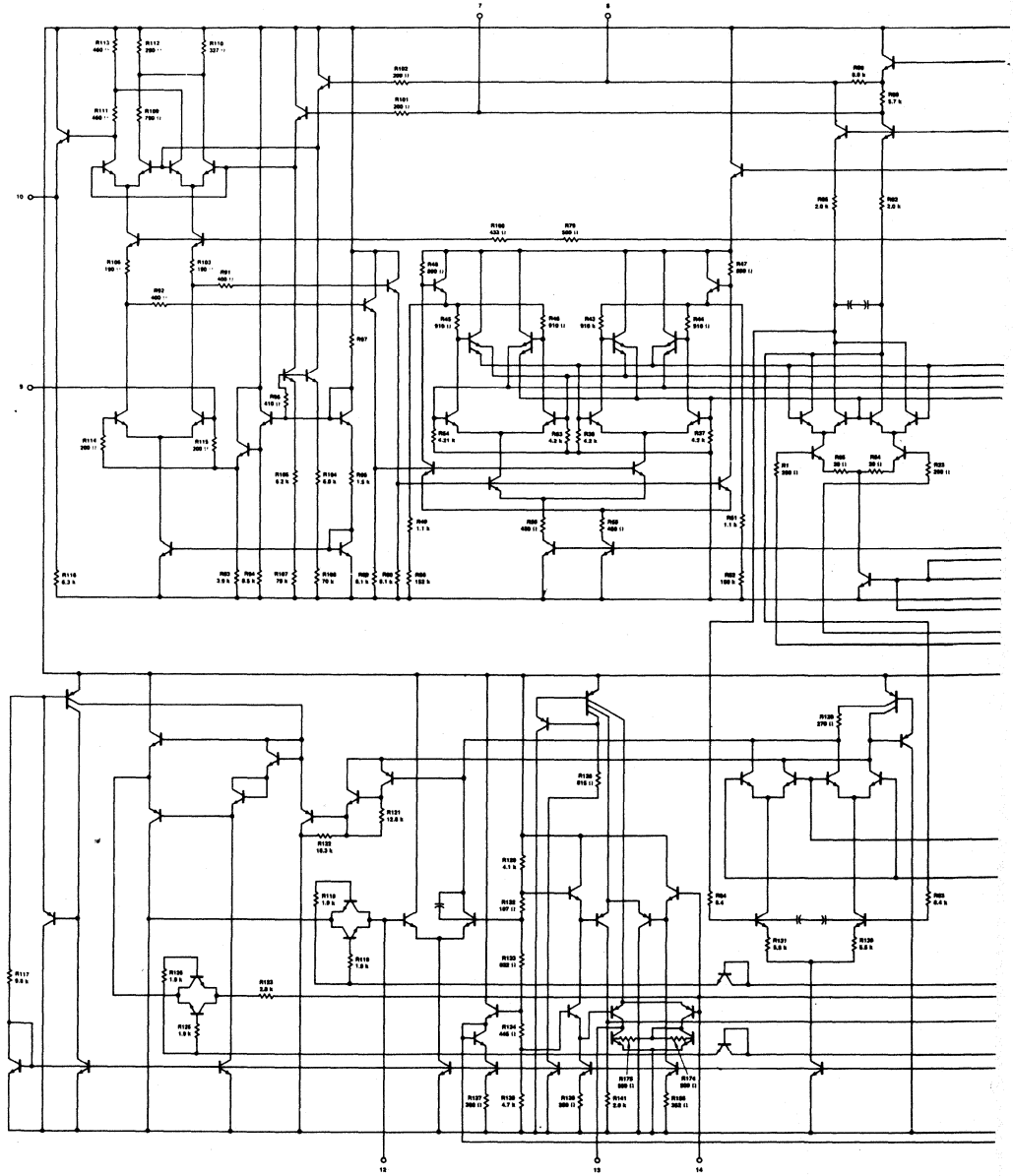
ELECTRICAL CHARACTERISTICS: V+ = 12 V, T_A = 25°C, unless otherwise specified

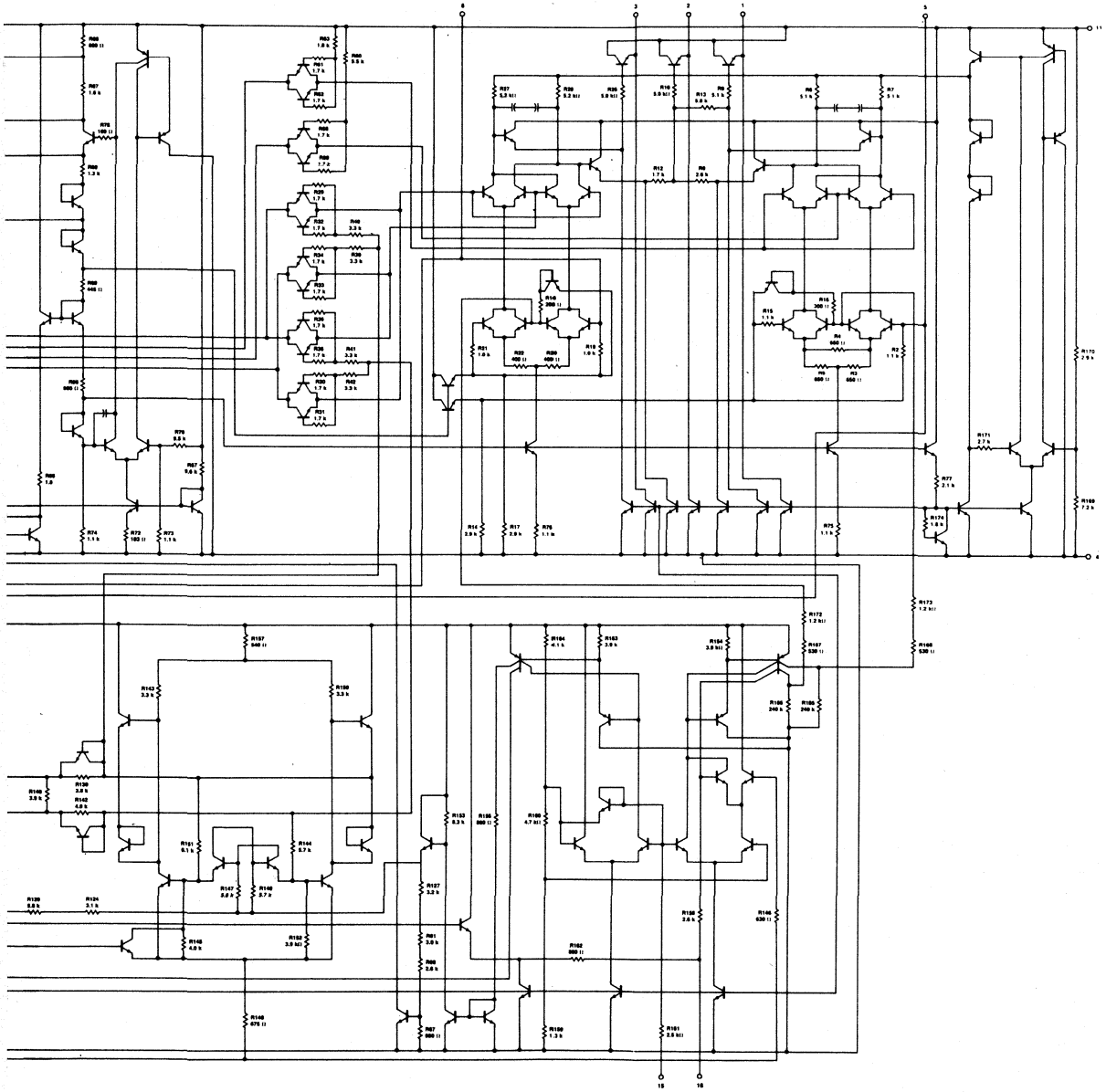
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_{11})			40		mA
DEMODULATOR SECTION					
Ratio of Demodulated Signals B−Y/R−Y G−Y Channel	$V_5 = V_6$ = 50 mV_{pk-pk}		1.78 Note 1		
Color Difference DC Output Voltage					
R−Y Output (V_3) G−Y Output (V_2) B−Y Output (V_1)			5.6 5.6 5.6		V V V
Color Difference Output Voltage					
R−Y Output (V_{3pk-pk}) G−Y Output (V_{2pk-pk}) B−Y Output (V_{1pk-pk})	Note 2	2.4 1.35 3.0			V_{pk-pk} V_{pk-pk} V_{pk-pk}
Chroma Input Signal (Including Burst)					
R−Y Input (V_{6pk-pk}) B−Y Input (V_{5pk-pk})	Note 3		500 350		mV mV
H/2 Ripple Voltage at R−Y Output (V_{3pk-pk})				10	mV_{pk-pk}
Input Resistance of Chroma Inputs (R5, R6) Input Capacitance of Chroma Inputs (C5, C6)		800		 10	Ω pF
Output Resistance of Color Difference Terminals (R1, R2, R3)			250		Ω
REFERENCE SECTION					
Static Phase Error for ±400 Hz Deviation between f Burst and f Oscillator		−5		+5	degrees
Holding Range using a Typical Crystal			±500		Hz
Burst Signal Input with Keying Pulse Width of 4 μs	Note 4		.25		V_{pk-pk}
ACC Control Output Voltage (V_{14})					
With Zero Burst With Correct Phase Burst Signal	 0.25 V_{pk-pk} Burst		7.0 5.5		V V
ACC Reference Output Voltage (V_{12})			7.0		V
ACC Amplifier Output					
I_{13}	V_{13} = 0.5 to 5.0 V	−200		+200	μA
Color Killer (V_{14} or V_{16})					
OFF (V_{14}) ON (V_{14})		6.0		 5.6	V V
OFF (V_{16}) ON (V_{16})		7.0		 5.0	V V
Color Killer Turn-On Delay	C_V Varried on Pin 16		20		ms/μF
Keying Pulse Levels from Horizontal Combination TDA2590 (V_{15})					
Burst Keying (ON) Burst Keying (OFF) Blanking (ON) Blanking (OFF)		7.5 2.0 		 6.5 1.0	V V V V
Oscillator Input Resistance (R9) Oscillator Output Resistance (R10)			270 200		Ω Ω

NOTES:

1. G−Y output is typically equal to −0.51 (R−Y) − 0.19 (B−Y).
2. Increase $V_{IN} = V_5 = V_6$ until gain is equal to 0.7 of small signal gain.
3. Color bar with 75% saturation.
4. Burst amplitude is kept constant by ACC but varies linearly with keying pulse width.

EQUIVALENT CIRCUIT





TDA2530

RGB MATRIX PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The TDA2530 is a monolithic RGB matrix preamplifier for color TV receivers. It is constructed using the Fairchild Planar* process. The TDA2530 provides RGB drive to the picture tube and also includes clamping circuits.

Symmetrical layout of the three channels assures uniform tracking and frequency response.

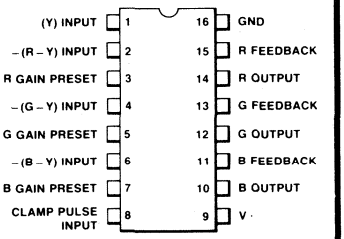
The TDA2530 is designed to be used with the TDA2560 and TDA2522 to form a three chip Chroma/Luma kit for PAL TV receivers

- **THREE MATCHED CHANNELS FOR MATRIXING**
- **MATCHED FREQUENCY RESPONSE AND TEMPERATURE STABILITY**
- **DIRECT DRIVE OF RGB VIDEO OUTPUT TRANSISTORS**
- **DC CLAMPING**

CONNECTION DIAGRAM

16-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE 9B



ORDER INFORMATION

TYPE	PART NO.
2530	TDA2530

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+)	15 V
Voltage Applied to Pin 1, 2, 3, 4, 5, 6, 7	0 to V+
Voltage Applied to Pin 8	V+
Voltage Applied to Pin 10	From V_{11} to (3 V + V+)
Voltage Applied to Pin 12	From V_{13} to (3 V + V+)
Voltage Applied to Pin 14	From V_{15} to (3 V + V+)
Voltage Applied to Pin 11, 13, 15	0.3 V+ to V+
Current into Pin 8	−1 mA
Power Dissipation	1 W
Operating Temperature Range	−20°C to +60°C
Storage Temperature Range	−20°C to +125°C
Pin Temperature (Soldering 10 s)	260°C

*Planar is a patented Fairchild Process.

APPLICATIONS INFORMATION

The TDA2530 is normally driven with the color difference outputs from the TDA2522 and the luminance output from the TDA2560. These signals are matrixed within the TDA2530 to directly drive the video output transistors and provide the RGB drive to the picture tube.

The TDA2530 may also be used as a matrix circuit in other configurations for both NTSC and PAL television receivers, monitors, etc. . A typical circuit is shown in Figure 1.

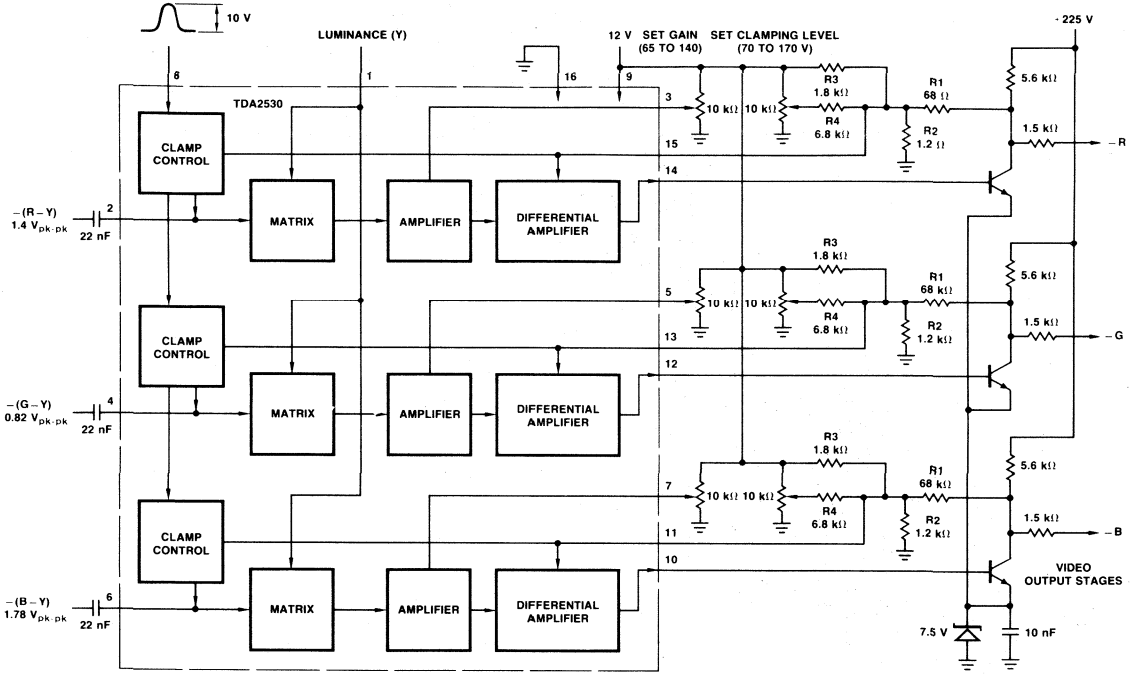


Figure 1.

CLAMPING

With the clamping level potentiometers (Figure 1) set in their mid-positions, the clamping of the video output stages is :

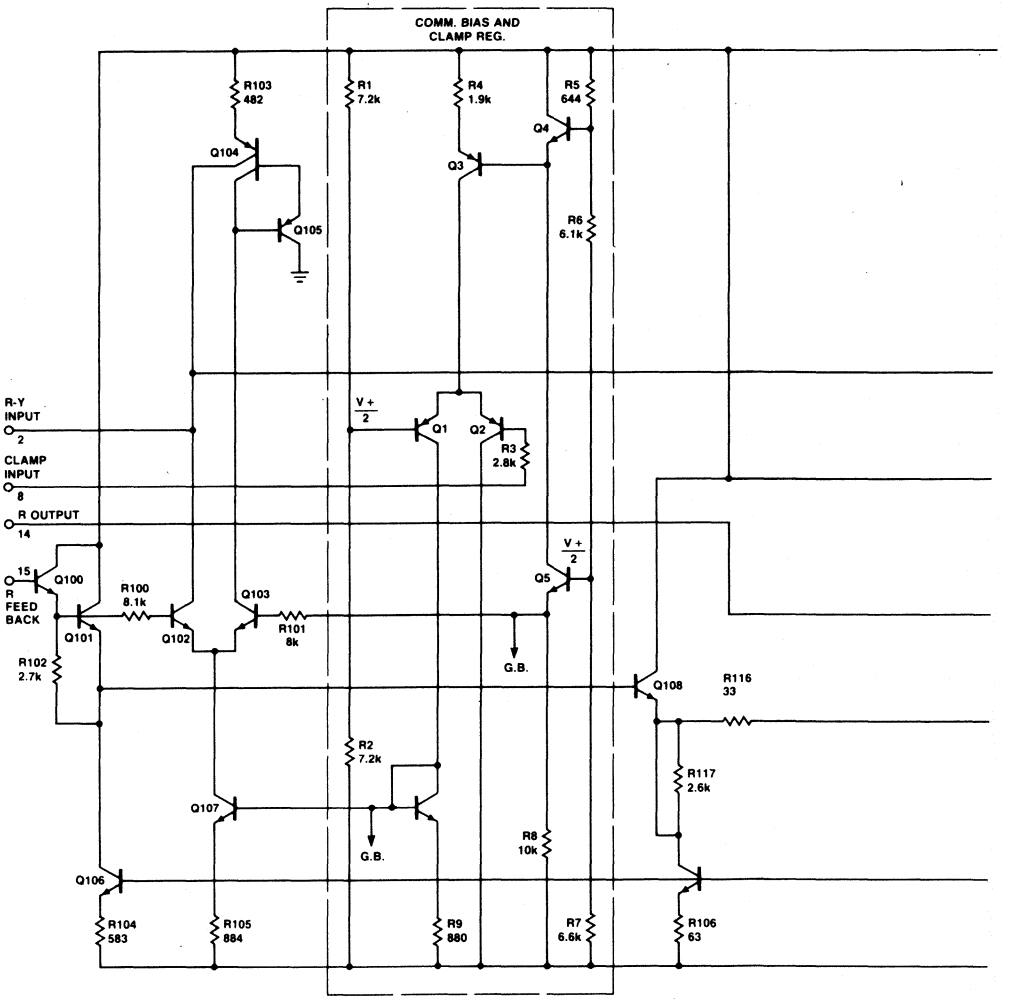
$$V_{CL} = \left(\frac{V+}{2}\right)\left(1 + \frac{R_1}{R_2} - \frac{R_1}{R_3}\right)$$

VIDEO GAIN

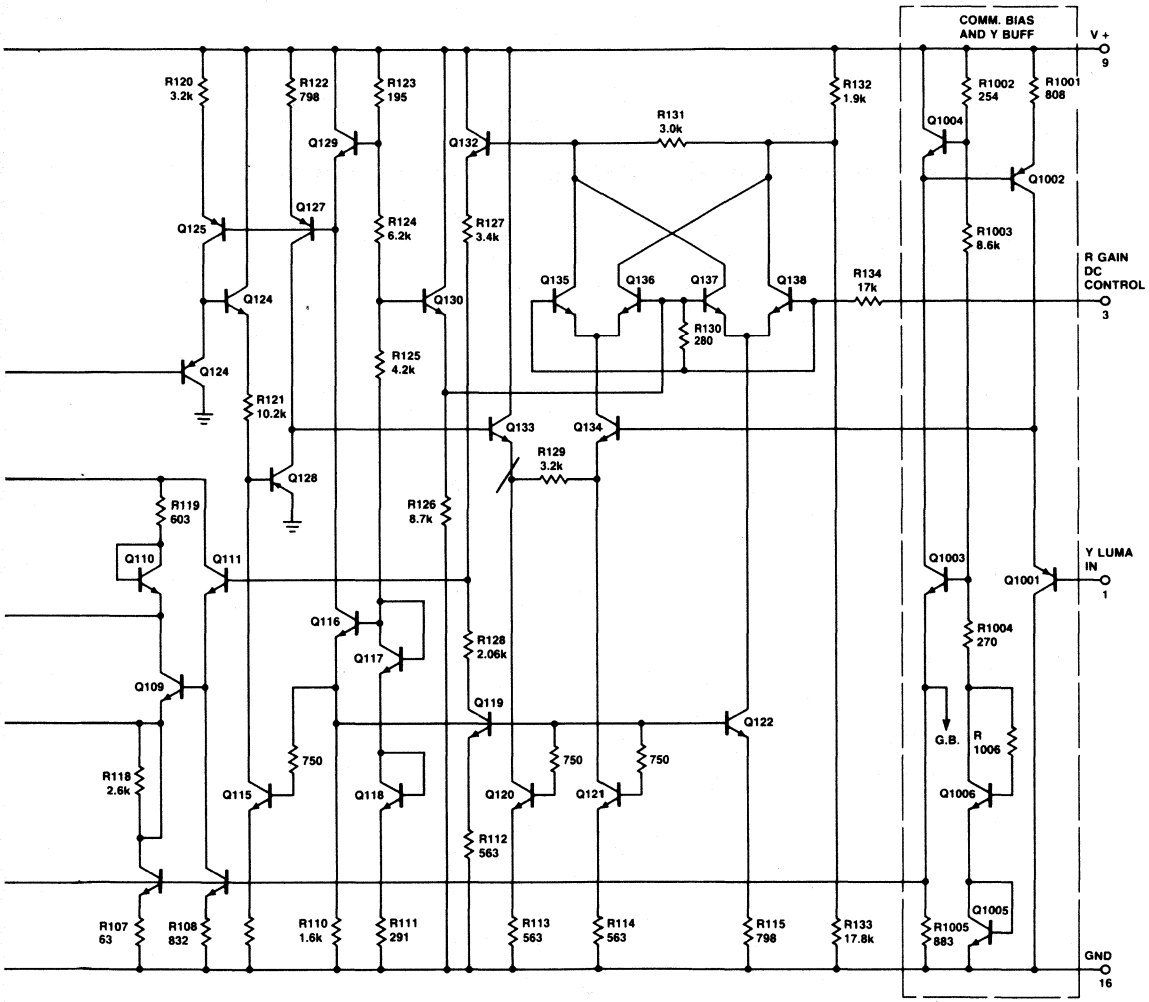
The video output stage gain of the circuit of Figure 1 may be calculated as:

$$G = 1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}$$

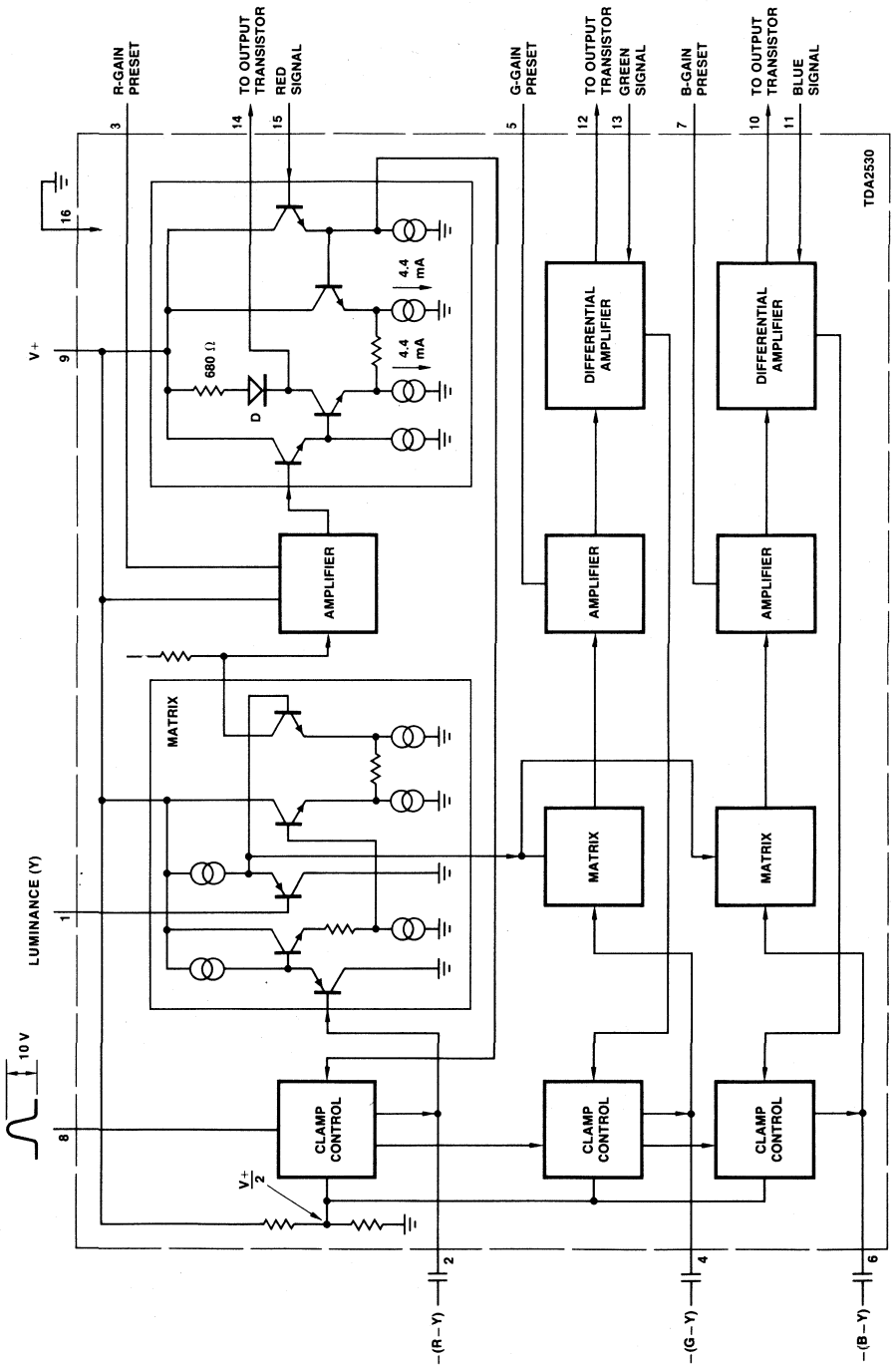
SCHEMATIC DIAGRAM



Resistor values are in ohms (Ω).


COMM. BIAS AND Y BUFF
V+
9
R120 3.2k
R122 798
R123 195
R131 3.0k
R132 1.9k
R1002 254
R1001 808
Q129
Q132
Q1004
Q1002
Q127
Q125
R124 6.2k
R127 3.4k
R1003 8.6k
R GAIN DC CONTROL
Q135
Q136
Q137
Q138
R134 17k
3
Q124
Q130
Q124
R130 280
R125 4.2k
R121 10.2k
Q133
Q134
R129 3.2k
Q128
R119 603
R126 8.7k
Q110
Q111
Q1003
Q1001
Y LUMA IN
1
Q116
Q117
R128 2.06k
R1004 270
Q109
Q119
Q122
G.B.
R 1006
750
750
750
R118 2.6k
Q115
Q118
Q120
Q121
Q1006
R112 563
Q1005
R107 63
R108 832
R110 1.6k
R111 291
R113 563
R114 563
R115 798
R133 17.8k
R1005 883
GND
16

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS: V+ = 12 V, V_1 = 1.5 V, T_A = 25°C measured in test circuit unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_9)			50		mA
LUMINANCE					
Black Level (V_1)			1.5		V
Black-to-White Input Voltage Range			1.0		V_{pk-pk}
Input Resistance (R_1)		100			kΩ
CHROMA DIFFERENCE INPUTS					
R−Y Input (V_2)	Note 1		1.4		V_{pk-pk}
G−Y Input (V_4)	Note 1		0.82		V_{pk-pk}
B−Y Input (V_6)	Note 1		1.78		V_{pk-pk}
Input Current (I_2, I_4, I_6)		−4.0	−2.0		μA
Input Current during Clamping (I_2, I_4, I_6)			±0.2		mA
CLAMP PULSE INPUT					
Input Voltage for Clamping (V_8)					
ON Level	Note 2		6.5 to 12.0		V
OFF Level			0 to 5.5		V
Input Current for Clamping (I_8)					
ON Level				1	μA
OFF Level		−20			μA
FEEDBACK INPUT					
DC Level during Clamping (V_{11}, V_{13}, V_{15})			$\frac{V+}{2}$		V
GAIN ADJUSTMENTS FOR COLOR DRIVE					
Adjustment Voltage Range (V_3, V_5, V_6)			0-10		V
Adjustment Voltage for Nominal Gain			5.0		V
Nominal Gain between Color Difference, Luminance Inputs, and Color Feedback Inputs	Note 3		0		dB
Adjustment Range of Nominal Gain	Δ V_3, V_5, V_7 = ±5V	+3		−3	dB
DIFFERENTIAL AMPLIFIER					
Input Current (I_{11}, I_{13}, I_{15})			2		μA
Gain of Error Amplifier			20		mA/V
Output Current Swing (I_{10}, I_{12}, I_{14})			±4.4		mA
Load Resistance (R_{10}, R_{12}, R_{14})	Note 4		680		Ω
Output Bias Voltage (V_{10}, V_{12}, V_{14})	Note 4		8		V

NOTES:
1. The inputs and therefore the corresponding outputs may be interchanged as all three channels are identical.
2. Switching from clampling ON to OFF occurs at approximately 6 Volts.
3. Neglible error signal is assumed.
4. The load resistors have series diodes (D in block diagram). Thus, the resistors can be ignored when V_{10}, V_{12}, and $V_{14} \geq$ V+. In this case, the external load resistors must be chosen such that the nominal current is 4.4 mA.

TDA2560

LUMINANCE AND CHROMINANCE CONTROL COMBINATION

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION: The TDA2560 is a monolithic integrated circuit for use in the luma and chroma sections of color television receivers. It contains the brightness, saturation and contrast control circuitry and is manufactured using the Fairchild Planar* process. It is designed to interface directly with the TDA2522 chroma demodulator. The TDA2530 may be added to provide an RGB drive to the picture tube. The TDA2560 may also be used in NTSC receivers.

LUMINANCE SECTION

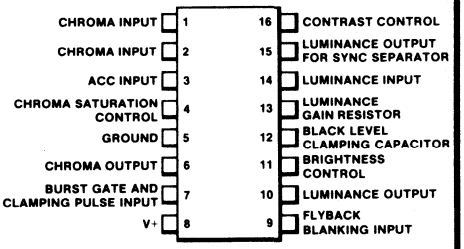
- **LOW INPUT IMPEDANCE FOR EASE IN MATCHING DELAY LINE**
- **DC CONTRAST AND BRIGHTNESS CONTROL**
- **BLACK LEVEL CLAMP**
- **BLANKING**
- **ADDITIONAL VIDEO OUTPUT WITH POSITIVE SYNC**

CHROMINANCE SECTION

- **GAIN CONTROLLED AMPLIFIER**
- **CHROMA GAIN TRACKS WITH CONTRAST**
- **SEPARATE DC SATURATION CONTROL**
- **COMBINED CHROMA AND BURST OUTPUT**
- **BURST AMPLITUDE INDEPENDENT OF CONTRAST AND SATURATION CONTROL**
- **DIRECT DELAY LINE DRIVE FROM THE IC**

*Planar is patented Fairchild process.

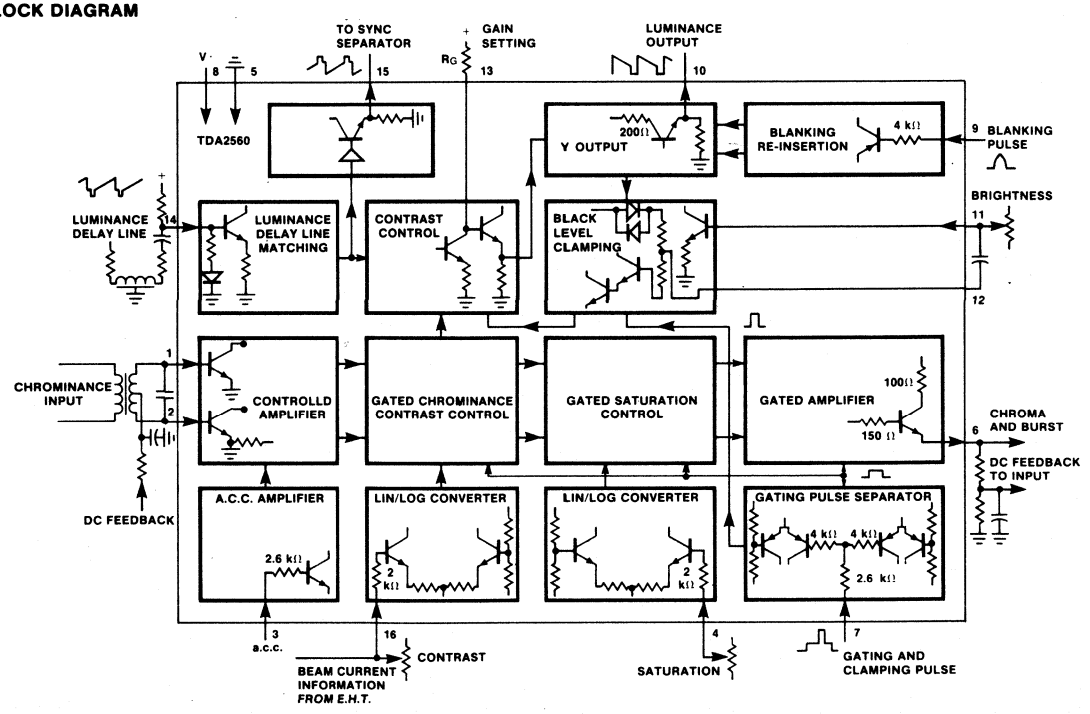
CONNECTION DIAGRAM
16-PIN DIP
PACKAGE OUTLINE 9B



ORDER INFORMATION

TYPE	PART NO.
2560	TDA2560

BLOCK DIAGRAM



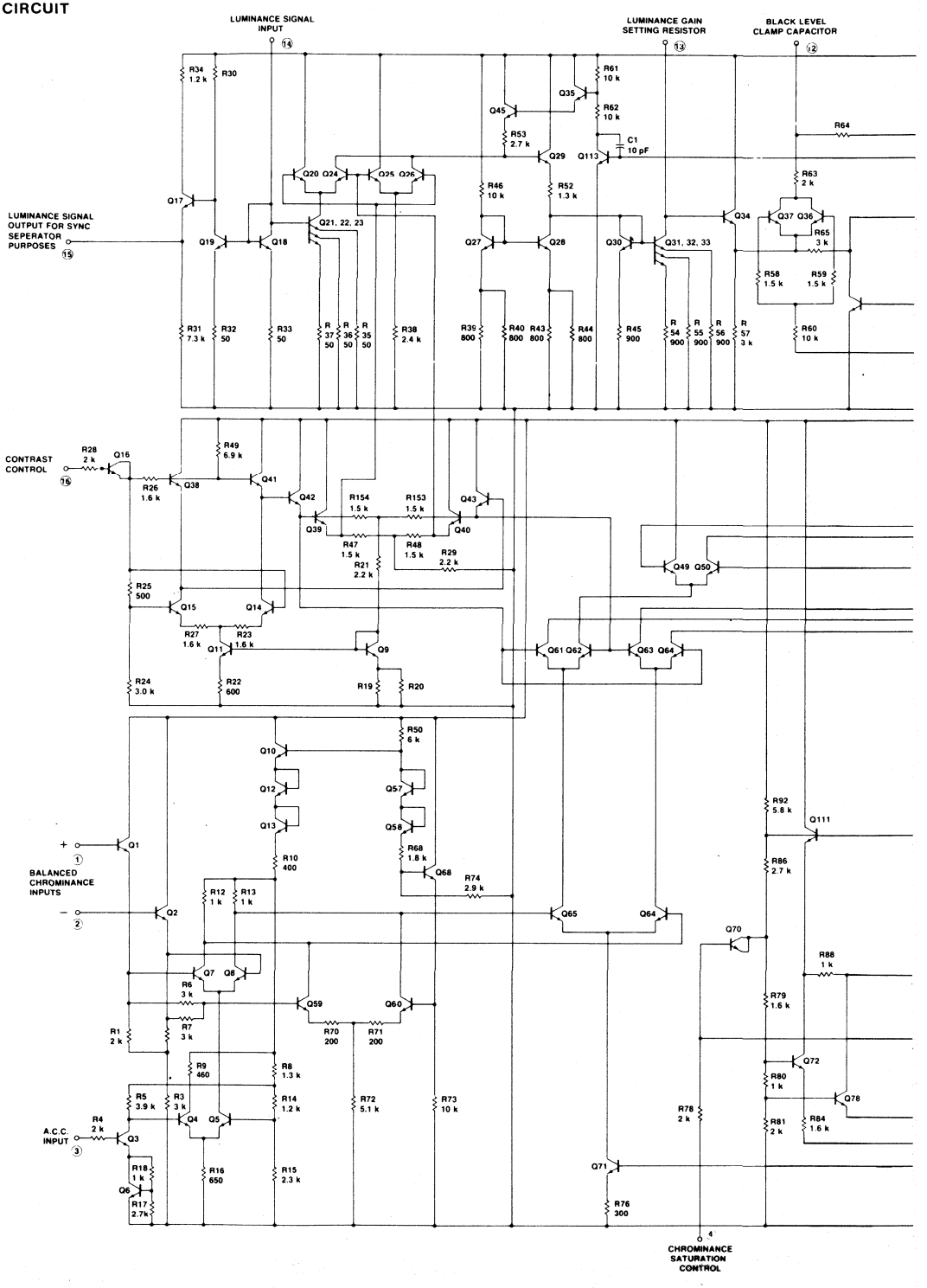
ABSOLUTE MAXIMUM RATINGS

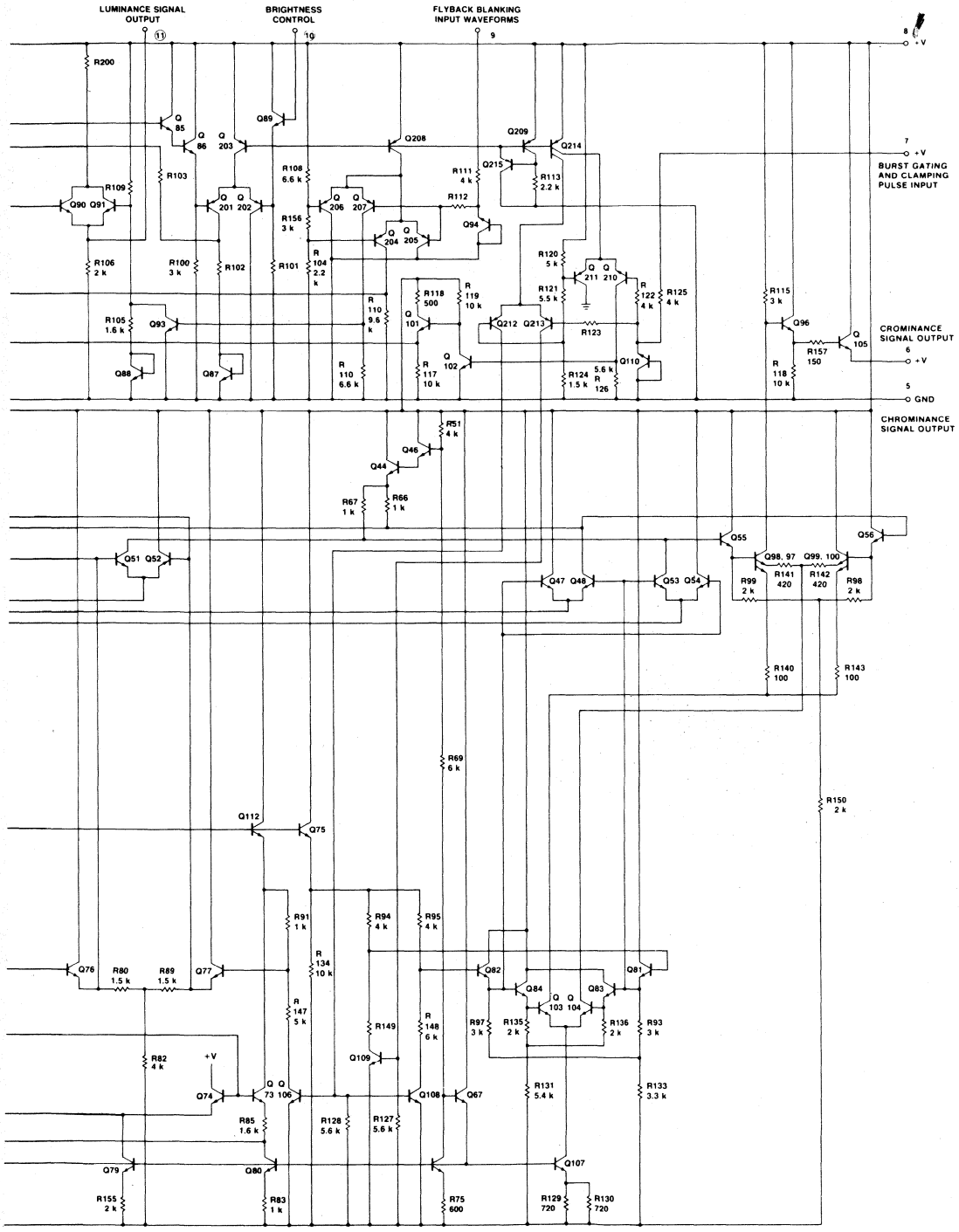
Supply Voltage	14 V
Power Dissipation	930 mW
Operating Temperature Range	0°C to +65°C
Storage Temperature Range	-55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

ELECTRICAL CHARACTERISTICS: T_A = 25°C, V+ = 12 V, R_G = 2.7 kΩ; (see test circuit unless otherwise specified).

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range (V_8)		10	12	14	V
Supply Current (I_8)	Note 1		45		mA
Allowable Hum on Supply Line				100	mV_{pk-pk}
LUMINANCE AMPLIFIER (Note 2)					
Input Signal Current (I_{14}) Black to White Value			0.2		mA
Input-Bias Current (I_{14})			0.25		mA
Input Impedance	I_{14} = 0.25 mA		150		Ω
Gain (Pin 13)	Notes 2, 5		40		dB
Contrast Control Range		20			dB
Contrast Control Voltage Range (V_{16})	See Figure 1		2-4		V
Contrast Control Current (I_{16})				8.0	μA
Black Level Range (V_{10})		1.0		3.0	V
Brightness Control Voltage Range (V_{11})			1 to 3		V
Brightness Control Current (I_{11})	$V_{11} \geq 4$ V			20	μA
Black Level Stability with Temperature			0.1		mV/°C
Black Level Stability with Contrast (V_{10}) See Applications section Pin 10	I_{14} = 0.25 mA			10	mV
Bandwidth (-3 dB)	Nominal Contrast	5.0			MHz
Output Voltage (V_{10}) (Black to White)	Max. Contrast, I_{14} = 0.2 mA		3.0		V
Output Voltage (V_{15}) (Black to White)	Sync Positive I_{14} = 0.2 mA (Black to White)		3.4		V_{pk-pk}
BLACK LEVEL CLAMP PULSE					
ON Level V_7	Note 3	7.0		V+	V
OFF Level V_7	See Figure 3			5.0	V
BLANKING PULSE	Note 4 (See Figure 4)				
ON Level V_9	V_{10} = 0 V	2.5		4.5	V
OFF Level V_9				1.5	V
ON Level V_9	V_{10} = 1.5 V	6.0		V+	V
OFF Level V_9				4.5	V
CHROMINANCE AMPLIFIER	Note 6				
Input Signal V_2		4.0		80	mV_{pk-pk}
Chroma Output Signal V_6	Nominal Contrast and Saturation V_{burst} = 1 V_{pk-pk}		2.0		V_{pk-pk}
Maximum Chroma Output V_6	V_{burst} = 1 V_{pk-pk}		4.6		V_{pk-pk}
Bandwidth (-3 dB)		6.0			MHz
Ratio of Burst to Chroma at Nominal Contrast and Saturation	See Note 2, 6, and 7		1:2		V/V
ACC Starting Voltage - V_3	Note 8		1.2		V
ACC Range		30			dB
Tracking between Luma and Chroma with Contrast Control	10 dB Contrast Control Adjustment		±1.0		dB
Saturation Control Range		20			dB
Saturation Control Voltage Range	See Figure 2		2-4		V
Gating Pulse					
ON Level V_7		2.3		5.0	V
OFF Level V_7	See Figure 3			1.0	V
Width		8.0			μs
Signal pulse Noise to Noise Ratio	Nominal Input Voltage	46			dB
Phase Shift between Burst and Chroma				5.0	°

EQUIVALENT CIRCUIT




LUMINANCE SIGNAL OUTPUT
BRIGHTNESS CONTROL
FLYBACK BLANKING INPUT WAVEFORMS
BURST GATING AND CLAMPING PULSE INPUT
CROMINANCE SIGNAL OUTPUT
CHROMINANCE SIGNAL OUTPUT
+V
GND

RELATIVE CONTRAST GAIN AS A FUNCTION OF CONTROL VOLTAGE

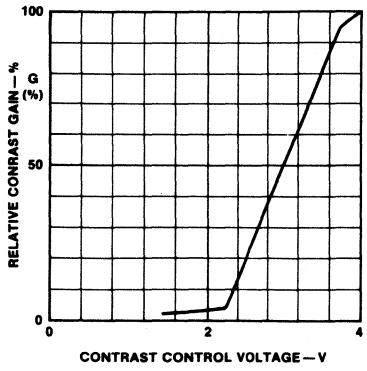


Fig. 1

RELATIVE SATURATION GAIN AS A FUNCTION OF CONTROL VOLTAGE

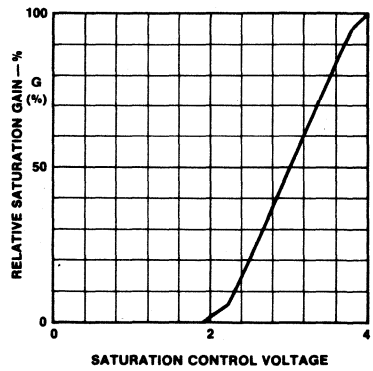


Fig. 2

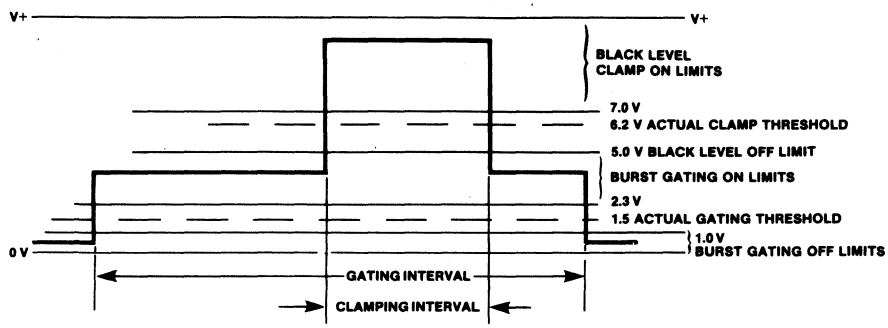


Fig. 3 PIN 7 INPUT VOLTAGE (SANDCASTLE PULSE)

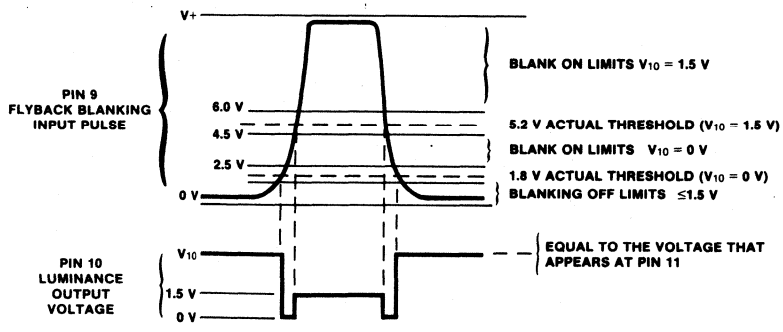


Fig. 4 DUAL THRESHOLD LUMINANCE BLANKING

NOTES:

1. Load on pin 6 is 1.5 kΩ. No load on pins 10 and 15.

2. Nominal contrast is defined as maximum contrast -3 dB
   Nominal Saturation is defined as maximum saturation -6 dB

3. This pulse (pin 7) is used for gating the chrominance amplifier and black level clamping. The latter function is actuated at +7 V. The input pulse must have an amplitude such that the clamping circuit is active only during the back porch of the blanking interval. The gating pulse switches the gain of the chroma amplifier to maximum during the flyback time, when the pulse rises above 2.3 V and switches it back to the normal setting when the pulse falls below 1 V.

4. This pulse (pin 9) is used for blanking the luminance amplifier. When the pulse exceeds +2.5 V, the output signal is blanked to a level of about 0 V. When the input exceeds +6 V, a fixed level of about +1.5 V is inserted in the output signal. This level can be used for clamping purposes.

5. The gain of the luminance amplifiers may be adjusted by varying R_G (see test circuit). R_G adjusts the gain of the contrast control circuit. This circuit configuration was chosen to keep the variation in gain to a minimum. With this design, the variation in gain is primarily a function of the ratio of the delay line matching resistors to R_G. At $R_G = 2.7\ k\Omega$, the output voltage at nominal contrast is 3 V black-to-white with an input current of 0.2 mA black-to-white. Under thse conditions the gain is;

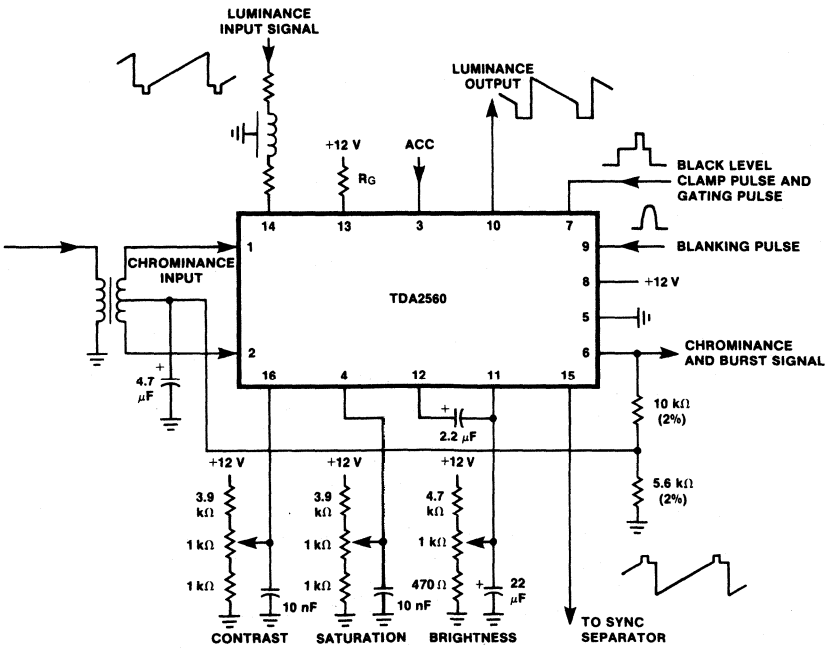
$$A_V = 20 \log \frac{\Delta V_{OUT}}{\Delta I_{IN} \times R_{IN}} = 20 \log \left(\frac{3\ V}{(.2\ mA)\ (150\ \Omega)} \right) = 40\ dB$$

6. All measurements of the chrominance signal are based on a color bar signal with 75% saturation; i.e., the burst-to-chrominance ratio is 1:2.

7. The chrominance and burst signal are both available on this pin (6). The burst signal is not affected by the contrast and saturation control and is kept constant by the ACC circuit of the TDA2522. The output of the delay line matrix circuit, which is the input of the TDA2522, is thus automatically compensated for insertion losses. Therefore, the output signal of the TDA2560 is determined by the insertion losses of the delay line. At nominal contrast and saturation setting, the ratio of the burst to the chrominance signal at the output is typically identical to that at the input.

8. A negative-going control voltage decreases the gain.

TEST AND APPLICATION CIRCUIT



APPLICATIONS INFORMATION

A basic description of the conditions and signals at each pin is shown below:

1. **BALANCED CHROMINANCE INPUT SIGNAL (in conjunction with pin 2)**
The balanced input signal is derived from the chrominance bandpass filter, which is designed to provide a push-pull input. A signal amplitude of at least 4 mV peak-to-peak is required between pins 1 and 2. The chrominance amplifier is stabilized by an external feedback loop from the output (pin 6) to the input (pins 1 and 2). The required level at pins 1 and 2 is 3 V. All measurements of the chrominance signals are based on a color bar signal with 75% saturation: i.e., the burst-to-chrominance ratio of the input signal is 1 : 2.

2. **CHROMINANCE SIGNAL INPUT (see pin 1)**

3. **ACC INPUT**
A negative-going potential, starting at +1.2 V, gives a 40 db range of ACC. Maximum grain reduction is achieved at an input voltage of 500 mV.

4. **CHROMINANCE SATURATION CONTROL**
A control range of +6 dB to > -14 dB is provided over a range of dc potential on pin 4 from +2 to +4 V. The saturation control is a linear function of the control voltage.

5. **GROUND**

6. **CHROMINANCE SIGNAL OUTPUT**
For nominal settings of saturation and contrast controls (max. -6 dB for saturation, and max. -3 dB for contrast) both the chroma and burst are available at this pin, and in the same ratio as at the input pins 1 and 2. The burst signal is not affected by the saturation and contrast controls. The acc circuit of the TDA2522 will hold the color burst amplitude constant at the input of the TDA2522. As the PAL delay line is situated between the TDA2560 and TDA2522, there may be some variation of the nominal 1 V peak-to-peak burst output of the TDA2560, depending on the tolerances of the delay line. An external network is required from pin 6 of the TDA2560 to provide negative dc feedback in the chroma channel via pins 1 and 2.

7. **BURST GATING AND CLAMPING PULSE INPUT**
A two-level pulse is required at this pin to be used for burst gate and black level clamping. The black level clamp is activated when the pulse level is greater than 7 V. The timing of this interval should be such that no appreciable encroachment occurs into the sync pulse on picture line periods during normal operation of the receiver. The burst gate, which switches the gain of the chroma amplifier to maximum, requires that the input pulse at pin 7 should be sufficiently wide, at least 8 μs, at the actuating level of 2.3 V.

8. **V+**
Correct operation occurs within the range 10 to 14 V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design, this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels.

9. **FLYBACK BLANKING INPUT WAVEFORM**
This pin is used for blanking the luminance amplifier. When the input pulse exceeds +2.5 V, the output signal is blanked to a level of about 0 V. When the input exceeds +6 V, a fixed level of about 1.5 V is inserted in the output. This level can be used for clamping purposes.

10. **LUMINANCE SIGNAL OUTPUT**
An emitter follower provides a low impedance output signal of 3 V black-to-white amplitude at nominal contrast setting having a black level in the range 1 to 3 V. An external emitter load resistor is not required. The luminance amplitude available for nominal contrast may be modified according to the resistor value from pin 13 to the +12 V supply. At an input bias current of 0.25 mA during black level, the amplifier is compensated so that the black level shift does not exceed 10 mV as a function of contrast control setting. When the input current deviates from this value, the black level shift amounts to 100 mV/mA.

APPLICATIONS INFORMATION (continued)

11. **BRIGHTNESS CONTROL**

The black level at the luminance output (pin 10) is identical to the control voltage required at this pin. A range of black level from 1 to 3 V may be obtained.

12. **BLACK LEVEL CLAMP CAPACITOR**

13. **LUMINANCE GAIN SETTING RESISTOR**

The gain of the luminance amplifier may be adjusted by selection of the resistor value from pin 13 to +12 V. The nominal luminance output amplitude is 3 V black-to-white at pin 10 when this resistor is 2.7 kΩ, and the input current is 0.2 mA black-to-white. Maximum and minimum values of this resistor are 3.9 kΩ and 1.8 kΩ respectively.

14. **LUMINANCE SIGNAL INPUT**

A low input impedance in the form of a current sink is obtained at this pin. Nominal input current is 0.2 mA black-to-white. The luminance signal may be coupled to pin 14 using a dc blocking capacitor and, in addition, a resistor employed to give a dc current into pin 14 at black level of about 0.25 mA.

15. **LUMINANCE SIGNAL OUTPUT FOR SYNC SEPARATOR PURPOSES**

A luminance signal output with positive-going sync is available which is not affected by the contrast control or the value of resistor at pin 13. This voltage is intended for drive of sync separator circuits. The output amplitude is 3.4 V peak-to-peak when the luminance signal input is 0.2 mA black-to-white.

16. **CONTRAST CONTROL**

With 3 V on this pin, the gain of the luminance channel is such that 0.2 mA black-to-white at pin 14 gives a luminance output on pin 10 of 3 V black-to-white. The nominal value of 2.7 kΩ is then assumed for the resistor from pin 13 to the +12 V supply. The variation of control potential at pin 16 from 2 to 4 V gives -17 to +3 dB gain variation of the luminance channel. A similar variation in the chrominance channel occurs in order to provide correct tracking between the two signals.

TDA2590

TV HORIZONTAL OSCILLATOR COMBINATION

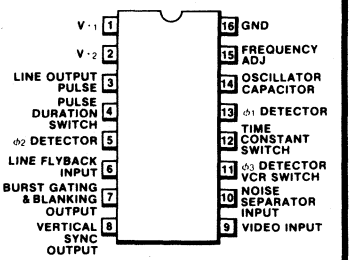
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The TDA2590 is a monolithic integrated circuit designed as a horizontal oscillator combination for TV receivers and monitors. It is constructed using the Fairchild Planar* process.

- **LINE OSCILLATOR USING THE THRESHOLD SWITCHING PRINCIPLE**
- **PHASE COMPARISON BETWEEN SYNC PULSE AND OSCILLATOR VOLTAGE (ϕ_1)**
- **PHASE COMPARISON BETWEEN LINE FLYBACK PULSE AND OSCILLATOR VOLTAGE (ϕ_2)**
- **SWITCH FOR CHANGING THE FILTER CHARACTERISTIC AND THE GATE CIRCUIT (WHEN USED FOR VCR)**
- **COINCIDENCE DETECTOR (ϕ_3)**
- **SYNC SEPARATOR**
- **NOISE SEPARATOR**
- **VERTICAL SYNC SEPARATOR AND OUTPUT STAGE**
- **COLOR BURST KEYING AND LINE FLYBACK BLANKING PULSE GENERATOR**
- **PHASE SHIFTER FOR THE OUTPUT PULSE**
- **OUTPUT PULSE DURATION SWITCHING**
- **OUTPUT STAGE FOR DIRECT DRIVE OF THYRISTOR DEFLECTION CIRCUITS**
- **SYNC GATING PULSE GENERATOR**
- **LOW SUPPLY VOLTAGE PROTECTION**

*Planar is a patented Fairchild process.

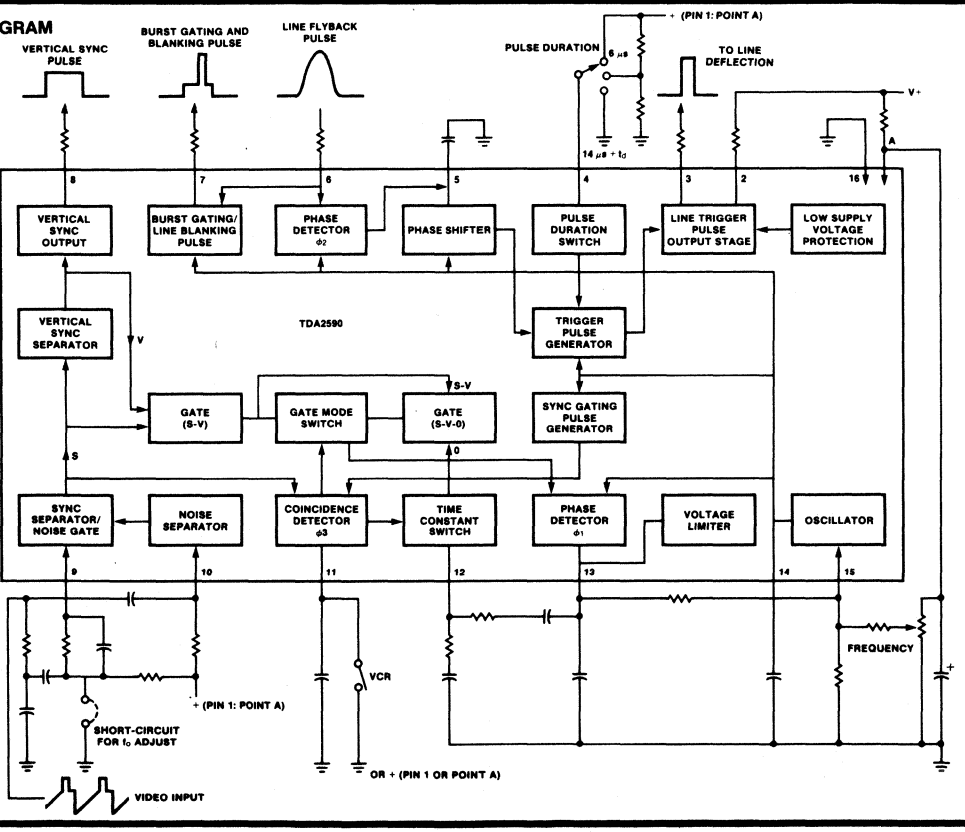
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

TYPE	PART NO.
2590	TDA2590

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage at Pin 1 (When Supplied by the IC)	13.2 V
Supply Voltage at Pin 2	18 V
Power Dissipation	800 mW
Storage Temperature	-25°C to +125°C
Operating Temperature	-20°C to +60°C
Pin Temperature (Soldering, 10 s)	260°C

VOLTAGES

V_4, V_{11}	0 to 13.2 V
V_9, V_{10}	-6 to +6 V

CURRENTS

I_2 (peak)	400 mA
I_3 (peak)	-400 mA
I_4	1 mA
I_6	±10 mA
I_7	-10 mA
I_{11}	2 mA

4

ELECTRICAL CHARACTERISTICS: T_A = 25°C; V_1 = 12 V, See test circuit unless otherwise noted.

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_1			30		mA
SYNC SEPARATOR (PIN 9)						
Input Switching Voltage	V_9			0.8		V
Input Keying Current	I_9			5	100	μA
Input Blocking Current	I_9	V_9 = -5 V			1	μA
Input Switching Current	I_9				5	μA
Input Voltage ($_{pk-pk}$)	V_9	Sync Positive Video Signal	1	3	7	V_{pk-pk}
NOISE SEPARATOR (PIN 10)						
Input Switching Voltage	V_{10}			1.4		V
Input Keying Current	I_{10}			5	100	μA
Input Switching Current	I_{10}			150		μA
Input Blocking Current	I_{10}	V_{10} = -5 V			1	μA
Input Voltage (pk-pk)	V_{10}	Sync Positive Video Signal	1	3	7	V_{pk-pk}
Superimposed Noise Voltage ($_{pk-pk}$)	V_n				7	V_{pk-pk}
LINE FLYBACK PULSE (PIN 6)						
Input Current	I_6		10			μA
Input Switching Voltage	V_6			1.4		V
Input Limiting Voltage	V_6			-0.7 to +1.4		V
Input Resistance	R_6			400		Ω
PULSE DURATION SWITCH (PIN 4)						
Input Voltage	V_4	t = 0 μs, V_3 = 0 (Note 1)		5.4 to 6.5		V
		t = 6 μs		9.4 to V_1		V
		t = 14 μs + td (Note 6)		0 to 4		V
Input Current	I_4	t = 0 μs, V_3 = 0		0		μA
		t = 6 μs	200			μA
		t = 14 μs + td (Note 6)			-200	μA

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$; $V_1 = 12$ V, See test circuit unless otherwise noted. (Cont'd)

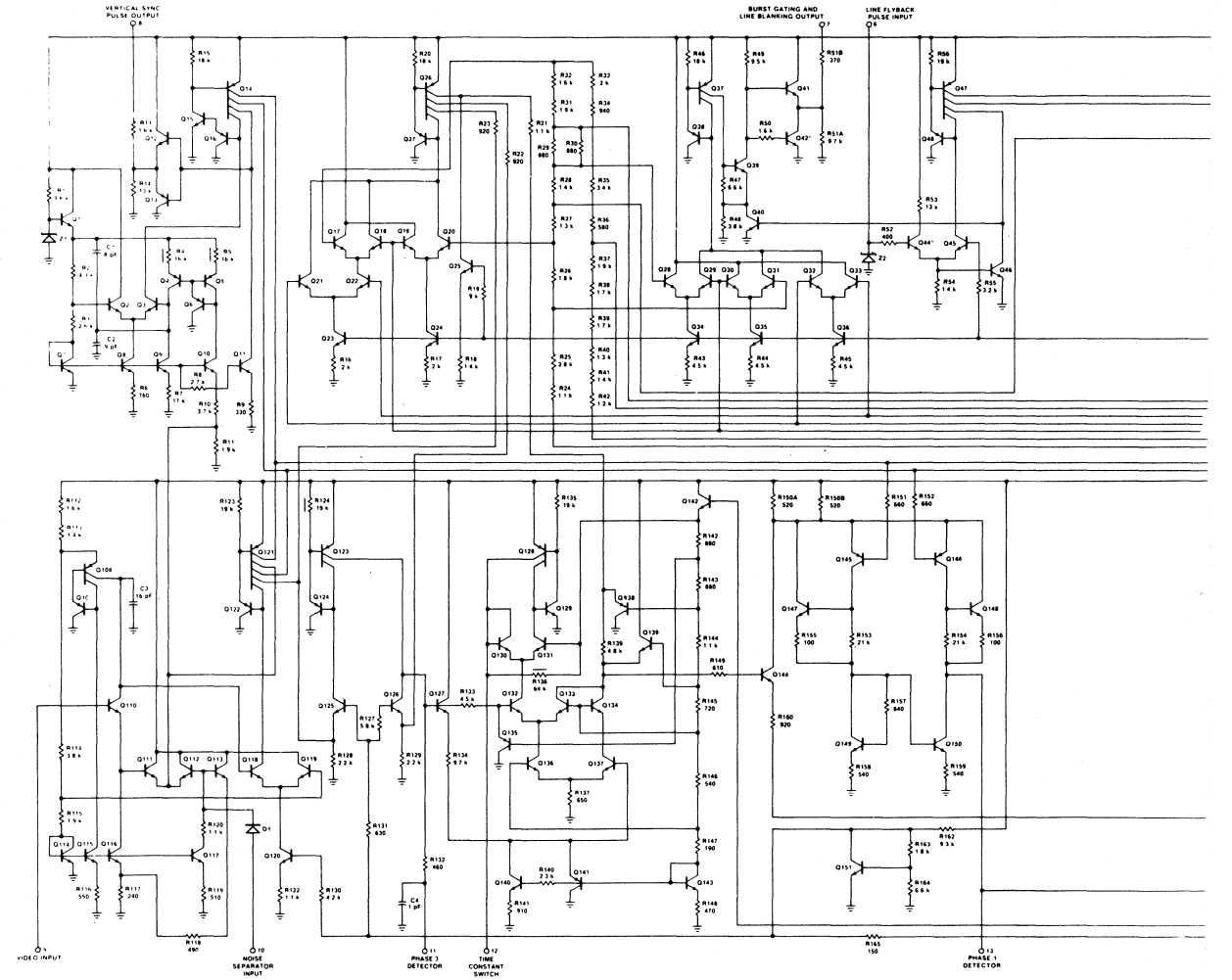
CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR (PIN 14 and PIN 15)						
Low Level Threshold Voltage	V_{14}			4.4		V
High Level Threshold Voltage	V_{14}			7.6		V
Discharge Current	I_{14}			±.47		mA
Free Running Frequency	f_o	$C_{14} = 4.7$ nF, $R_{15} = 12$ kΩ		15625		Hz
Spread of Frequency	$\Delta f_o/f_o$	Note 4	-5		+5	%
Frequency Control Sensitivity	$\Delta f_o/\Delta I_{15}$			31		Hz/μA
Adjustment Range	$\Delta f_o/f_o$			±10		%
Frequency Change With Supply Voltage	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	$V_1 = 12$ V, Note 4	-.05		+.05	
Frequency Change With Supply Voltage	Δf_o	$V_1 = 12$ to 5 V, Note 4	10		+10	%
Temperature Coefficient of Oscillator Frequency per °C		Note 4	-10^{-4}		$+10^{-4}$	
COINCIDENCE DETECTOR (ϕ_3) and SWITCHING ON VCR (PIN 11)						
Input Voltage	V_{11}	Note 2		0 to 1.5		V
Input Current	I_{11}	Note 2			-200	μA
Input Voltage	V_{11}			9 to V_1		V
Input Current	I_{11}			1 to 2		mA
Output Voltage	V_{11}			0.5 to 6		V
Peak Output Current	I_{11}	Without Coincidence		0.1		mA
Peak Output Current	I_{11}	With Coincidence		-0.5		mA
VERTICAL SYNC PULSE (PIN 8)		Positive Going				
Output Voltage	V_8		10	11		V_{pk-pk}
Output Resistance	R_8			2		kΩ
Turn-ON Delay	t_{on}	Delay between leading edge of input & output signal		12		μs
Turn-OFF Delay	t_{off}	Delay between trailing edge of input & output signal	t_{on}			μs
BLANKING AND BURST GATING PULSE (PIN 7)		Positive Going				
Burst Gating Pulse Output Voltage	V_7		10	11		V_{pk-pk}
Output Resistance	R_7			400		Ω
Phase Relationship to Leading Edge	t	Note 3 $V_7 = 7$ V		1.9 typ 1.0 to 2.8		μs
Phase Relationship to Trailing Edge	t	Note 3 $V_7 = 7$ V		6.6 typ 5.8 to 7.4		μs
Blanking Pulse Output Voltage	V_7			2.5 to 3.5		V
LINE DRIVE PULSE (PIN 3)		Positive Going				
Output Voltage	V_3			10.5		V_{pk-pk}
Output Current (Average Value)	I_3			-100		mA
Output Resistance	R_3	For leading edge of Line Pulse		2.5		Ω
Output Resistance	R_3	For trailing edge of Line Pulse		20		Ω
Output Pulse Duration	t_p	$V_4 > 9.4$ V		6 typ 4.5-7.5		μs
Output Pulse Duration	t_p	$V_4 < 4$ V, Note 6		14 + td		μs
Supply Voltage for Switching off the Output Pulse	V_1			4		V

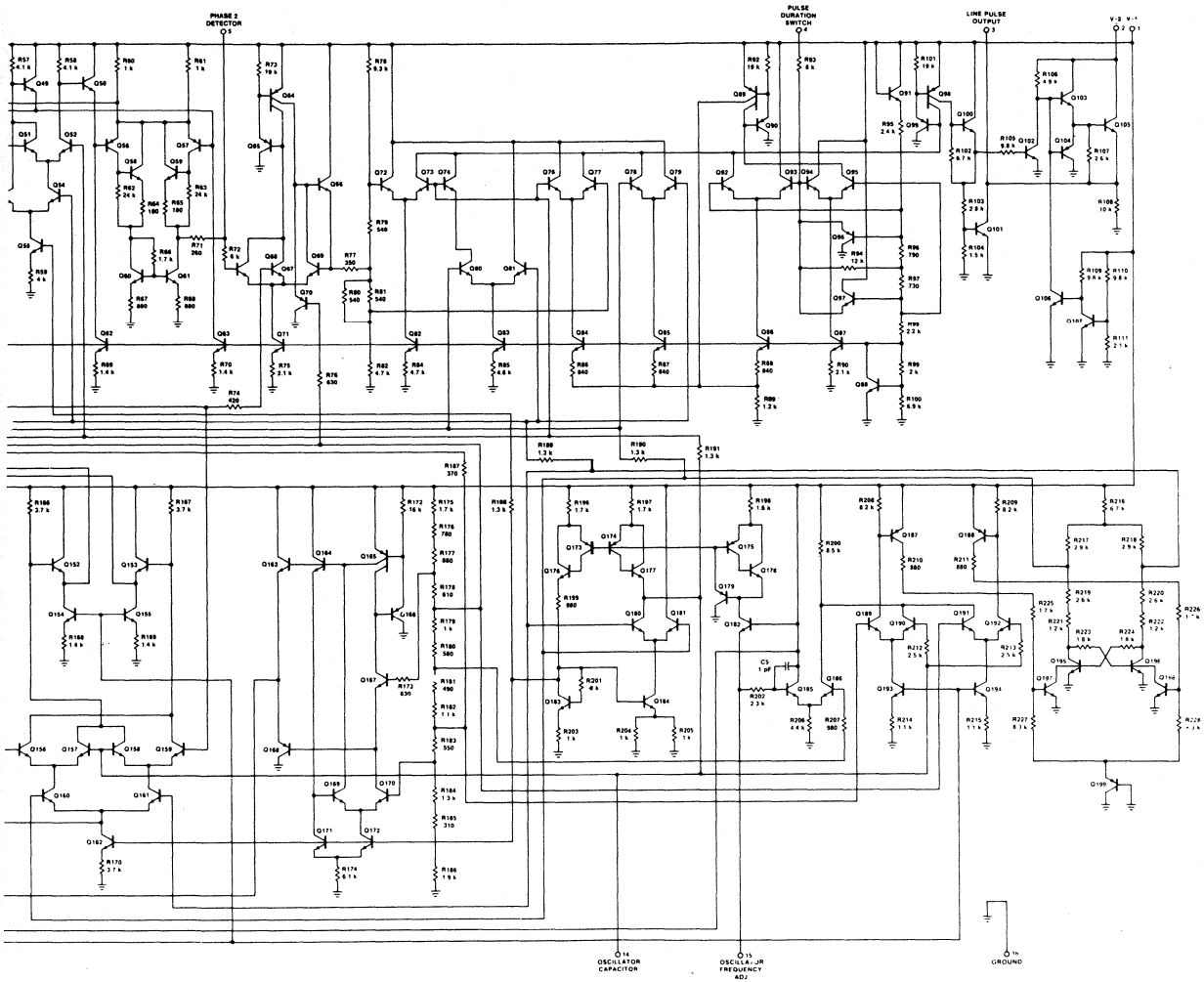
ELECTRICAL CHARACTERISTICS: T_A = 25°C; V_1 = 12 V, See test circuit unless otherwise noted. (Cont'd)

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
PHASE COMPARISON (ϕ_1) (PIN 13)		Sync Pulse/Oscillator				
Control Voltage Range	V_{13}			3.8 to 8.2		V
Peak Control Current	I_{13}			±2.1 typ ±1.9-2.3		mA
Output Blocking Current	I_{13}	V_{13} = 4 to 8 V			1	μA
Output Resistance	R_{13}	Current Source V_{13} = 4 to 8 V		High		ohmic
Output Resistance	R_{13}	Emitter Follower V_{13} < 3.8 or > 8.2 V		Low		ohmic
Control Sensitivity				2		kHz/μs
Capture & Holding Range	Δf	82 kΩ between Pins 13 & 15		±780		Hz
Spread of Capture & Holding Range	$\Delta(\Delta f)$	Note 4		±10		%
PHASE COMPARISON (ϕ_2) (PIN 5)		Oscillator/Line Flyback Pulse				
Control Voltage Range	V_5			5.4 to 7.6		V
Peak Control Current	I_5			±1		mA
Input Current at Blocked Phase Detector	I_5	V_5 = 5.4 to 7.6 V			5	μA
Output Resistance	R_5	Current Source V_5 = 5.4 to 7.6 V		High		ohmic
Output Resistance	R_5	V_5 = < 5.4 or > 7.6 V		8		kΩ
Allowable Delay between Leading Edge of Output Pulse and Leading Edge of Flyback Pulse (t_{fp} = 12 μs)	t_d			0-15		μs
Static Control Error	$\Delta t/\Delta td$				0.2	%
OVERALL PHASE RELATION		Note 5				
Phase Relation Between Middle of Sync Pulse and the Middle of the Flyback Pulse	t			2.6		μs
Tolerance of Phase Relationship	Δt		-0.7		+0.7	μs
TIME CONSTANT SWITCH (PIN 12)						
Output Voltage	V_{12}			6		V
Output Current	I_{12}		-1		+1	mA
Output Resistance	R_{12}	V_{11} = 2.5 to 7 V		100		Ω
Output Resistance	R_{12}	V_{11} = < 1.5 V or > 9 V		60		kΩ
INTERNAL GATING PULSE						
Pulse Duration	t_p			7.5		μs

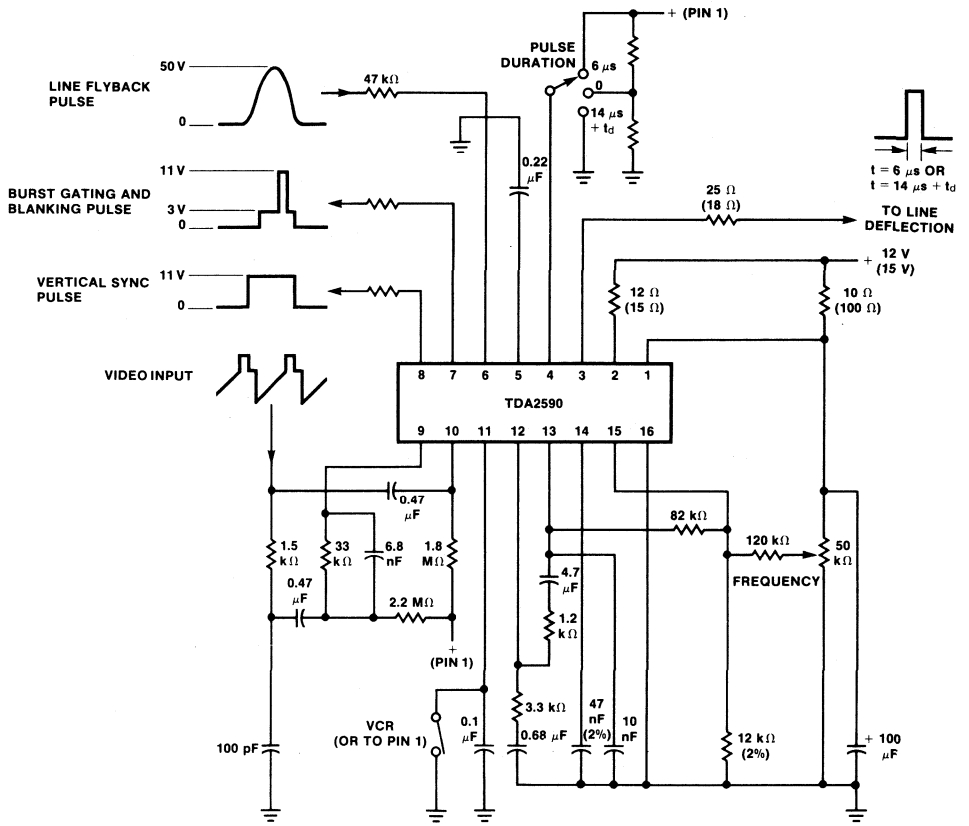
NOTES:
1. Can also be left unconnected.
2. When supplied by the IC.
3. Phase relationship between the middle of the sync pulse at the input and leading or trailing edge of the burst gating pulse.
4. Excluding the affect of variations in external components tolerances.
5. The adjustment of the overall phase relation and consequently the leading edge of the output pulse occurs automatically by phase control ϕ_2. If additional adjustment is used, the following values apply:
   ADJUSTMENT SENSITIVITY
   caused by: adjustment voltage $\Delta V_5/\Delta t$ typ 0.1 V/μs
   adjustment current $\Delta I_5/\Delta t$ typ 30 μA/μs
6. td = switch-OFF delay of the line output stage.

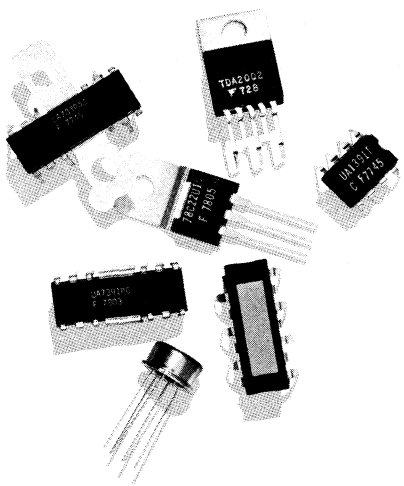
EQUIVALENT CIRCUIT




PHASE 2 DETECTOR
O 5
PULSE DURATION SWITCH
O 4
LINE PULSE OUTPUT
O 3
V-3 V-1
O 2 O 1
O 14
OSCILLATOR CAPACITOR
O 15
OSCILLATOR FREQUENCY ADJ
O 16
GROUND

TEST AND APPLICATIONS CIRCUIT





ORDER INFORMATION

Three basic units of information are contained in the code.

μA703	H	C
Device Type	Package Type	Temperature Range

DEVICE TYPE

This group of alpha numeric characters defines the data sheet which specifies the device functional and electrical characteristics.

PACKAGE TYPE

One letter represents the basic package style.

- D = Dual In-line Package (Hermetic, Ceramic)
- F = Flatpak (Hermetic)
- H = Metal Can Package
- J = Metal Power Package (TO-66 Outline)
- K = Metal Power Package (TO-3 Outline)
- P = Dual In-line Package (Molded)
- R = Mini DIP (Hermetic, Ceramic)*
- T = Mini DIP (Molded)
- U = Power Package (Molded, TO-220 Outline)

*Refer to individual data sheets for details. For special requirements, contact factory.

Different outlines exist within each package style to accommodate various die sizes and number of leads. Specific dimensions for each package can be found in the PACKAGE OUTLINES section of this catalog.

TEMPERATURE RANGE

Two basic temperature grades are in common use:

C = Commercial/Industrial/Consumer	M = Military
0°C to +70/75°C	−55°C to +125°C
−20°C to +85°C	−55°C to + 85°C
−40°C to +60°C	
−40°C to +85°C	

Exact values and conditions are indicated on the individual data sheets.

EXAMPLES

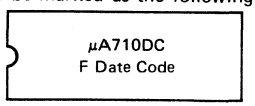
1. μA710FM
   This number code indicates a μA710 Voltage Comparator in a flatpak with military temperature rating capability.

2. μA725EHC
   This number code indicates a μA725 Instrumentation Operational Amplifier, electrical option E, in a metal can with a commercial temperature rating capability.

3. μA725EHCG
   This number code indicates the identical device as in example 2. Except it has a gold plated kovar header; the standard header is tin dipped.

DEVICE IDENTIFICATION/MARKING

All Fairchild standard catalog linear circuits will be marked as the following example:



UNIQUE 38510 PROCESSING

Additional processing to Fairchild Unique 38510 specifications is indicated by noting the appropriate requirements (QB, QC) after the standard order code.

Detailed ordering procedures are provided in the OEM price list.

MATRIX VI PROGRAM

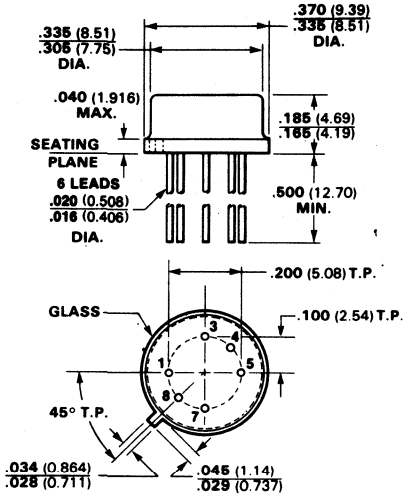
Additional screening to the Fairchild Matrix VI program is indicated by the QM or QR suffix to the standard order code.

OLD ORDER CODES

Devices may continue to be purchased against old order codes (Example: U5R7723393; now 723HC). However, all products will be marked with new order codes unless otherwise specified.

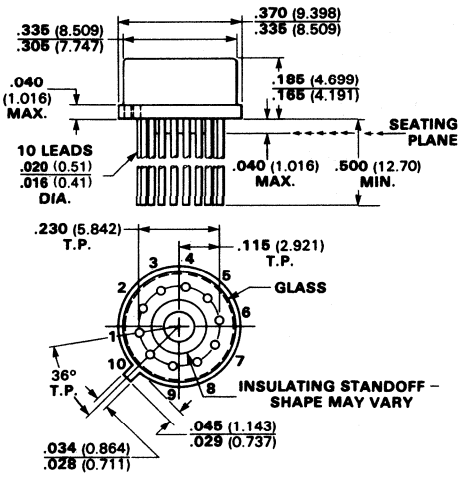
PACKAGE OUTLINES

In Accordance with JEDEC (TO-78) **(H)5C**



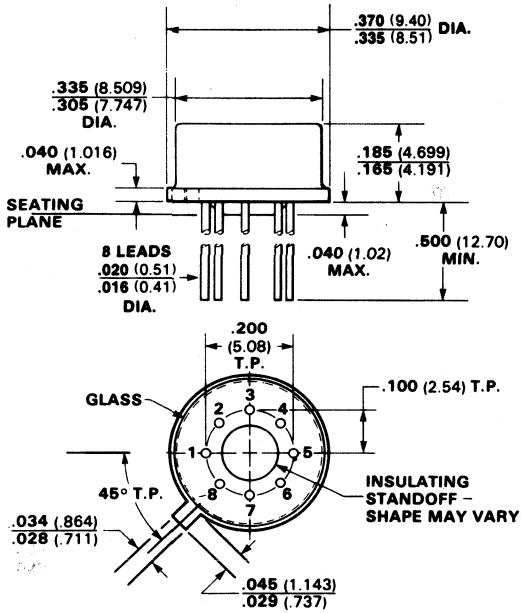
NOTES:
Pins are solder dipped to within .040 of seating plane
Six pins through
Pins 2 and 6 are omitted
50 mil kovar header
Package weight is 0.95 gram

In Accordance with JEDEC (TO-100) **(H)5Q**



NOTES:
Pins solder dipped to the seating plane
Ten pins thru
15 mil kovar header
Package weight is 1.32 grams

In Accordance with JEDEC (TO-99) **(H)5S**

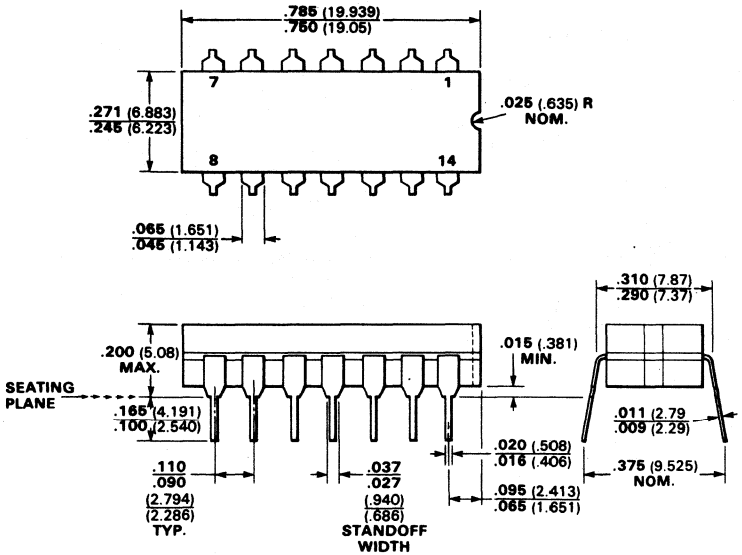


NOTES:
Pins are solder dipped to seating plane
Seven leads thru, pins No. 4 connected to case
15 mil kovar header
Package weight is 1.22 grams

All dimensions in inches **(bold)** and millimeters (parentheses)

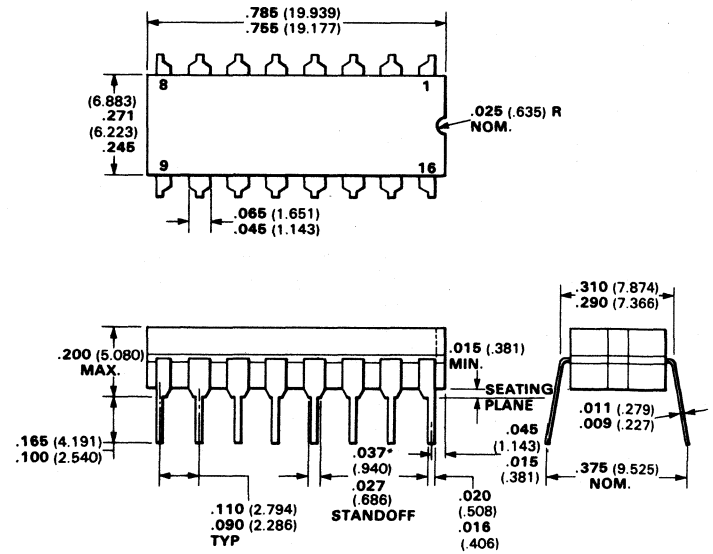
PACKAGE OUTLINES

In Accordance with JEDEC (TO-116) 14-Pin Hermetic Dual In-Line **(D)6A**



NOTES:
Pins are intended for insertion in hole rows on .300" (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" (0.508) diameter pin
Pins are alloy 42
Package weight is 2.0 grams

16-Pin Hermetic Dual In-Line **(D)6B**



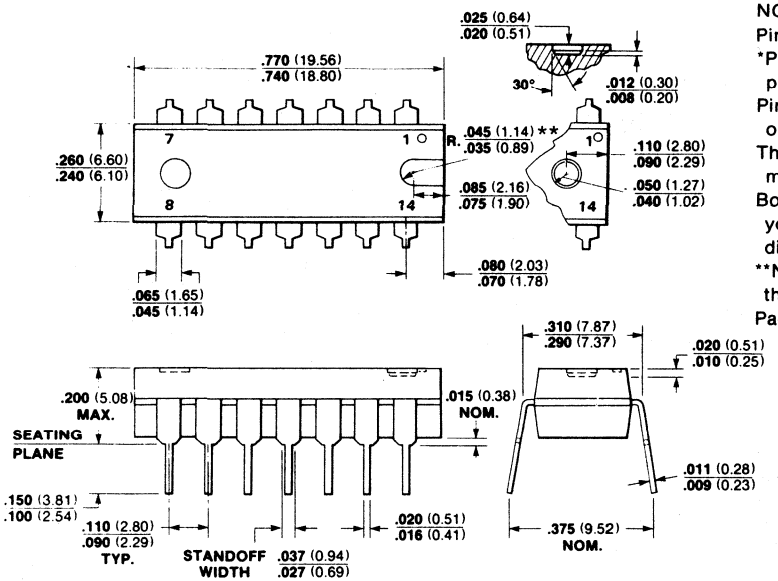
NOTES:
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on .300" centers (7.62)
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin (0.51)
Hermetically sealed alumina package
Cavity size is .110 x .140 (2.79 x 3.56)
Package weight is 2.0 grams
*The .037-.027 dimension does not apply to the corner pins

All dimensions in inches **(bold)** and millimeters (parentheses)

PACKAGE OUTLINES

14-Pin *Plastic Dual In-Line In accordance with JEDEC (TO-116) Outline

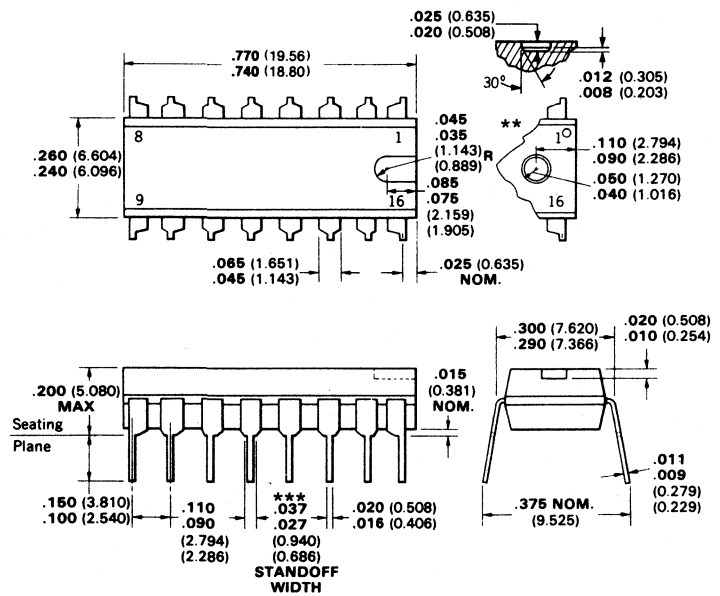
(P)9A



NOTES:
Pins are tin-plated copper
*Package material varies depending on the product line
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (0.508) inch diameter pin
**Notch or ejector hole varies depending on the product line
Package weight is 0.9 gram

16-Pin*Molded Plastic Dual In-Line

(P)9B



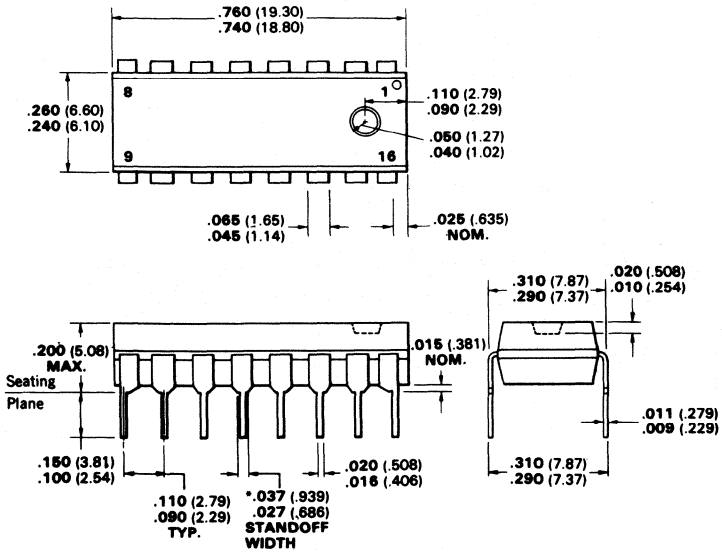
NOTES:
Pins are tin-plated copper
Pins are intended for insertion in hole rows on .300" (7.62) centers
Pins purposely have a "positive" *misalignment to facilitate insertion*
Board-drilling dimensions should equal your practice for .020 inch (0.51) diameter pin
Package weight is 0.9 gram
*Package material varies depending on the product line
***The .037-.027 (0.94-0.69) dimension does not apply to the corner pins
**Notch or ejector hole varies depending on the product line

All dimensions in inches **(bold)** and millimeters (parentheses)

PACKAGE OUTLINES

16-Pin Molded Dual In-Line
9B Package for all TAA, TBA and TDA types

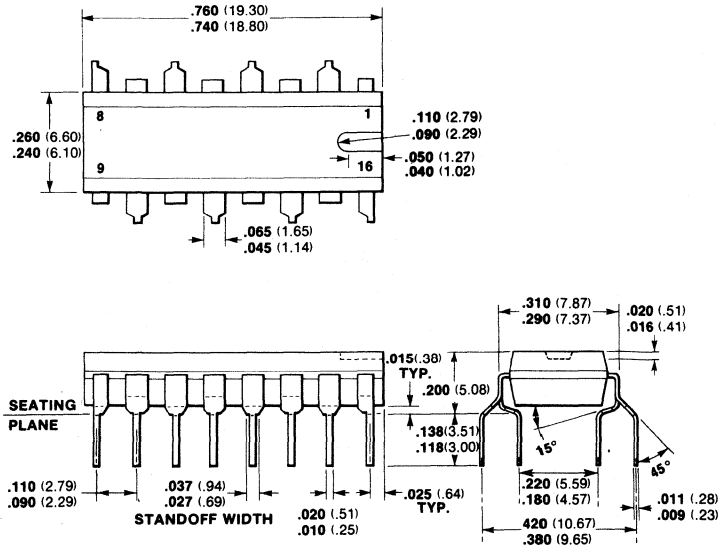
9B



NOTES:
Pins are tin-plated copper
Pins are intended for insertion in hole rows on .300" (7.62) centers
Board-drilling dimensions should equal your practice for .020 inch (0.51) diameter pin
Package weight is 0.9 gram
*Package material varies depending on the product line
***The .037-.027 (0.94-0.69) dimension does not apply to the corner pins
**Notch or ejector hole varies depending on the product line

16-Pin Molded Quad In-Line
9D Quad Package for all TAA, TBA, TDA types

9D

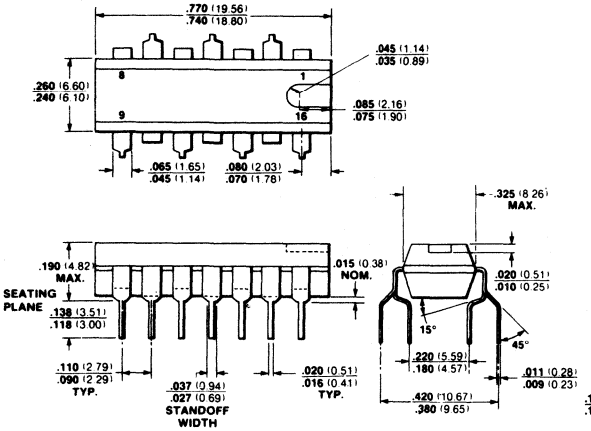


NOTES:
Pins are tin-plated copper
Pins are intended for insertion in hole rows on .300" (7.62) centers
Board-drilling dimensions should equal your practice for .020 inch (0.51) diameter pin
Package weight is 0.9 gram
*Package material varies depending on the product line
**The .037-.027 (0.94-0.69) dimension does not apply to the corner pins

All dimensions in inches **(bold)** and millimeters (parentheses)

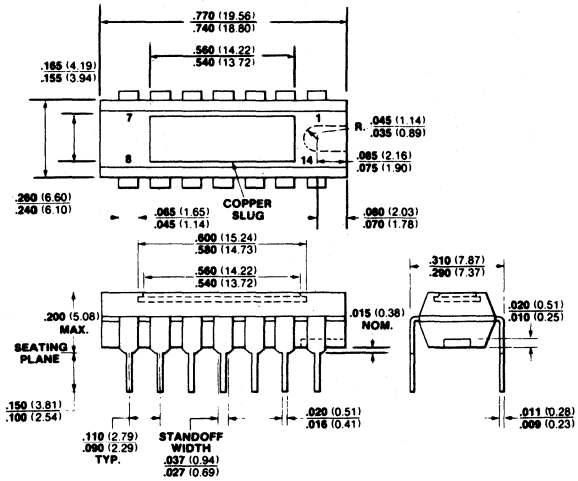
PACKAGE OUTLINES

14-Pin Plastic Quad In-Line (JEDEC TO-116 Outline*) (L)9C



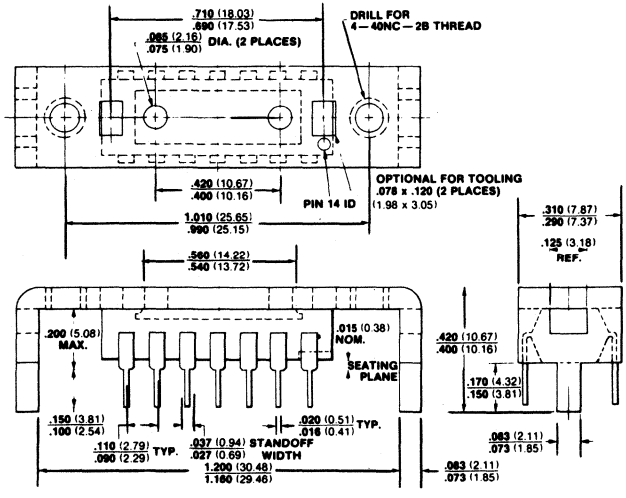
NOTES:
Pins are tin-plated copper
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter pin
Package weight is 0.9 gram
*This is a 9A package with the pins formed in assembly

14-Pin Plastic Dual In-Line (With Copper Slug) (AP)9H



NOTES:
Pins are tin-plated kovar
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter lead
Package material is epoxy with copper slug
Package weight is 0.9 gram
Pin 14 is identified by an indentation on underside of package

14-Pin Plastic Dual In-Line (Copper Slug and Heat Bracket)* (BP)9J

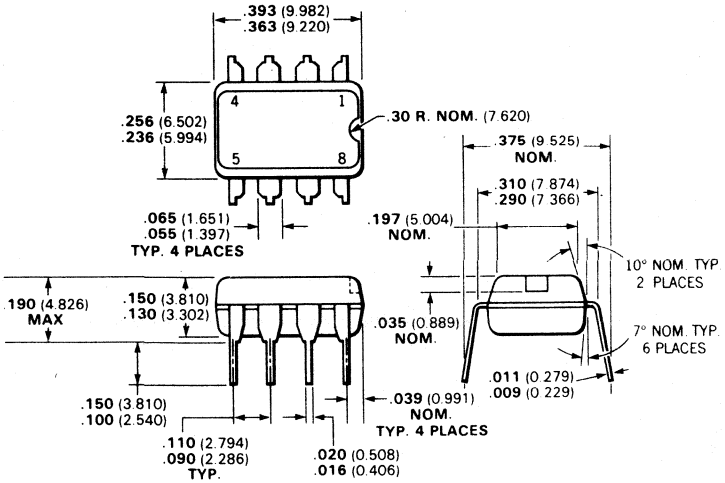


NOTES:
Pins are tin-plated kovar
Package materisl is epoxy with copper slug and tin-plated bracket
Board-drilling dimensions should equal your practice for .020 (0.51) diameter pin
*Package is the same as 9H except that a heat bracket is attached
Pin 14 is identified by an indentation on underside of package

All dimensions in inches **(bold)** and millimeters (parentheses)

PACKAGE OUTLINES

8-Pin Molded Dual In-Line (T)9T

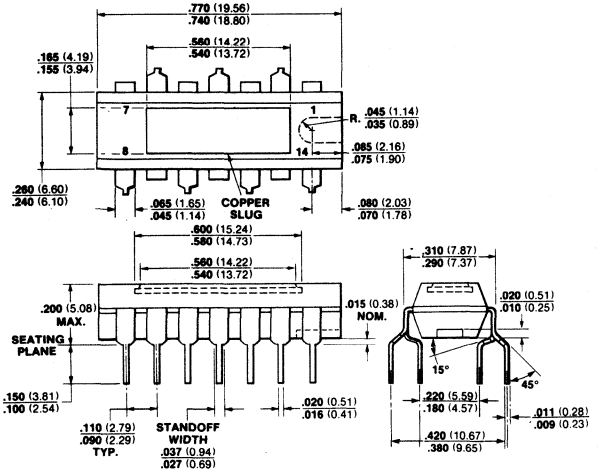


NOTES:
Pins are tin-plated copper
Package material is plastic
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter pin
Package weight is 0.6 gram

All dimensions in inches **(bold)** and millimeters (parentheses)

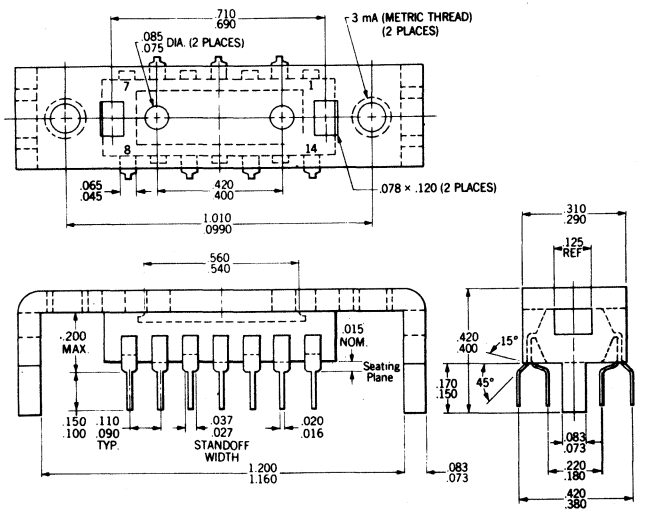
PACKAGE OUTLINES

14-Pin Plastic Quad In-Line (With Copper Slug) — A12



NOTES:
Pins are tin-plated kovar
Package material is epoxy with copper slug
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter pin
Pin 14 identified by indentation on underside

14-Pin Plastic Quad In-Line (Copper Slug and Heat Bracket)* — B11

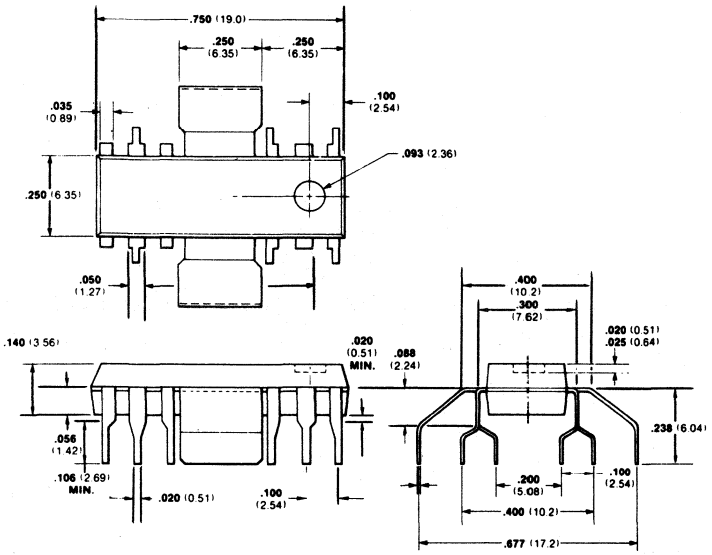


NOTES:
Pins are tin-plated kovar
Package material is epoxy with copper slug and tin-plated bracket
Board-drilling dimensions for pins should equal your practice for .020 (0.51) inch diameter pin
Pin 14 identified by indentation on underside

All dimensions in inches **(bold)** and millimeters (parentheses)

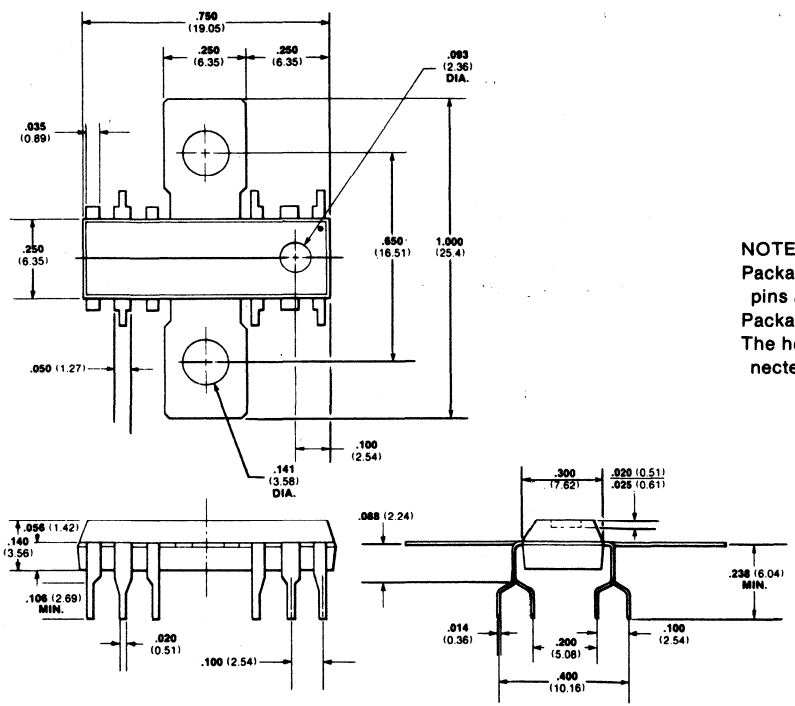
PACKAGE OUTLINES

12-Pin Power Plastic Package (P3) 9W



NOTES:
Package is plastic with tin-plated copper pins and wings
Package weight is 0.9 gram
The heat sinking tabs are electrically connected to the most negative potential pin

12-Pin Power Plastic Package (P4) 9W

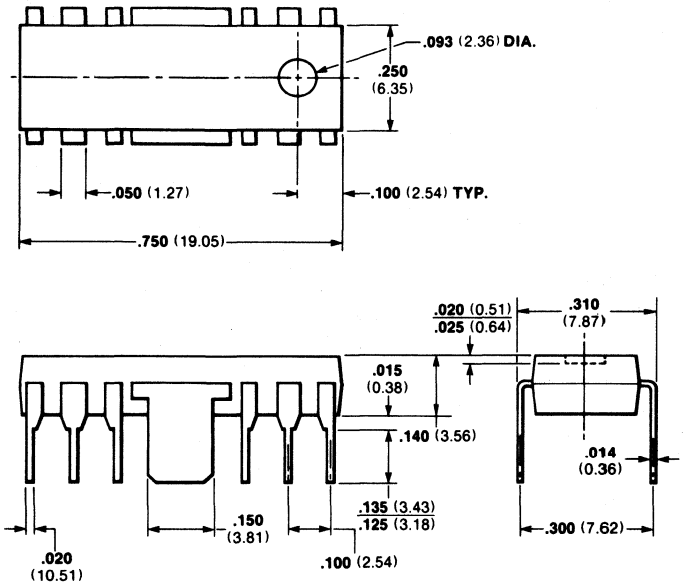


NOTES:
Package is plastic with tin-plated copper pins and wings
Package weight is 0.9 gram
The heat sinking tabs are electrically connected to the most negative potential pin

All dimensions in inches **(bold)** and millimeters (parentheses)

PACKAGE OUTLINES

12-Pin Power Plastic Dual In-Line 9W (P6)

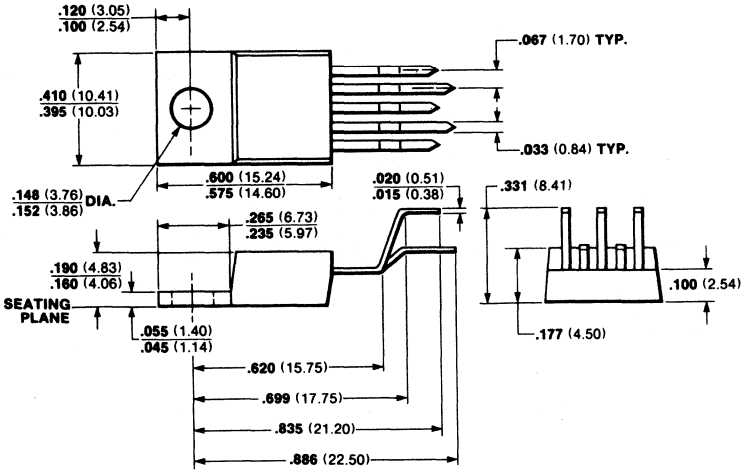


NOTES:
Package is plastic with tin-plated copper pins and wings
Package weight is 0.9 gram
The heat sinking tabs are electrically connected to the most negative potential pin

All dimensions in inches **(bold)** and millimeters (parentheses)

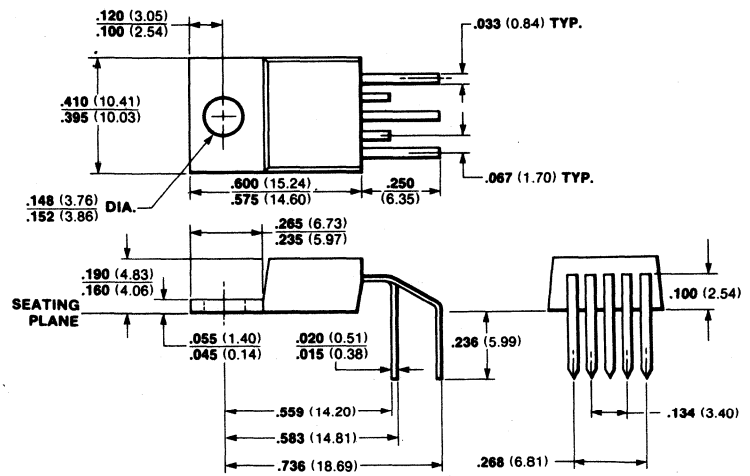
PACKAGE OUTLINES

5-Pin Power Package Vertical Mounting (V) GO



NOTES:
Mounting tab electrically connected to center pin
Package is molded over a copper base material with solderable pins
Package weight is 2.1 grams

5-Pin Power Package Horizontal Mounting (H) GO

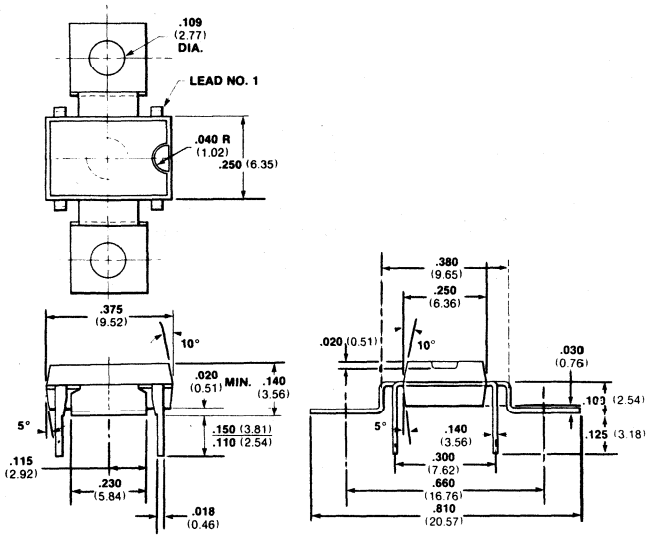


NOTES:
Mounting tab electrically connected to center pin
Package is molded over a copper base material with solderable pins
Package weight is 2.1 grams

All dimensions in inches **(bold)** and millimeters (parentheses)

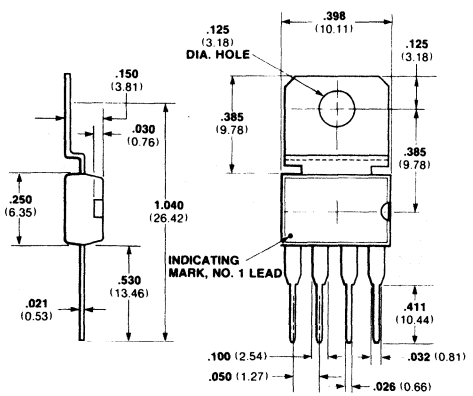
PACKAGE OUTLINES

4-Pin Power Mini DIP (T2)9V



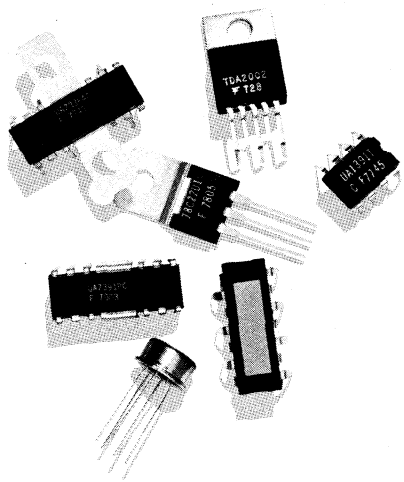
NOTES:
Package is plastic with tin-plated copper pins and wings
Package weight is 0.6 gram
T-2 package is intended to be mounted with the tabs flush with the top of the PC board. Either No. 2-56 screws or No. 2 rivets may be used to secure the package. Single or double-sided PC boards can be used. Thermal compound is recommended.

4-Pin Single Side Power Plastic Mini DIP (U1)8Z



NOTES:
Package is plastic with tin-plated copper pins
Board-drilling dimensions should equal your practice for .033 (0.84) inch diameter pins
Package weight is 0.6 gram
Tab is electrically insulated from leads
This package is intended to be mounted with the tab flush with the top of the PC board or heat sink. A No. 4 screw may be used to secure the package. Thermal compound is recommended.

All dimensions in inches **(bold)** and millimeters (parentheses)



FAIRCHILD SEMICONDUCTOR

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Via Flaminia Nuova 219
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Telex: 620630

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Telex: 26004

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76057 Le Havre Cedex
Tel: 16 35 21 34 00

Societe Aufray
Entrepots de la Asse Seine
Zone Industrielle
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Telex: 120257

Societe Gros S.A.
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54000 Nancy
Tel: 15 28 24 22
Telex: 8507

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15-17, Boulevard Bon Repos
31008 Toulouse Cedex
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Telex: 531501

S.R.D. (Societe de Representation et de Distribution)
88,' Rue du Commandant Mages
13001 Marseille
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Telex: 23382 KONT E

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Telex: 52927 ECROS E

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